Flexible dv/dt and di/dt Control Method for Insulated Gate Power Switches

Shihong Park, *Student Member, IEEE*, and Thomas M. Jahns, *Fellow, IEEE*

***Abstract*—Active gate control techniques are introduced in this paper for flexibly and independently controlling the dv/dt and di/dt of insulated gate power devices during hard-switching events. In the case of dv/dt control, the output voltage dv/dt can be controlled over a wide range by electronically adjusting the effective gate-to-drain (-collector) capacitance (i.e., Miller capacitance). For di/dt control, similar techniques are applied for electronically adjusting the output current di/dt over a wide range using voltage feedback from a small inductor connected in series with the switch's source (emitter) terminal. Both techniques are designed to maximize their compatibility with power module implementations that combine the power switch and its gate drive, including integrated circuit gate drives. Simulation and experimental results are included to verify the desirable performance characteristics of the presented dv/dt and di/dt control techniques.**

***Index Terms*—Driver circuits, electromagnetic interference (EMI), insulated gate bipolar transistors (IGBTs), insulated gate transistor switches, power MOSFETs, power FETs.**

I. Introduction

TECHNIQUES are often desired for actively controlling the output terminal dv/dt and di/dt of insulated gate power devices such as MOSFETs and insulated gate bipolar transistors (IGBTs) in hard-switched converters in order to reduce electromagnetic interference (EMI) and voltage overshoots without requiring bulky and lossy snubber circuits [1]–[4]. In hard-switched applications requiring series or parallel connections of several MOS-gated power switches, these dv/dt and di/dt control techniques are critical to insuring that the voltage or current is properly shared among the power devices during the switching transients.

Several techniques have been reported for providing such features using gate control schemes [5]–[9]. Most of this prior work has been targeted at improved voltage sharing among series-connected switches without providing external control of the dv/dt or di/dt rates. An exception is [8], which uses a closed-loop op-amp circuit to actively control the collector voltage during switching transients.

Paper IPCSD 02–066, presented at the 2001 Industry Applications Society Annual Meeting, Chicago, IL, September 30–October 5, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Power Electronics and Devices Committee of the IEEE Industry Applications Society. Manuscript submitted for review October 1, 2001 and released for publication February 20, 2003. This work was supported by the ERC Program of the National Science Foundation under Award Number EEC-9731677 and by the Center for Power Electronics Systems (CPES), an Engineering Research Center sponsored by the National Science Foundation.

The authors are with the Department of Electrical and Computer Engineering, University of Wisconsin, Madison, WI 53706 USA (e-mail: jahns@engr.wisc.edu; shi-hong@cae.wisc.edu).

Digital Object Identifier 10.1109/TIA.2003.810654

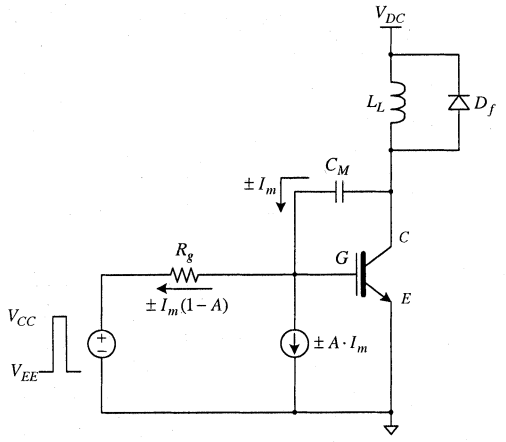


Fig. 1. Equivalent circuit for flexible dv/dt control topology.

Flexible dv/dt and di/dt control techniques are presented in this paper that have been developed to achieve the following two specific objectives: 1) independent control of the output terminal dv/dt and di/dt rates that are adjusted *electronically* over a wide range without the need to change passive components and 2) maximum compatibility with integrated circuit design techniques that will encourage their eventual implementation in power module configurations that include both the power switches and their integrated gate drives.

For dv/dt control, the output voltage dv/dt rate can be controlled by electronically adjusting the effective gate-to-drain capacitance (i.e., Miller capacitance) in order to dynamically control the gate charging current. For di/dt control, similar techniques are applied to electronically adjust the output current di/dt over a wide range using voltage feedback from a small inductor connected in series with the switch's source (emitter) terminal. Both of these techniques can be combined to provide flexible and independent control of the power device dv/dt and di/dt switching rates during both turn-on and turn-off events in hard-switching applications.

II. dv/dt Switching Rate Control Techniques

A. Descriptions of dv/dt Control Techniques

Fig. 1 shows the equivalent model for the flexible dv/dt control topology applied to the gating circuit for an IGBT. A small external capacitor C_M is used to sense the switch's collector (C) terminal voltage derivative dv/dt and to generate current

feedback to the gate (G) terminal for dv/dt control. The impact of gate-collector capacitance on reducing the dv/dt of three-terminal switching devices is a well-understood phenomenon known as the Miller effect [10].

If the physical capacitor value is fixed, its contribution to the gate current will not change for a given dv/dt. However, this new approach introduces a dependent current source at the gate node whose current is proportional to the value of the capacitor current I_m, achieving the same effect as changing the value of the external Miller capacitor C_M. In fact, the net effect of the control circuit can be interpreted as providing an electronically controlled Miller capacitance.

The net current at gate node contributed by the external Miller capacitor combined with the dependent source is $\pm I_m(1-A)$. Adjusting the value of A over a range including positive and negative polarities makes it possible to electronically increase *or decrease* the effective value of the total Miller capacitance. Note that if the gain A is set to one, the net contribution to the gate current is zero, canceling the effects of the external Miller capacitor C_M.

This approach offers several attractive features for dv/dt control. First, the control circuit activates only when the drain voltage is changing. Second, the control action begins as soon as the collector voltage switching transient begins without additional detection or timing circuits. Third, the ability to electronically control the Miller capacitance makes adjustments of the dv/dt rates particularly easy to accomplish. As a result, this technique offers the basis for flexible dv/dt control that is suitable for fast switching devices without affecting their on-state performance.

The turn-on and turn-off collector voltage dv/dt values delivered by the Fig. 1 control circuit can be expressed as follows [10]:

$$\frac{dV_{ce,\text{off}}}{dt} = \frac{V_T + \frac{I_L}{g_m} - V_{EE}}{R_g \cdot (C_{\text{gc}} + [1-A] \cdot C_M)} \tag{1}$$

$$\frac{dV_{ce,\text{on}}}{dt} = \frac{V_T + \frac{I_L}{g_m} - V_{CC}}{R_g \cdot (C_{\text{gc}} + [1-A] \cdot C_M)} \tag{2}$$

where

V_T gate threshold voltage (V);
g_m device transconductance (A/V);
I_L load inductor current (A);
C_{gc} device gate-collector capacitance (F).

In (1) and (2), the $R_g \cdot (1-A) \cdot C_M$ term in the denominator represents the effect of the new control circuit, showing how the dv/dt rate can be controlled by adjusting the value of gain A. The value of dv/dt can be progressively lowered by reducing the gain A, including negative values of A that amplify the effects of the external capacitor C_M. At the other extreme, the value of A can be greater than 1, causing dv/dt to *exceed* its nominal value when $C_M = 0$. This condition corresponds to overcompensation of the external Miller capacitance if very fast switching is desired. However, care must be taken in this regime since the dynamic stability of the switching circuit can suffer when C_{gc} is overcompensated. The dv/dt control range can be expanded for a given range of A values by increasing the value of capacitor C_M.

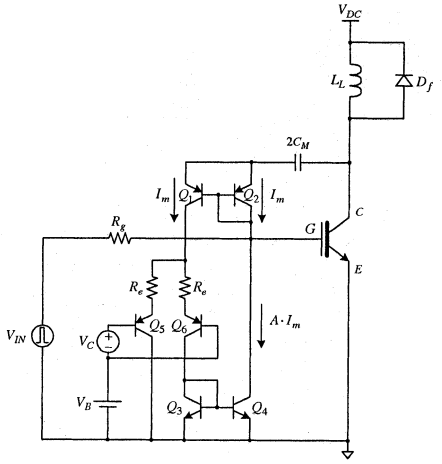


Fig. 2. Circuit implementation of turn-off dv/dt control circuit.

Fig. 2 shows one of the possible implementations of the flexible turn-off dv/dt control circuit. All of the transistors in this control circuit operate in their active regions for fast response. The transistors in the current mirror [11] consisting of Q_1 and Q_2 split the total current in the external Miller capacitance ($= 2C_M$) into halves, each equal to I_m. The collector current of $Q_1 (= I_m)$ is then delivered to the emitter-coupled pair consisting of Q_5, Q_6, and R_e. The control voltage V_c applied between the gates of Q_5 and Q_6 determines the fraction of this current, $A \cdot I_m$, $(0 < A < 1)$ that flows through Q_6 and is delivered to Q_3.

The action of current mirror of Q_3 and Q_4 repeats the current in Q_6 into Q_4 so that the Q_4 current ($= A \cdot I_m$) controls the net gate current contribution, $(1-A) \cdot I_m$. The value of the current fraction A is a linear function of V_c. As the amplitude of the injected current at the gate node $(1-A) \cdot I_m$ increases by reducing the value of A, dv/dt monotonically decreases as indicated by (1). Note that this particular circuit implementation does not permit $A > 1$, preventing overcompensation of the external Miller capacitance.

The same approach described above can also be applied to control the turn-on dv/dt. Since the direction of the Miller capacitor current is opposite during turn-on compared to turn-off, the turn-on dv/dt control circuit (Fig. 3) is essentially an inverted version of the Fig. 2 turn-off control circuit. Comparing these two figures, it can be noted that the positions of the n-p-n and p-n-p transistors exchange places in the two control circuits.

B. Simulation of dv/dt Control With 70 A IGBT

Simulation of the turn-on and turn-off dv/dt control circuits was conducted using PSPICE models of a 1200-V 70-A IGBT (IXSK35N120AU from IXYS). All simulation results in this paper have been carried out using PSPICE.

Predicted dv/dt switching waveforms for the 1200-V 70-A IGBT operating in a hard-switching circuit at 600 V and 70 A with an inductive load (Fig. 1) are shown in Fig. 4. The predicted switching waveforms are well-behaved for all of the dv/dt command values. The turn-off dv/dt is varied over a range of approximately 5:1 from approximately 920 V/μs to 4870 V/μs by adjusting the value of control gain A using the adjustable

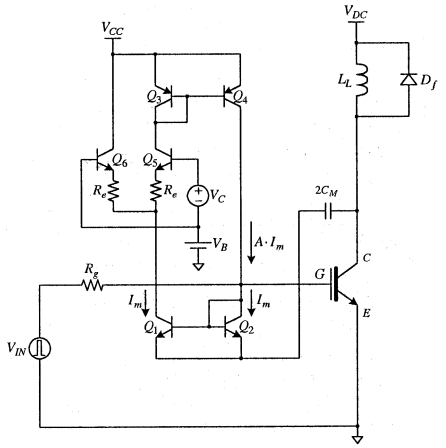


Fig. 3. Circuit implementation of turn-on dv/dt control circuit.

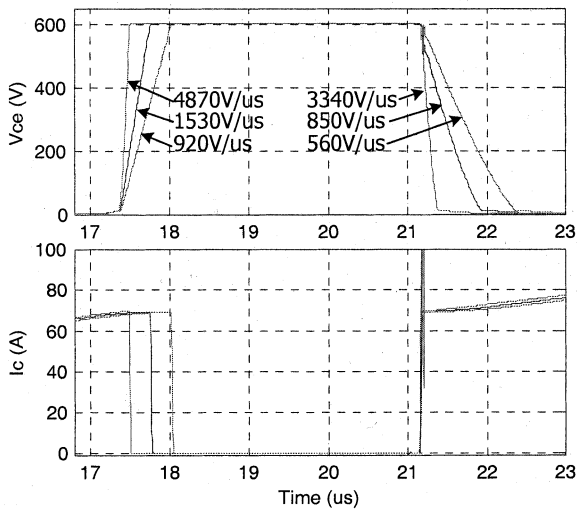


Fig. 4. Simulation results showing the collector voltage and current switching waveforms of a 1200-V 70-A IGBT (IXSK35N120AU) operating at 600 V, 70 A with the dv/dt control circuits at three different turn-on and turn-off dv/dt command settings.

voltage V_c in Figs. 3 and 4. (Note that a separate V_c voltage control is required for the turn-on and turn-off circuits.) The turn-on dv/dt is varied over a similarly wide range. Fig. 4 also shows that the current waveforms are unaffected by the operation of the dv/dt control circuit.

C. Experimental Results for dv/dt Control With 70-A IGBT

Experimental verification of the dv/dt control circuits has been carried out using the same 1200-V 70-A IGBT (IXSK35N120AU) that was used in the preceding simulations. Tests have been performed using the following parameters and operating conditions:

$$V_{\rm dc} = 600\ {\rm V} \quad I_C = 20\ {\rm A} \quad L_{\rm load} = 1\ {\rm mH}$$
$$V_{cc} = 16\ {\rm V} \quad V_{EE} = -5\ {\rm V} \quad R_g = 40\ \Omega.$$

Figs. 5 and 6 provide measured voltage waveforms for the turn-off and turn-on dv/dt control circuits, respectively, with a 1.5-nF external Miller capacitor ($2C_M$ in Figs. 2 and 3). For both of these cases, dv/dt is demonstrated to vary over a range

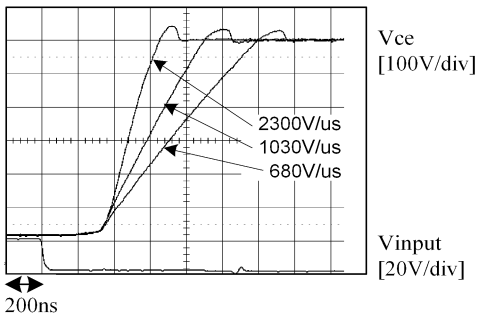


Fig. 5. Experimental test results for turn-off dv/dt control of a 1200-V 70-A IGBT operating at 600 V, 16 A at three different dv/dt command settings.

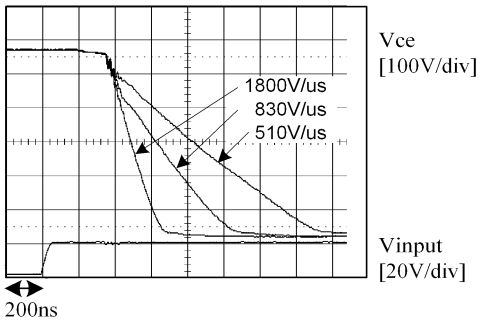


Fig. 6. Experimental test results for turn-on dv/dt control of a 1200-V 70-A IGBT operating at 600 V, 16 A at three different dv/dt command settings.

exceeding 3:1. The breadth of the dv/dt control range is influenced by the values of the external Miller capacitor and gate resistor R_g, consistent with the expression for dv/dt in (1).

The voltage waveforms in Figs. 5 and 6 and generally well-behaved for all of the tested conditions. Minor differences between the simulated and measured voltage waveforms in Figs. 4–6 can be attributed to the fact that the PSPICE simulation does not include all of the parasitic components such as extra inductance in the collector circuit that causes the voltage overshoot that is apparent in Fig. 5. Similarly, the high-frequency ripple that appears at the beginning of the voltage turn-on switching waveforms in Fig. 6 can be associated with the reverse recovery transient of the inductor's freewheeling diode in Fig. 1.

III. di/dt Switching Rate Control Techniques

A. Technique Description

Flexible control of the transistor di/dt during hard switching can be achieved by applying a dual version of the Miller capacitance used to control dv/dt. Fig. 7 shows the equivalent model for the flexible di/dt control topology. The small external inductance L_s connected in series with the switch emitter is used to sense the di/dt value and generate feedback voltage for the control circuit. The value of this inductance can be chosen to be sufficiently small that it has negligible effect on the dominant time constant of the gate drive circuit.

Using the same conceptual approach as in the dv/dt equivalent circuit of Fig. 1, the measured di/dt is used to control a dependent current source that extracts current I_f from the switch's gate node. The value of this current is $\pm B \cdot V_{L_s}$, where $V_{L_s} = L_s\ di/dt$ and B is an adjustable gain analogous to A in

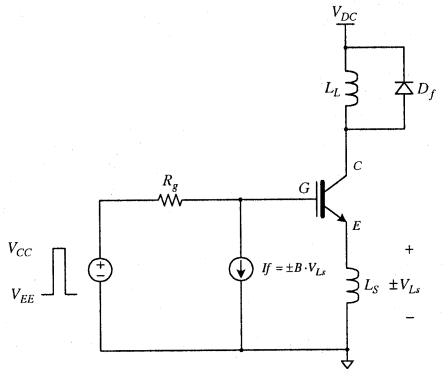


Fig. 7. Equivalent circuit for flexible di/dt control topology.

the dv/dt control circuit. Changing B makes it possible to electronically adjust the value of di/dt, providing the same effect as changing the value of the external inductance L_s.

This di/dt control circuit offers some of the same fundamental advantages as the dv/dt control circuit introduced above, responding immediately to switch turn-on and turn-off transients without any additional detection or timing circuits. It should be noted that this di/dt control circuit responds to changes in transistor current regardless of whether they are initiated internally by a change in the switch conduction state or externally by a transient in the attached load. However, the value of L_s is chosen to be sufficiently small that the di/dt control circuit will not interfere with the gate circuit's on-state operation during normal load variations.

If B is set to zero, the effect of the series emitter inductance L_s acting alone is to reduce the di/dt switching rates, similar to the impact of Miller capacitor C_M on the dv/dt rates. Increasing the value of feedback current gain B above zero amplifies the effect of the inductance so that the di/dt rate decreases during both turn-on and turn-off.

The switch circuit in Fig. 7 can be modeled as a third-order system due to the two internal device capacitors (C_{gc} and C_{ge}) and inductor (L_s). However, introduction of realistic device parameters has shown that the system can be approximated very accurately as a simplified first-order system. The resulting closed-form equations for the turn-off and turn-on di/dt during switching events are

$$\left.\frac{I_{d,\text{off}}}{dt}\right|_{t=0} = \frac{g_m\left[V_{EE} - \left(V_T + \frac{I_L}{g_m}\right)\right]}{R_g(C_{gc}+C_{ge}) + (1 + B \cdot R_g) g_m L_s} \quad (3)$$

$$\left.\frac{I_{d,\text{on}}}{dt}\right|_{t=0} = \frac{g_m(V_{CC} - V_T)}{R_g(C_{gc}+C_{ge}) + (1 + B \cdot R_g) g_m L_s} \quad (4)$$

where all of the variables have been previously defined.

Equations (3) and (4) express di/dt as a function of the circuit parameters and the dependent current gain B that is determined by the control voltage V_c. The denominator term $(1 + B \cdot R_g) g_m L_s$ captures the impact of the series emitter inductance L_s and the control circuit.

Fig. 8 shows a candidate implementation of the flexible turn-on di/dt control circuit. As in the dv/dt control circuit, all of the transistors in this di/dt control circuit also operate in their active regions. Resistor R_s and transistor Q_4 (diode-connected) convert the inductor voltage into a proportional current I_s and the transistor current mirror consisting of Q_3 and Q_4 repeats this sensing current in Q_3. The emitter-coupled pair circuit consisted of Q_1 and Q_2 splits I_s into two parts whose relative values depend on the control voltage, V_c. The unbalanced current mirror consisting of Q_5, Q_6, R_5, and R_6 amplifies the current in Q_1 so that a resulting feedback current I_f is subtracted from the nominal gate current delivered through R_g.

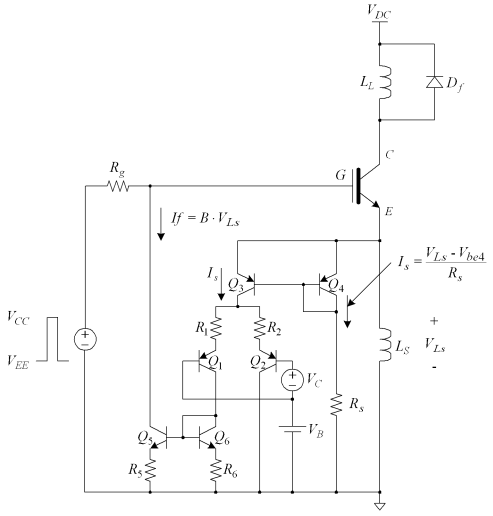


Fig. 8. Turn-on di/dt control circuit implementation.

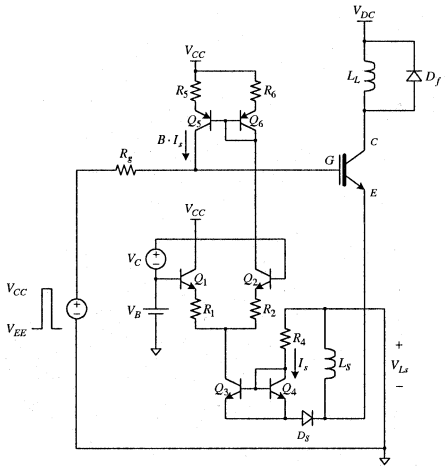


Fig. 9. Implementation of turn-off di/dt control circuit.

Since I_f in this circuit implementation acts to reduce the gate voltage during turn-on events, the output current di/dt is decreased compared to its value without this control circuit. In a manner that is directly analogous to the dv/dt control technique described above, V_c electronically adjusts the effective value of the series inductor L_s in order to control the di/dt value during switch turn-on.

Just as in the case of dv/dt control, the turn-on di/dt control technique can also be applied to controlling the turn-off di/dt. The turn-off di/dt control circuit is readily derived as an inverted version of the turn-on di/dt control circuit as shown in Fig. 9. Diode D_S is used to prevent reverse-polarity voltages

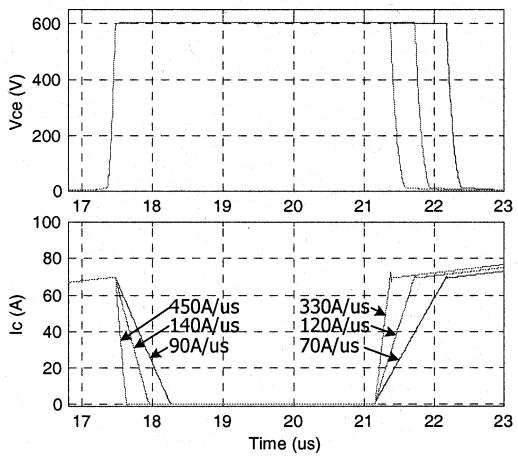


Fig. 10. Simulation results showing the collector voltage and current switching waveforms of a 1200-V 70-A IGBT (IXSK35N120AU) operating at 600 V, 70 A with the di/dt control circuits at three different turn-on and turn-off di/dt command levels.

from being applied to Q_3 and Q_4 because of the low breakdown voltage of the n-p-n transistor.

B. Simulation of di/dt Control With 70-A Device

Fig. 10 shows predicted hard-switching operation using the di/dt control circuitry for the same 1200-V 70-A IGBT and operating conditions (600 V, 70 A) as used earlier for the dv/dt simulations. A small 50-nH inductor is introduced in series with the switch's emitter for L_s. The value of this external inductor value is important in determining the di/dt controllability range. The external inductor value L_s and the maximum value of gain B are selected to demonstrate a 5:1 di/dt control range for both turn-on and turn-off. Both the turn-on and turn-off control circuits are present and traces are overlaid for three values of control voltage V_c in both directions. The upper limit on this *di/d*t range is determined by the inductor acting alone with gain $B = 0$.

C. Experimental Results of di/dt Control With 70-A Device

The basic IGBT test circuit used for the di/dt control investigation is the same as that used earlier for dv/dt control except that an external inductor L_s appears in the power circuit instead of the Miller capacitor C_M. The power device used in these tests is the same 1200-V 70-A IGBT (IXSK35N120AU) that was used in the preceding simulations and the test conditions are similar as well

$$V_{\rm dc} = 600\ {\rm V} \quad I_{ds} = 20\ {\rm A} \quad L_{\rm load} = 1\ {\rm mH}$$
$$V_{cc} = 16\ {\rm V} \quad V_{EE} = -5\ {\rm V} \quad R_g = 40\ \Omega.$$

Figs. 11 and 12 show experimental results for the turn-on and turn-off di/dt control circuits with an 80-nH external inductor. For the turn-on case, the value of di/dt varies from 16 A/μs to 60 A/μs, while for the turn-off case, it varies from 26 A/μs to 80 A/μs. Similar to the dv/dt circuits discussed earlier, the range of di/dt values demonstrated in these waveforms exceeds 3:1 for both turn-on and turn-off. A wider range of di/dt variation can be obtained by using a larger value of external series inductor consistent with the di/dt expressions in (3) and (4).

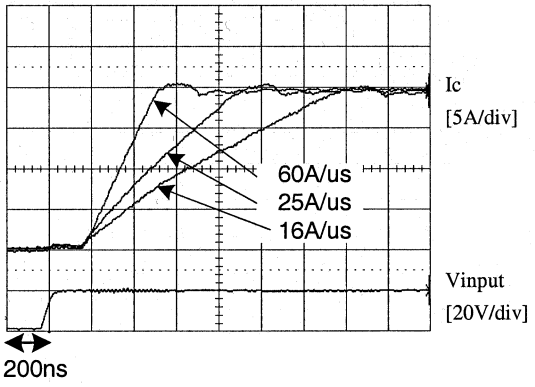


Fig. 11. Experimental test results for turn-on di/dt control of a 1200-V 70-A IGBT operating at 600 V, 20 A at three different di/dt command levels.

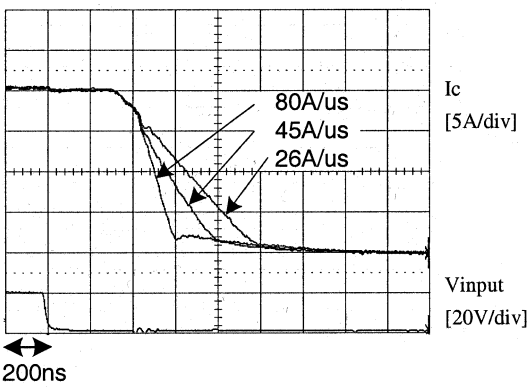


Fig. 12. Experimental test results for turn-off di/dt control of a 1200-V 70-A IGBT operating at 600 V, 20 A at three different di/dt command levels.

The current waveforms are well behaved for all of the test conditions appearing in Figs. 11 and 12. Here again, parasitic elements not included in the simulation model account for residual differences between the predicted and measured waveforms. The slight dip in current appearing near the beginning of the turn-off di/dt transient waveforms is coincident with the end of the turn-off voltage transient when the collector voltage is suddenly clamped by the inductor's freewheeling diode. The familiar tail current characteristic of the IGBT [10] is apparent near the end of the turn-off di/dt transient waveforms, particularly for the fastest di/dt setting.

IV. Performance Evaluations

Although the basic feasibility of the flexible turn-on and turn-off techniques was established in the preceding sections, there are several other performance aspects of these techniques that deserve attention. The simulation model has been exercised to address several of these issues. First, the interactions between the dv/dt and di/dt control circuits have been investigated to determine the extent of the coupling between them. Second, the sensitivity of the di/dt and dv/dt values to device operating current levels is explored. Finally, the range of usefulness of these techniques is explored by adapting the gate circuits to control a low-current MOSFET as well as a high-current IGBT module.

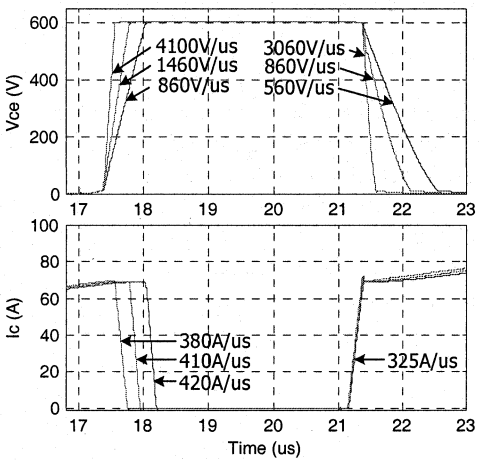


Fig. 13. Simulated voltage and current waveforms for 1200-V 70-A IGBT operating at 600 V, 70 A showing near independence of di/dt values for wide range of commanded dv/dt levels.

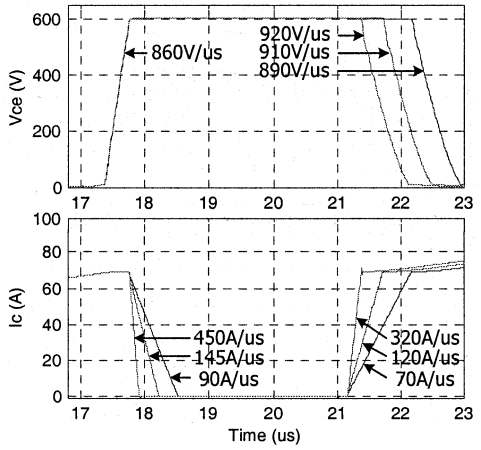


Fig. 14. Simulated voltage and current waveforms for 1200-V 70-A IGBT operating at 600 V, 70 A showing near independence of dv/dt values for wide range of commanded di/dt levels.

All of the simulations in this section have been performed with both the dv/dt and di/dt control circuits simultaneously present in the model. This was done so that any potential interactions between the dv/dt and di/dt control circuit under different conditions could be conveniently identified.

A. Control Circuits Interactions

The interactions of the dv/dt and di/dt control circuits have been investigated by including them both in the same simulation model together with the 1200-V 70-A IGBT. Fig. 13 shows the effect of dv/dt control on the switch current waveforms, demonstrating that the resulting di/dt values are almost completely independent of the adjusted dv/dt values. For the inductive load condition, the switch voltage only begins to fall after the current transient is completed during turn-on. Similarly, the switch current starts to drop only after the voltage transition is completed during turn-off. The sequential nature of these transitions minimizes potential interactions between the dv/dt and di/dt control circuits. This same independence is apparent in the switch voltage waveforms of Fig. 14 when the current di/dt is adjusted over a wide range.

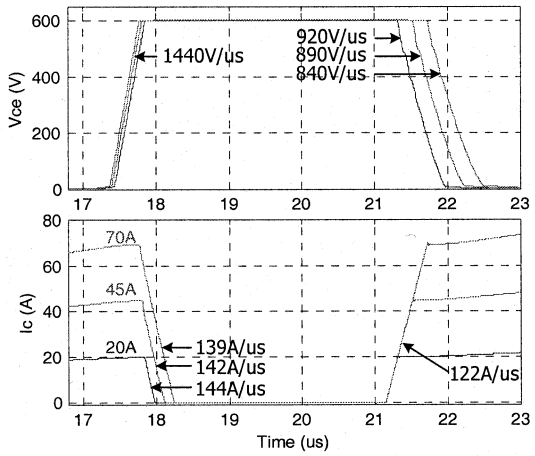


Fig. 15. Effect of current amplitude on control circuit operation showing near independence of dv/dt and di/dt value for wide current amplitude variations.

B. Effect on Current Amplitude on dv/dt and di/dt Control

The sensitivity of the dv/dt and di/dt values to current amplitude has been investigated by performing simulations with the 70-A IGBT at three different current levels −20, 45, and 70 A—with fixed dv/dt and di/dt command levels. As shown in Fig. 15, neither the dv/dt or di/dt rates exhibit any significant change for turn-on or turn-off conditions as the current amplitude is varied over this wide range.

C. Effectiveness for Lower and Higher Current Devices

Simulations have also been carried out for two additional insulated gate power devices to determine the effectiveness of the dv/dt and di/dt control techniques for devices with widely varying current ratings. More specifically, the simulation study included a 1000-V 12-A MOSFET (IXFH12N100 from IXYS) and a 1200-V 560-A IGBT module. Parameters for the 1200-V 560-A IGBT were derived by paralleling eight of the 1200-V 70-A IXSK35N120AU devices in the simulation since PSPICE model parameters for a high-current IGBT module ($>$500 A) were not conveniently available.

Figs. 16 and 17 show the predicted waveforms for the 1000-V 12-A MOSFET operating at 600 V and 12 A during adjustment of dv/dt and di/dt, respectively, with both control circuits present. The demonstrated control range is approximately 5:1 for both dv/dt and di/dt, and the interaction between the two control circuits is again very low.

Comparable simulation results for the 1200-V 560-A IGBT modules are shown in Figs. 18 and 19 for operation at 600 V and 560 A with both control circuits present. These waveforms also demonstrate a 5:1 control range for dv/dt and di/dt during both turn-on and turn-off, and low coupling effects between the control circuits.

Taken together, these results suggest that the flexible dv/dt and di/dt control techniques presented in this paper scale well over a wide range of power device current ratings.

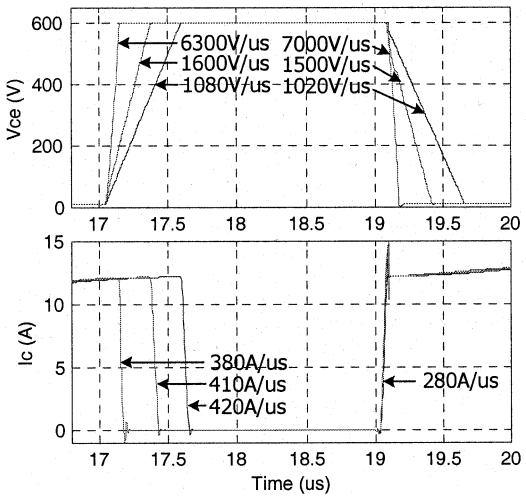


Fig. 16. Simulated voltage and current waveforms for 1000-V 12-A MOSFET with combined control circuits operating at 600 V, 12 A for several values of commanded dv/dt.

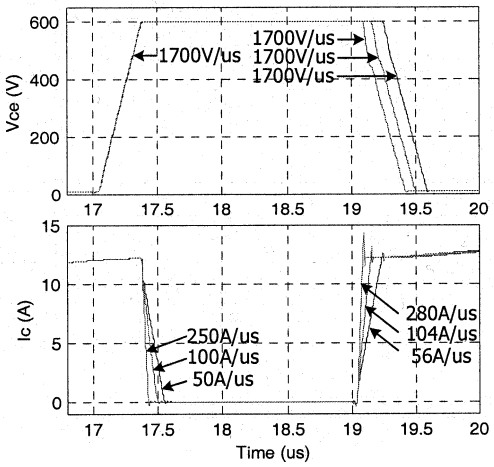


Fig. 17. Simulated voltage and current waveforms for 1000-V 12-A MOSFET with combined control circuits operating at 600 V, 12 A for several values of commanded di/dt.

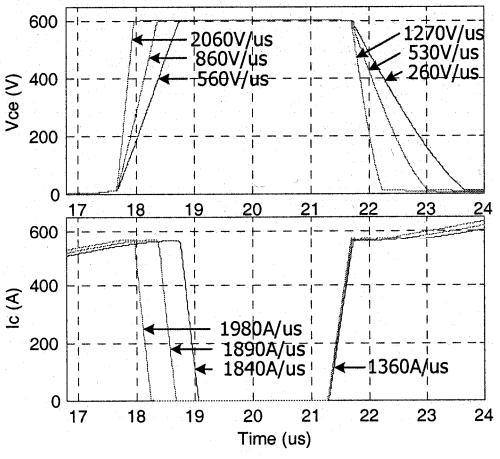


Fig. 18. Simulated voltage and current waveforms for 1200-V 560-A IGBT with combined control circuits operating at 600 V, 560 A for several values of commanded dv/dt.

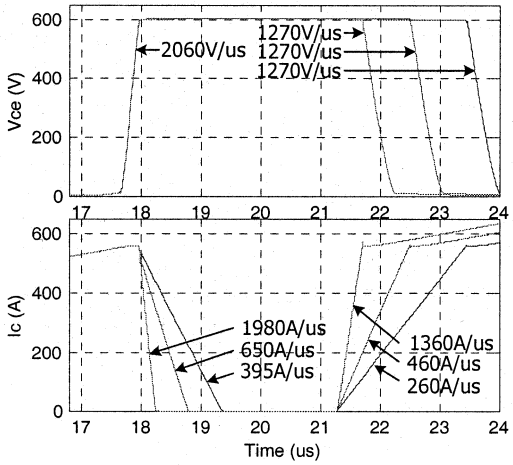


Fig. 19. Simulated voltage and current waveforms for 1200-V 560-A IGBT with combined control circuits operating at 600 V, 560 A for several values of commanded di/dt.

V. Conclusion

This paper has presented flexible dv/dt and di/dt control techniques for hard-switched inverters that make it possible to conveniently adjust the switching rates during both turn-on and turn-off. These techniques have demonstrated the following combination of attractive features:

- electronic control of the dv/dt and di/dt rates over a range of at least 5:1;
- well-behaved voltage and current waveforms for all investigated operating conditions with inductive loads;
- suitability for use with both IGBTs and power MOSFETs over a wide range of current ratings extending from at least 12 to 560 A;
- no indication of harmful interactions between the dv/dt and di/dt control circuits when both are present;
- suitability of control techniques for implementation in integrated circuits, requiring only a small external capacitor and inductor for dv/dt control and di/dt control, respectively.

All of the results presented in this paper refer to circuits in which the power device's emitter (source) is grounded. However, the same techniques can be adopted for power circuit topologies in which the power device collector (drain) is connected to a fixed potential. Examples include classic dc/dc buck converters and high-side switches in phase-leg inverter circuits. Although the basic operating principles are unchanged, it is necessary in these cases to protect the gate drives from undesired parasitic effects on drive circuit operation caused by large common-mode voltage swings.

It is well known that the benefits of reduced dv/dt and di/dt in the areas of reduced EMI and improved current sharing must be balanced against attendant increases in device switching losses. Quantitative evaluation of such tradeoffs is beyond the scope of this paper and a subject for future investigation.

Both simulation and experimental results have been presented to confirm the operating characteristics of the dv/dt and di/dt control techniques. Work is continuing to explore how these

techniques can be best utilized in future generations of gate drive circuits.

ACKNOWLEDGMENT

The authors thank the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC) for use of its laboratory facilities in carrying out this investigation.

REFERENCES

[1] V. John, B.-S. Suh, and T. A. Lipo, "High perfomance active gate drive for high power IGBT's," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Oct. 1998, pp. 1519–1529.

[2] B. Weis and M. Bruckmann, "A new gate driver circuit for improved turn-off characteristics of high current IGBT modules," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Oct. 1998, pp. 1073–77.

[3] M. Kimata, S. Chikai, T. Tanaka, and K. Ishii, "High performance gate drive circuit of high voltage IPM's (HVIPM's)," in *Proc. IEEE PESC'98*, June 1998, pp. 1196–1200.

[4] H.-G. Lee, Y.-H. Lee, B.-S. Suh, and D.-S. Hyun, "An improved gate control scheme for snubberless operation of high power IGBT's," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Oct. 1997, pp. 975–982.

[5] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo, and M. Melito, "A new adaptive technique for high current gate controlled devices," in *Proc. IEEE APEC'94*, Feb. 1994, pp. 480–486.

[6] P. R. Palmer and A. N. Githiari, "The series connection of IGBT's with optimized voltage sharing in the switching transient," in *Proc. IEEE PESC'95*, June 1995, pp. 44–49.

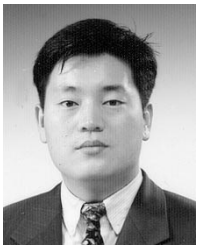
[7] C. Gerster, P. Hofer, and N. Karrer, "Gate-control strategies for snubberless operation of series connected IGBT's," in *Proc. IEEE PESC'96*, June 1996, pp. 1739–42.

[8] S. Igarashi *et al.*, "An active control gate drive circuit for IGBT's to realize low-noise and snubberless system," in *Proc. IEEE ISPSD'97*, 1997, pp. 69–72.

[9] A. Galluzzo, G. Belverde, M. Melito, S. Musumeci, and A. Raciti, "Snubberless balancement of series connected insulated gate devices by a novel gate control strategy," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Oct. 1997, pp. 968–974.

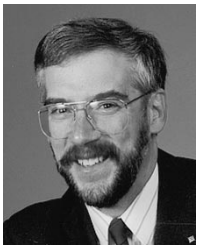
[10] B. J. Baliga, *Power Semiconductor Devices*. Boston, MA: PWS, 1995.

[11] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 1993.



Shihong Park (S'01) was born in Pusan, Korea. He received the B.S. degree in electrical engineering from Yonsei University, Seoul, Korea, in 1988. He is currently working toward the Ph.D. degree at the University of Wisconsin, Madison.

From 1988 to 1998, he was with Samsung Electronics, Puchon, Korea, as a Senior Power IC Design Engineer. His main research interests are integrated power electronic modules (IPEMs), active gate drive topology, and power converter circuits.



Thomas M. Jahns (S'73–M'79–SM'91–F'93) received the S.B. and S.M. degrees in 1974 and the Ph.D. degree in 1978 from Massachusetts Institute of Technology, Cambridge, all in electrical engineering.

In 1998, he joined the faculty of the University of Wisconsin, Madison, as a Professor in the Department of Electrical and Computer Engineering, where he is also an Associate Director of the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC). Prior to joining the University of Wisconsin, he was with GE Corporate Research and Development, Schenectady, NY, for 15 years, where he pursued new power electronics and motor drive technology in a variety of research and management positions. His research interests include permanent-magnet synchronous machines for a variety of applications ranging from high-performance machine tools to low-cost appliance drives. During 1996–1998, he conducted a research sabbatical at Massachusetts Institute of Technology, where he directed research activities in the area of advanced automotive electrical systems and accessories as co-director of an industry-sponsored automotive consortium.

Dr. Jahns was awarded the William E. Newell Award by the IEEE Power Electronics Society (PELS) in 1999. He has been recognized as a Distinguished Lecturer by the IEEE Industry Applications Society (IAS) during 1994–1995 and by PELS during 1998–2000. He has served as President of PELS (1995–1996) and as a Member of the IAS Executive Board between 1992–2001. He was elected Director/Delegate of IEEE Division II, serving during 2002–2003 on the IEEE Board of Directors.