

**REALIZATION OF A MULTILEVEL,
BIDIRECTIONAL BUCK-DERIVED DC-
DC CONVERTER**

by

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Abstract

This thesis centers on the realization of a multilevel, bidirectional buck-derived DC-DC converter whose typology is capable of extremely large transformation ratios. The emphasis of this work is on the mode of operation in which the power flow is from a high voltage source to a low voltage load. The converter concept is explained in detail and a modulation scheme with considerations for practical implementation is discussed. The design of a prototype four-level converter is detailed and major loss mechanisms of the converter are described. Both directions of power flow are shown through simulation. Prototype hardware results are presented to demonstrate proof of the concept and provide validation for theoretical and simulation results.

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Table of Contents

Abstract	i
Acknowledgements	ii
List of figures	v
List of tables.....	x
Chapter 1 Introduction	1
Chapter 2 Converter Concept.....	3
2.1 Background	3
2.2 Converter typology	6
2.3 Converter implementation	7
2.4 Modulation scheme.....	12
Chapter 3 Prototype converter design.....	23
3.1 Design specifications and component selection	24
3.2 Gate signal generation.....	28
3.3 PCB design.....	29
Chapter 4 Converter loss mechanisms	36
4.1 MOSFET switching losses.....	36
4.2 Power MOSFET and diode conduction losses.....	41
Chapter 5 Simulation Results.....	43

5.1 Simulation model	43
5.2 Ideal circuit simulations	45
5.2.1 Bucking operation	45
5.2.2 Boosting operation	54
5.3 Non-ideal simulations	59
Chapter 6 Experimental results and analysis	63
6.1 Hardware versus simulation results	63
6.2 Other input voltages and load conditions	66
6.3 Imbalance of divider capacitor voltages	68
Chapter 7 Conclusion	77
References	79
Appendix A Simplified conduction loss equations	81
Appendix B Simulation Details	85

List of figures

Figure 2-1 Three-level buck converter from [5]	3
Figure 2-2 Three-level buck converter waveforms.....	5
Figure 2-3 Bidirectional version of the three-level buck converter from [5] realized using (a) MOSFETs and (b) ideal single pole double throw (SPDT) switches	6
Figure 2-4 SPDT realized (a) four-level and (b) five-level converters [4]	7
Figure 2-5 Conduction states the four-level SPDT converter.....	8
Figure 2-6 Plot of V_x for a four-level converter	9
Figure 2-7 Four-level converter transformation ratio vs. duty cycle	10
Figure 2-8 Schematic of a four-level converter with N-channel MOSFETs and antiparallel body diodes	13
Figure 2-9 Conduction states of four-level converter.....	14
Figure 2-10 State diagram based on conduction states	15
Figure 2-11 Excessive switch voltage stress being applied to SW2L	16
Figure 2-12 Excessive switch voltage stress being applied in to SW2H (c) during deadtime between (a) conduction state 5 and (b) conduction state 6	18
Figure 2-13 Desired maximum switch voltage stress during deadtime between conduction state 5 and conduction state 6	19
Figure 2-14 Deadtime state for a four-level converter in (b) bucking operation and (c) boosting operation for the transition state between (a) conduction state 1 and (d) conduction state 2	20

Figure 2-15 Modulation scheme state diagram including switch transitions and deadtime for bucking operation.....	21
Figure 3-1 Schematic of a four-level converter with MOSFETs.....	23
Figure 3-2 FDP26N40 reverse drain current versus body diode forward voltage [7]	26
Figure 3-3 Stellaris LM3S1968 Evaluation Board [10].....	28
Figure 3-4 Hardware of the prototype four-level converter.....	30
Figure 3-5 Top sheet schematic showing interconnections of daughter sheets	31
Figure 3-6 uC daughter sheet containing the microcontroller header and digital isolators ...	32
Figure 3-7 Power_supplies daughter sheet containing the microcontroller power supply and five isolated 12 V and 5 V supplies for each half-bridge	32
Figure 3-8 SW1 and SW2 daughter sheet containing the gate drive circuitry and switches for SW1 and SW2 as well as the low voltage filter.....	33
Figure 3-9 SW3 and SW4 daughter sheet containing the gate drive circuitry and switches for SW3 and SW4 as well as the divider capacitors C_1 and C_2	33
Figure 3-10 SW5 daughter sheet containing the gate drive circuitry and switches for SW5 as well as the divider capacitor C_3	34
Figure 3-11 Copper layers on the (a) top and (b) bottom of the PCB	35
Figure 4-1 Conduction states 1 and 2 and then transition state between them	37
Figure 4-2 Remaining conduction and transition states.....	39
Figure 4-3 Examples of parallel MOSFET/diode paths	42
Figure 5-1 Four-level converter PLECS circuit model of the converter in (a) bucking operation and (b) boosting operation	44

Figure 5-2 PLECS model used for ideal simulation of the four-level converter in bucking operation	45
Figure 5-3 Simulation gate signals for 75% duty cycle.....	46
Figure 5-4 Simulation waveforms for the ideal four-level converter in bucking operation for $d=75%$, $V_{HV} = 225$ V and $R_{Load} = 10\Omega$	47
Figure 5-5 Simulation waveforms for the ideal four-level converter in bucking operation for $d=50%$, $V_{HV} = 225$ V and $R_{Load} = 10\Omega$	49
Figure 5-6 Simulation waveforms for the ideal four-level converter in bucking operation for $d=25%$, $V_{HV} = 225$ V and $R_{Load} = 10\Omega$	49
Figure 5-7 Simulation gate signals for 75% duty cycle with a $1.25\mu s$ deadtime.....	50
Figure 5-8 SW5H and SW5L gate signal, switch current and switch voltage.....	51
Figure 5-9 SW1H and SW1L gate signal, switch current and switch voltage.....	52
Figure 5-10 SW2H and SW2L gate signal, switch current and switch voltage.....	53
Figure 5-11 SW3H and SW3L gate signal, switch current and switch voltage.....	53
Figure 5-12 SW4H and SW4L gate signal, switch current and switch voltage.....	54
Figure 5-13 PLECS model used for ideal simulation of the four-level converter in boosting operation	55
Figure 5-14 Simulation waveforms for the ideal four-level converter in boosting operation for $d=50%$, $V_{LV} = 24$ V and $R_{Load} = 250\Omega$	56
Figure 5-15 Simulation waveforms for the ideal four-level converter in boosting operation for $d=50%$, $V_{LV} = 24$ V and $R_{Load} = 250\Omega$	58

Figure 5-16 Simulation waveforms for the ideal four-level converter in boosting operation for $d = 25\%$, $V_{HV} = 24 \text{ V}$ and $R_{Load} = 250\Omega$	58
Figure 5-17 PLECS model used for non-ideal simulations of the four-level converter in bucking operation.....	60
Figure 5-18 Efficiency vs. duty cycle for the three simulation cases with a constant load of 10Ω	62
Figure 6-1 Transformation ratio versus duty cycle for 225 V input and 10Ω load	64
Figure 6-2 Hardware and simulated efficiency versus duty cycle for a 225 V input and 10Ω load.....	65
Figure 6-3 Hardware and simulated efficiency versus output power for a 225 V input and 10Ω load.....	65
Figure 6-4 Transformation ratio versus duty cycle for all input and load conditions.....	66
Figure 6-5 Efficiency versus duty cycle for all input and load conditions	67
Figure 6-6 Efficiency versus output power for all input and load conditions	68
Figure 6-7 Oscilloscope screen shots showing the inductor current (CH 1), and voltages of C_1 (CH 2), C_2 (CH 3) and C_3 (CH 4) for duty cycles of (a) 20%, (b) 50% and (c) 80%	69
Figure 6-8 Percent error of each capacitor voltage from the mean versus duty cycle for all tested input voltage and load conditions	71
Figure 6-9 Absolute value of the percent error from the mean of each capacitor voltage versus duty cycle for all tested input voltage and load conditions	72

Figure 6-10 Absolute value of the percent error from the mean of each capacitor voltage versus duty cycle for 225 V input, 10Ω load achieved with open loop balancing case as well as the nominal case	75
Figure A-1 Repeated conduction states 1 and 2.....	81
Figure A-2 Trapezoidal current waveform	82
Figure B-1 Ideal converter in bucking mode Simulink model	86
Figure B-2 “4-Level DC-DC converter” subsystem for the ideal simulation of the converter in bucking operation	87
Figure B-3 “Gate Signal Generation” subsystem for the ideal simulation of the converter in bucking operation.....	88
Figure B-4 “Conduction State Calculator” subsystem for the ideal simulation of the converter in bucking operation	89
Figure B-5 Ideal converter in boosting mode Simulink model.....	91
Figure B-6 “4-Level DC-DC converter” subsystem for the ideal boosting mode simulations	92
Figure B-7 “Gate Signal Generation” subsystem for the ideal boosting mode simulations ..	93
Figure B-8 “Conduction State Calculator” subsystem for the ideal boosting mode simulations	94
Figure B-9 Simulink model for the non-ideal simulations	97
Figure B-10 “4 Level DC-DC converter” subsystem for the non-ideal simulations	98

List of tables

Table 2-1 Three Level Converter Truth Table.....	4
Table 3-1 Design specifications of the prototype converter	24
Table 3-2 Bourns 1140-331K-RC inductor specifications [6].....	25
Table 3-3 FDP26N40 N-channel MOSFET specifications [7].....	25
Table 3-4 Specifications of the EEUEE2E101S capacitor used in the low voltage output filter.....	27
Table 3-5 Snubber components and component parameters	28
Table 4-1 Switch voltage and current for switching transitions	40
Table 5-1 Simulation parameters for ideal four-level converter in bucking operation.....	46
Table 5-2 Four-level converter bucking operation simulated results for $V_{HV}=225$ V and $R_{Load}=10\Omega$	50
Table 5-3 Simulation parameters for ideal four-level converter in boosting operation.....	55
Table 5-4 Four-level converter boosting operation simulated results for $V_{LV}=24$ V and $R_{Load}=250\Omega$	59
Table 5-5 Simulation parameters for non-ideal four-level converter in bucking operation ..	59
Table 5-6 Simulation results including MOSFET conduction, diode forward voltage and conduction losses, and snubber losses	60
Table 5-7 IRFB4115PbF N-channel MOSFET specifications [11].....	61
Table 5-8 Simulation results without RCD snubbers and with 150 V rated MOSFETs	62
Table 6-1 Hardware input and output data for 225 V input and 10 Ω load.....	64
Table 6-2 Capacitor voltage test data for 225 V input, 10 Ω load.....	70

Table 6-3 Capacitor voltage test data for 225 V input voltage and 10 Ω load in which open loop control of d_1 , d_2 and d_3 was implemented.....	73
Table 6-4 Voltage tranformation data for the open loop balancing test and the nominal case for a 225 V input and 10 Ω load	76

Chapter 1 Introduction

Many applications including energy sources of solar and fuel cells [1], industrial multilevel inverters [2], and wind farms [3] that use DC-DC converters with large transformation ratios are being increasingly developed for higher power levels. This thesis centers on a multilevel, bidirectional buck-derived DC-DC converter that is good candidate for non-isolated, large transformation ratio, and high power type applications.

The organization of this thesis is as follows. Chapter 2 details the converter concept by providing background information of the three-level converter in which the multilevel converter used in this thesis is based on and by showing how that converter typology can be extended to additional levels. The converter implementation of the converter is detailed and the equations for the transformation ratio and inductor current ripple are derived. A state machine based modulation scheme is also presented. Chapter 3 describes a prototype four-level converter that was developed. The design specifications, component selection, and gate signal generation are discussed. The completed PCB is displayed and the schematics are presented. Chapter 4 discusses the major loss mechanisms of the converter in bucking mode of operation including the MOSFET switching losses and the conduction losses of the power MOSFETs and diode. Chapter 5 presents the simulation results including the ideal simulation of the converter operating with power flow from the high voltage side source to a low voltage side load and from a low voltage side source to a high voltage side load. Simulation results of a model that accounts for the major loss mechanisms of the prototype hardware design are also shown and modifications for improvement to the converter efficiency are justified

through simulation. Chapter 6 discusses the prototype hardware testing results and makes comparisons to the simulation results. Results for a number of input voltage and load conditions are presented. The voltage imbalance of the high voltage side series capacitors that appeared throughout the hardware testing is revealed and results of an open loop duty cycle control to improve the imbalance is shown. Chapter 7 summarizes the work of this thesis.

Chapter 2 Converter Concept

This chapter outlines the concept of the multilevel, bidirectional converter. Section 2.1 describes the operation of the three-level converter that the multilevel converter in this thesis was derived from and the inherent advantages of the three-level converter over the traditional buck converter. Section 2.2 shows the extension of that converter to the multilevel, bidirectional converter. Section 2.3 details the converter implementation and derives the transformation ratio and inductor current ripple equations for an arbitrary number of level converter under the described control scheme. Section 2.4 demonstrates the implementation of the modulation scheme through a state machine.

2.1 Background

The multilevel, bidirectional converter used as a basis for this thesis was first conceptualized by my colleague Justin Reed in [4] and was derived from the three-level buck or boost converter presented in [5]. A schematic of the three-level buck converter is shown in Figure 2-1.

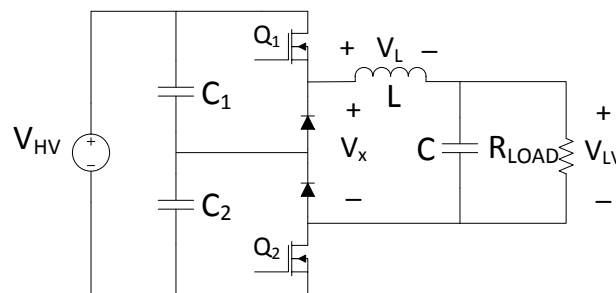


Figure 2-1 Three-level buck converter from [5]

The three-level buck converter operates very similar to the traditional buck converter with some distinct differences. The switches Q_1 and Q_2 in Figure 2-1 are used to apply a voltage to the left side of the output, shown by V_x in the diagram. The resulting voltage across the inductor is then $V_x - V_{LV}$. In contrast to the traditional buck converter, the three-level buck converter is capable of applying two additional voltages to the left side of the inductor, namely, V_{C1} and V_{C2} . The possible inductor voltages are shown in the converter's truth table in Table 2-1 assuming ideal switches.

Table 2-1 Three Level Converter Truth Table

Q_1	Q_2	V_L
Off	Off	$-V_{LV}$
Off	On	$V_{C2} - V_{LV}$
On	Off	$V_{C1} - V_{LV}$
On	On	$V_{HV} - V_{LV}$

If it is assumed C_1 and C_2 are of equal capacitance and the converter is modulated such that equal energy is sourced from each capacitor, the capacitors will equally divide the input voltage and each have a voltage of $\frac{V_{HV}}{2}$. The possible voltages at V_x are then 0 V, V_{HV} , and $\frac{V_{HV}}{2}$. Although three distinct voltages are possible at V_x , the control strategy suggested in [5] is to apply a two-level voltage. The switching scheme is illustrated in Figure 2-2.

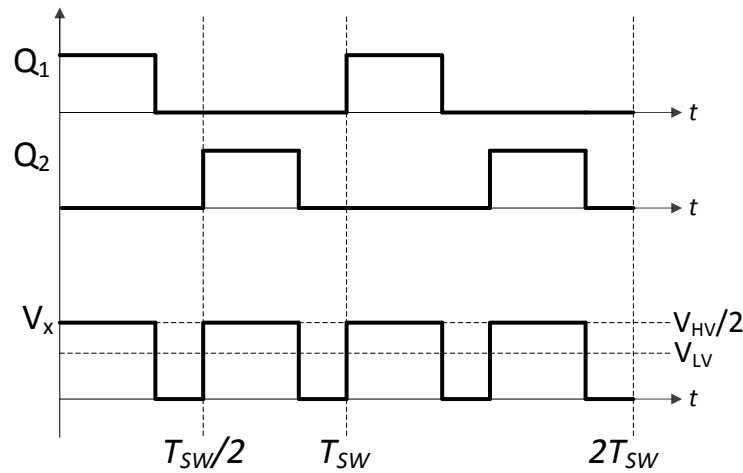


Figure 2-2 Three-level buck converter waveforms

During the first half of the switching period, Q_2 is off and Q_1 is on for a given duty cycle resulting in the applied voltage, V_x , being $\frac{V_{HV}}{2}$, and then Q_1 is turned off resulting in V_x being zero as the current free wheels through the ideal diodes. Similarly, in the second half of switching period, Q_1 is off and Q_2 is on for a given duty cycle and then turned off, resulting in the same voltages at V_x . Notice that V_x has a frequency of twice the switching frequency and that it is two-level. This is also true of the inductor voltage as the inductor sees a voltage of $V_x - V_{LV}$. The resulting advantage of this is that compared to the traditional buck converter with equal switching frequency, input voltage and output voltage, the three-level buck converter will need significantly smaller filter inductance to meet the same output ripple current specification. An additional advantage of the three-level converter is that the voltage ratings of the diodes and switches are halved as a maximum voltage of $\frac{V_{HV}}{2}$ is seen across the devices.

2.2 Converter typology

By replacing the diodes and switches of the converter in Figure 2-1 with switches containing antiparallel diodes as shown in Figure 2-3, a bidirectional version of the three-level converter is created [4].

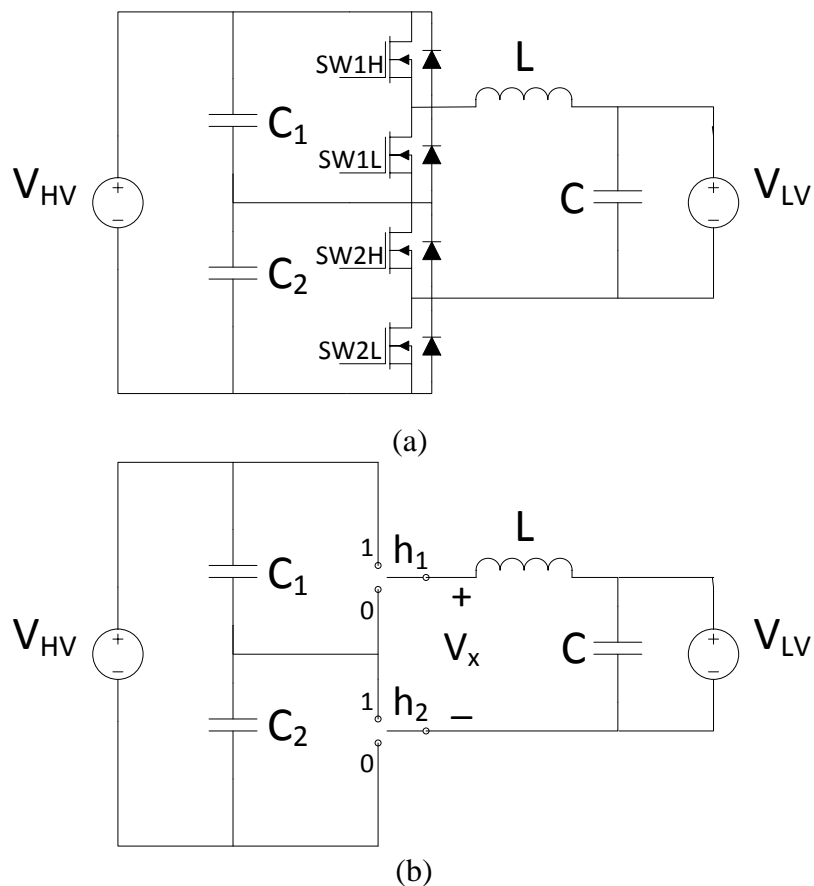


Figure 2-3 Bidirectional version of the three-level buck converter from [5] realized using (a) MOSFETs and (b) ideal single pole double throw (SPDT) switches

Next, that typology can be scaled to any number of levels to realize the multilevel, bidirectional converter first conceptualized in [4]. Examples of the four-level and five-level SPDT realized converter typologies are shown in Figure 2-4.

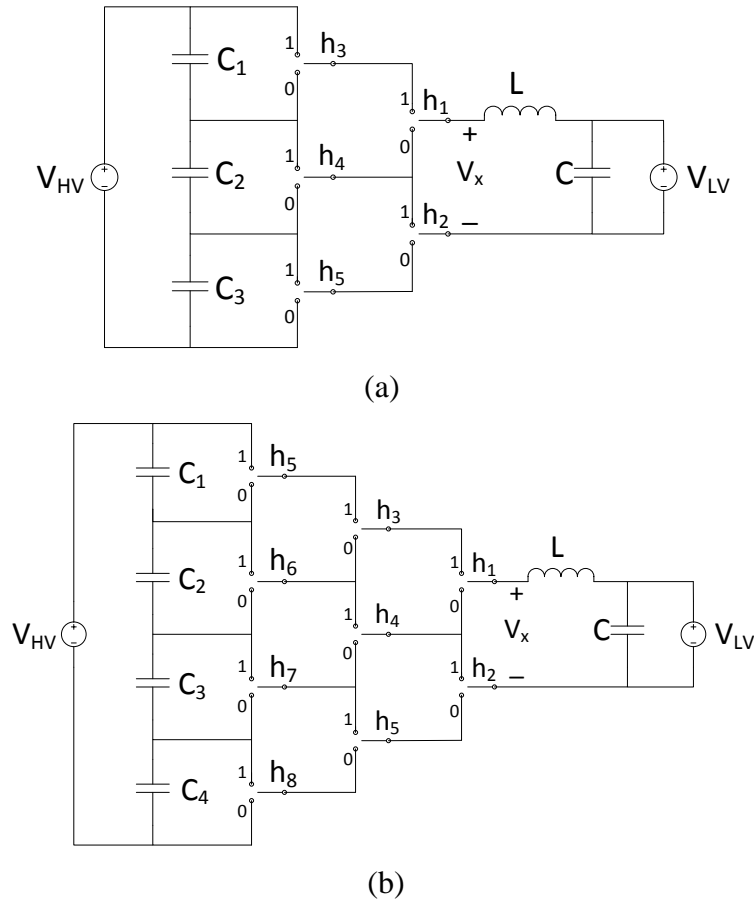


Figure 2-4 SPDT realized (a) four-level and (b) five-level converters [4]

Just as with the three-level buck converter, the high voltage is divided by a set of series capacitors and the switches are again used to select a voltage to apply across V_x .

2.3 Converter implementation

There are numerous ways in which the switches in this converter typology could be modulated but, as with the three-level converter, the proposed implementation of these multilevel converters is to apply a maximum of one capacitor's voltage at V_x . This implementation minimizes the filter inductance and the voltage rating of the switches as well

as allows for a constant switching frequency of all switching devices. The four-level converter will be used to illustrate the implementation and the conduction states of the SPDT realized four-level converter are shown in Figure 2-5. For this discussion, it will be assumed that the switches, capacitors and inductor are lossless and the C_1 , C_2 , and C_3 equally divide the voltage V_{HV} .

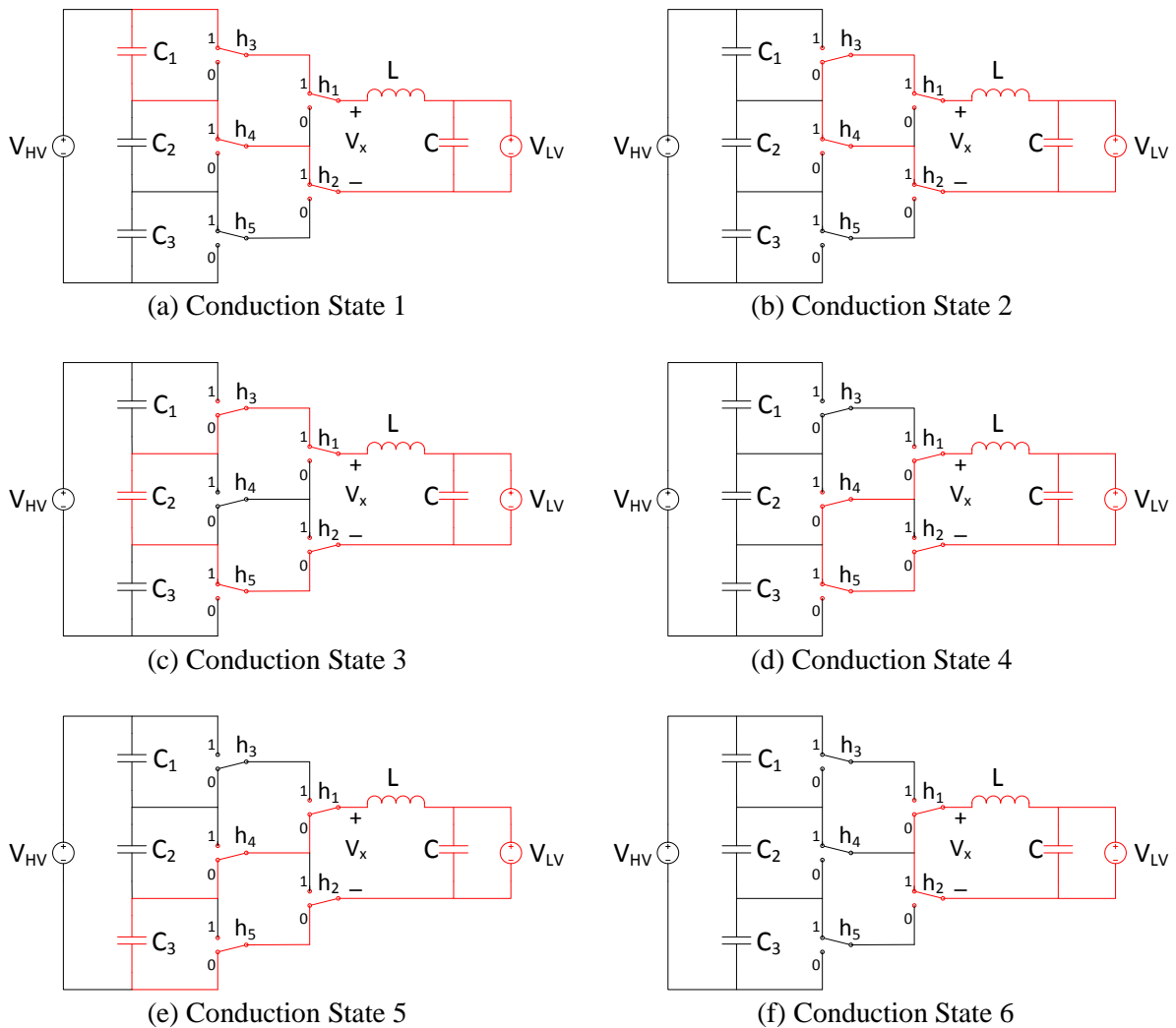


Figure 2-5 Conduction states the four-level SPDT converter

The red traces in the figure represent the inductor current carrying paths. The converter will go through all six conduction states from Figure 2-5 during one complete

switching cycle. During conduction states 1, 3 and 5, one of the series dividing capacitors is connected to V_x . The overall duty cycle, d , of the converter will be defined such that the converter is in each of those states for a time of

$$\frac{d}{3} T_{sw} , \quad (2-1)$$

where T_{sw} is the switching period of the converter. During the conduction states of 2, 4, and 6, V_x is zero as it is shorted out by a combination of switches. The converter is in each of those states for a time of

$$\frac{(1-d)}{3} T_{sw} . \quad (2-2)$$

The waveform applied to V_x over the course of one switching period is illustrated by the plot in Figure 2-6.

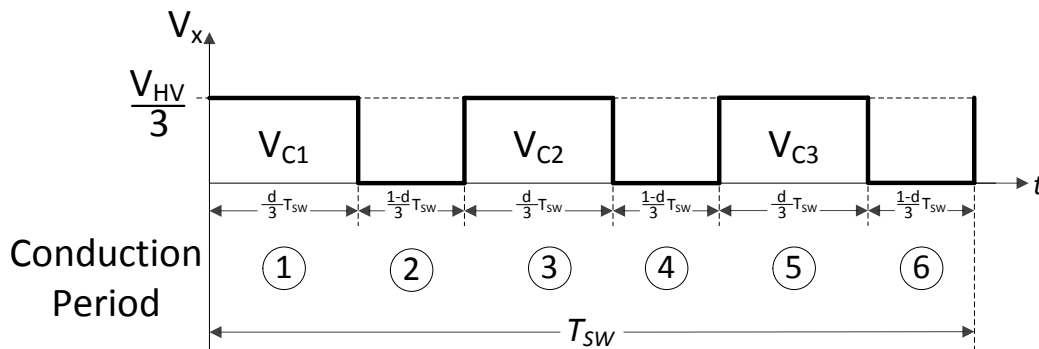


Figure 2-6 Plot of V_x for a four-level converter

To derive the theoretical transformation ratio of the converter under the previously described modulation, recall that the inductor voltage is simply V_x , plotted in Figure 2-6, subtracted by V_{LV} . Assuming the capacitors are sufficiently large that the capacitor voltage ripples can be ignored, the inductor voltage during conduction state 1, 3, and 5 is

$$v_L = \frac{V_{HV}}{3} - V_{LV}, \quad (2-3)$$

while during conduction states 2, 4, and 6, the inductor voltage is

$$v_L = -V_{LV}. \quad (2-4)$$

The inductor volt-second balance equation over one complete switching period is then

$$\langle v_L \rangle = 3 \left[\left(\frac{V_{HV}}{3} - V_{LV} \right) \frac{d}{3} \right] + 3 \left[(-V_{LV}) \frac{1-d}{3} \right] = 0. \quad (2-5)$$

Solving Eq. (2-5), the transformation ratio is found to be

$$\frac{V_{LV}}{V_{HV}} = \frac{d}{3}. \quad (2-6)$$

Notice that a duty cycle of 100% corresponds to a V_{LV} of $\frac{V_{HV}}{3}$. A plot of the transformation ratio vs. duty cycle is shown in Figure 2-7.

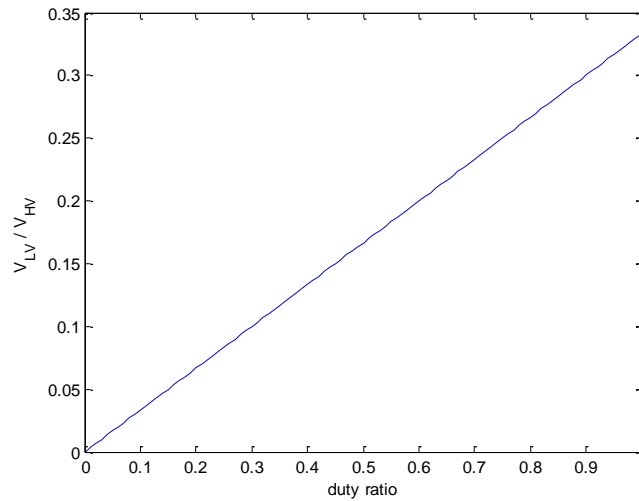


Figure 2-7 Four-level converter transformation ratio vs. duty cycle

Note the large transformation ratios that are possible with this converter typology and modulation scheme. At a duty cycle of 30%, the ideal transformation ratio is 1:10.

It is of interest to calculate the inductor ripple, which can be found from the differential equation describing the inductor voltage and current relationship,

$$v_L = L \frac{di_L}{dt}. \quad (2-7)$$

Rearranging, the peak-to-peak inductor ripple current can be described by

$$\Delta i_{L,pk-pk} = \frac{V_L \Delta t}{L}. \quad (2-8)$$

During conduction period 1, it was previously shown the inductor voltage is $\frac{V_{HV}}{3} - V_{LV}$ and that the period lasts for a duration of $\frac{d}{3} T_{sw}$. Thus, the peak-to-peak current ripple is found by

$$\Delta i_{L,pk-pk} = \frac{\left(\frac{V_{HV}}{3} - V_{LV}\right) d \frac{T_{sw}}{3}}{L} \quad (2-9)$$

or in terms of the switching frequency

$$\Delta i_{L,pk-pk} = \frac{\left(\frac{V_{HV}}{3} - V_{LV}\right) d}{L} \frac{1}{3F_{sw}}. \quad (2-10)$$

For higher level converters, the derivation of the transformation ratio and inductor ripple is just as straightforward. For an N-level converter operating under the previously described modulation, the inductor voltage during the odd conduction states is

$$v_L = \frac{V_{HV}}{N-1} - V_{LV}, \quad (2-11)$$

and those conduction states last for a duration of

$$\frac{d}{N-1} T_{sw}. \quad (2-12)$$

During the even conduction states, the inductor voltage is still

$$v_L = -V_{LV}, \quad (2-13)$$

and those states last for a duration of

$$\frac{(1-d)}{N-1} T_{sw}. \quad (2-14)$$

The inductor volt-second balance equation of the arbitrary N-level converter is

$$\langle v_L \rangle = (N-1) \left[\left(\frac{V_{HV}}{N-1} - V_{LV} \right) \frac{d}{N-1} \right] + (N-1) \left[(-V_{LV}) \frac{1-d}{N-1} \right] = 0 \quad (2-15)$$

and the transformation ratio can be solved to be

$$\frac{V_{LV}}{V_{HV}} = \frac{d}{N-1}. \quad (2-16)$$

The inductor current ripple for the N-level converter is then

$$\Delta i_{L,pk-pk} = \frac{\left(\frac{V_{HV}}{N-1} - V_{LV} \right) d \frac{T_{sw}}{N-1}}{L} \quad (2-17)$$

2.4 Modulation scheme

The modulation scheme proposed in [4] was based on four ramp functions separated by a fraction of the switching period and the gate signals were generated by comparing those ramps to either a constant or a value that was a function of the duty cycle. This approach was advantageous for its simplicity and introduction of the converter. However, that modulation scheme allowed for instances where certain switches would be exposed to higher than necessary voltage stress. Using the four-level converter, a modulation scheme implementation via a state machine is presented that limits the voltage stress of all switches to $\frac{V_{HV}}{3}$. Additionally, the practical consideration of adding deadtime and a brief mention of

voltage balancing of the divider capacitors are made. A four-level converter implemented using N-channel MOSFETs and antiparallel body diodes is shown in Figure 2-8.

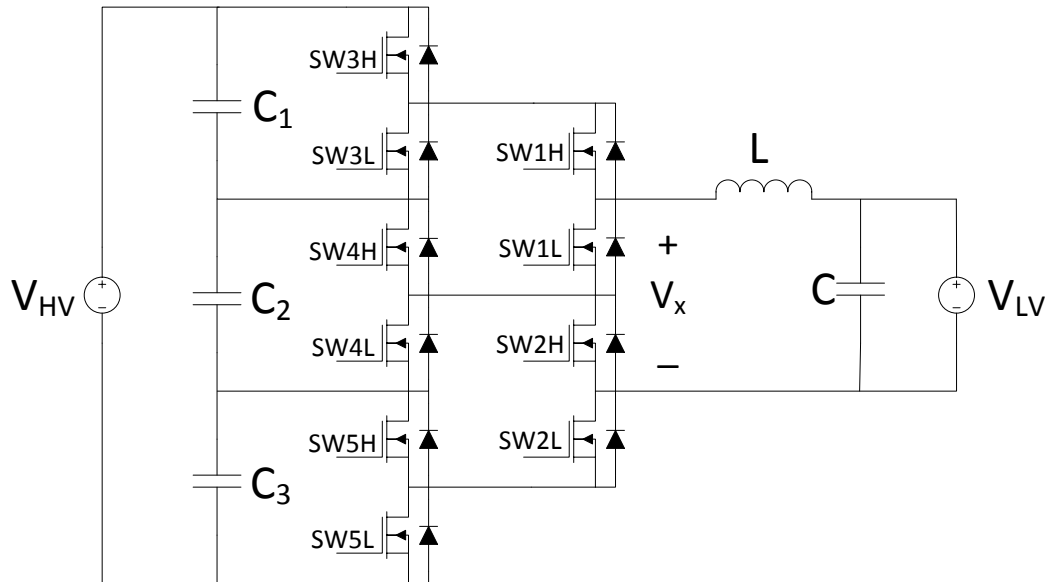


Figure 2-8 Schematic of a four-level converter with N-channel MOSFETs and antiparallel body diodes

The conduction states of the four-level converter, originally shown with SPDT switches in Figure 2-5, are repeated in Figure 2-9.

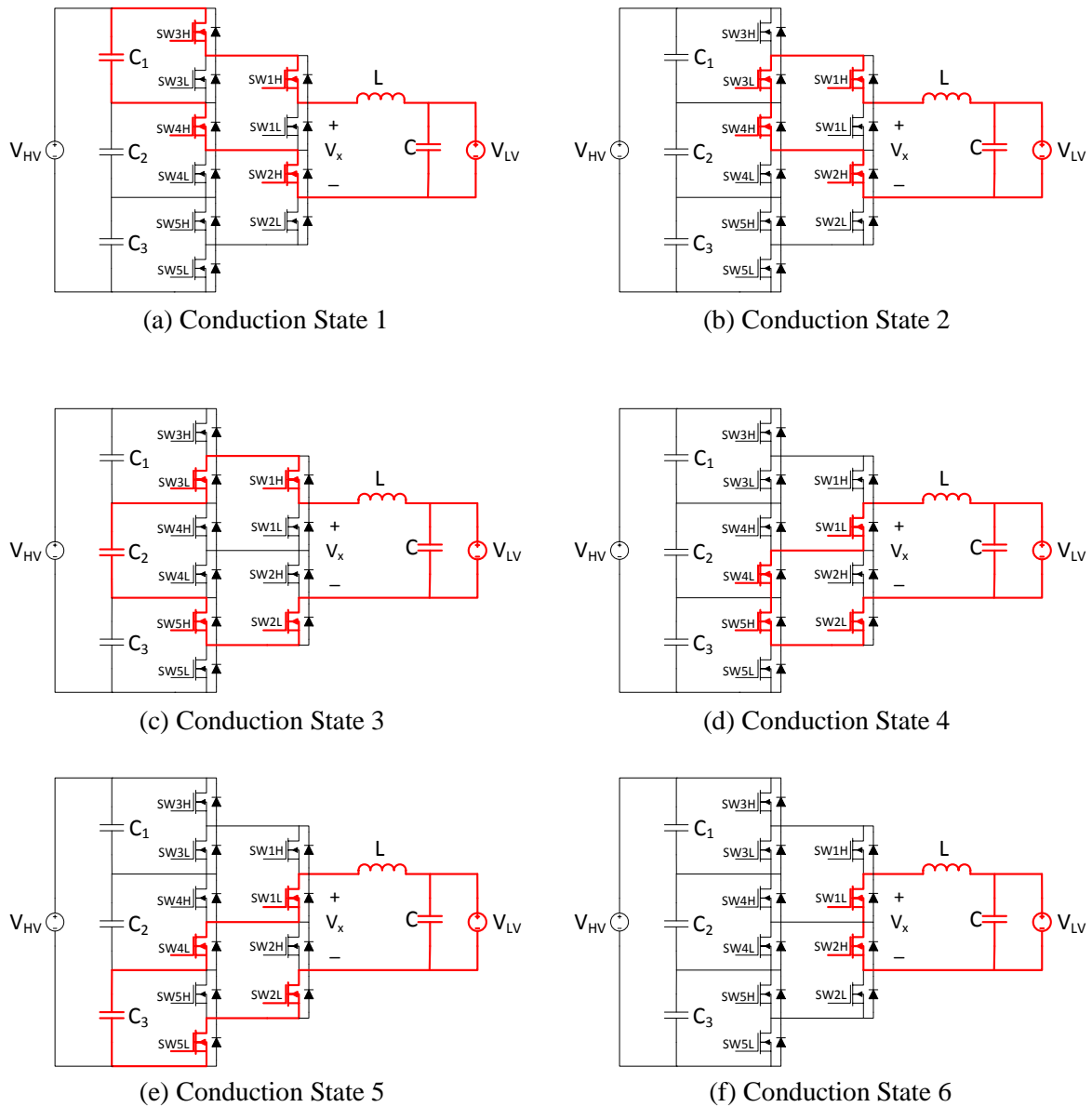


Figure 2-9 Conduction states of four-level converter

In the figure, the MOSFETs that are on during the conduction states in order to conduct the inductor current are highlighted in red. Note that depending on the direction of the inductor current, current may also flow through the body diode of a given switch in addition to the MOSFET. From Figure 2-9, the state diagram in Figure 2-10 can easily be derived.

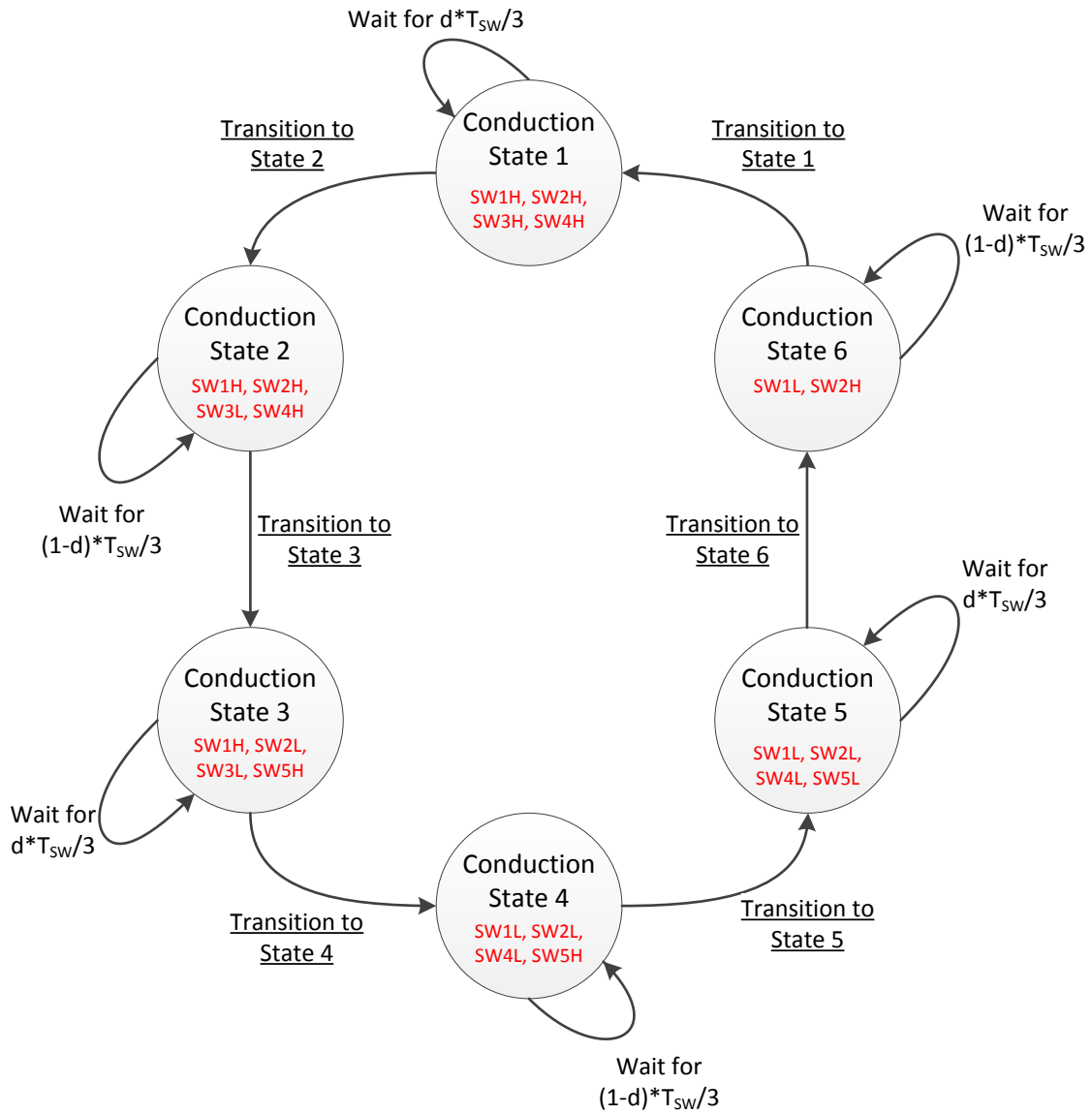


Figure 2-10 State diagram based on conduction states

Although the periods in which each switch needs to be on is obvious by simply observing the conduction states in Figure 2-9, there are a few more considerations when it comes to implementing the transitions of the switches to ensure that the voltage stress of the switches does not exceed the maximum of $\frac{V_{HV}}{3}$. First, there are certain situations in which the turn-on and turn-off timing of switches that are not conducting the inductor current must be paid particular attention to. For example, during conduction periods 1 or 2, if SW5L is on,

the drain of SW2L is connected to the negative terminal of V_{HV} while the source of SW2L is connected through SW2H and SW4H to C_2 . This results in a voltage of $\frac{2V_{HV}}{3}$ being applied across SW2L as shown in Figure 2-11. To alleviate this SW5H, and not SW5L, must remain on during conduction states 1 and 2.

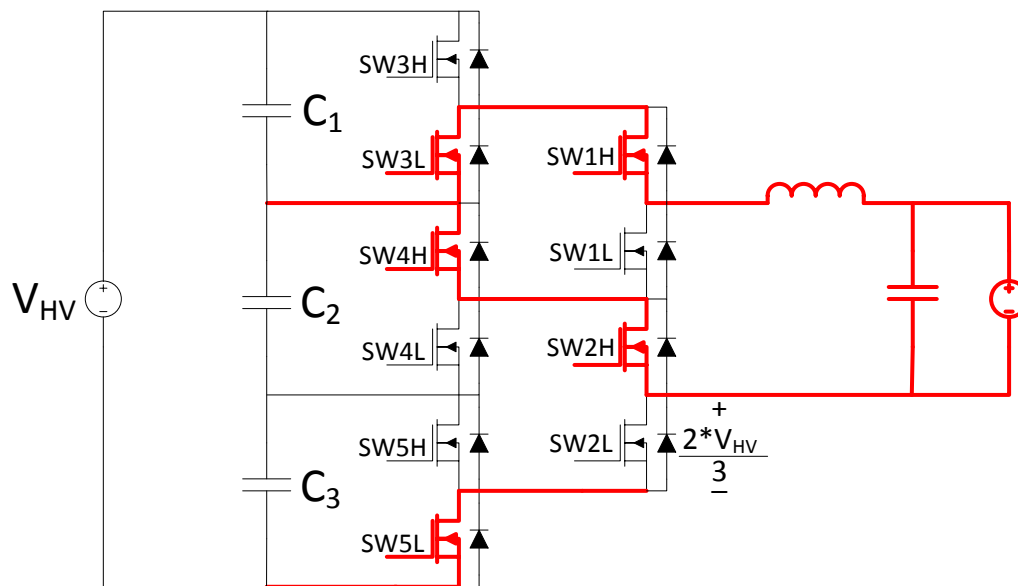


Figure 2-11 Excessive switch voltage stress being applied to SW2L

Similarly, if SW3L must remain on during conduction periods 4 or 5 to avoid a voltage of $\frac{2V_{HV}}{3}$ is applied across SW1H. Finally, during conduction period 6, if switches 3, 4 and 5 do not all have the low-side MOSFETs (SW3L, SW4L and SW5L) on or all have the high-side MOSFETs (SW3H, SW4H, and SW5H) on, a voltage of $\frac{2V_{HV}}{3}$ will be applied across SW1H or SW2L.

A second consideration for implementing the switch transitions which applies to a physically built converter rather than the ideal converter is the implementation of dead time between switch transitions of the high side and low side MOSFETs on the same half-bridge.

The bidirectional converter has two basic modes of operation based on the direction of power flow: “bucking” operation and “boosting” operation. During bucking operation, power is flowing from V_{HV} to V_{LV} and thus the inductor current is flowing towards V_{LV} . During the dead time states, that current is able to freewheel through the diodes that are parallel to SW1L and SW2H and/or flow through the actual MOSFET in SW1L and SW2H, if that switch happens to be on during the dead time. It turns out there are no situations in which the switch stress exceeds $\frac{V_{HV}}{3}$ during the dead time in the bucking operation. However, that is not the case in boosting operation in which the power flow is from V_{LV} to V_{HV} . Here, the inductor current is flowing away from the V_{LV} side and implementing dead time has the ability to cause higher than the desired voltage stress of $\frac{V_{HV}}{3}$ to be applied across a single switch. An example of this is during the transition from conduction state 5 to conduction state 6 as displayed in Figure 2-12.

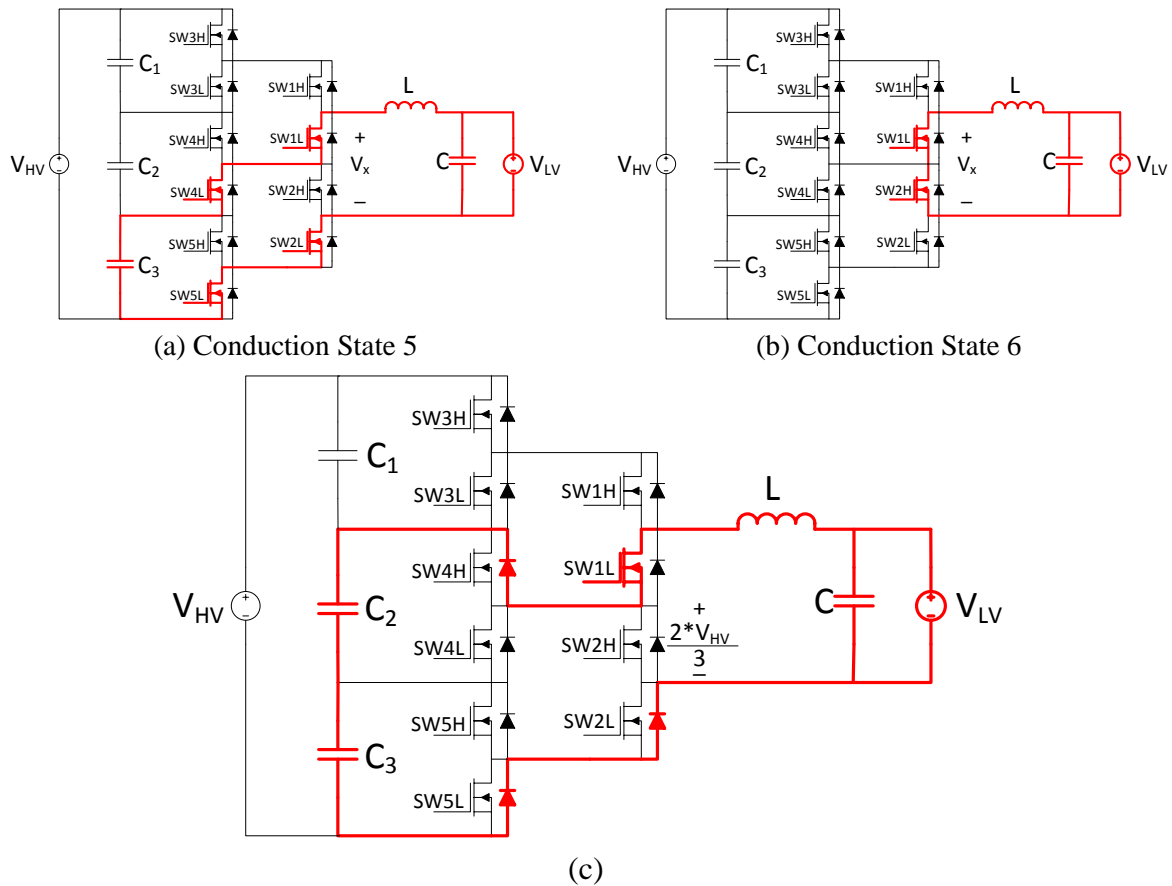


Figure 2-12 Excessive switch voltage stress being applied in to SW2H (c) during dead time between (a) conduction state 5 and (b) conduction state 6

In conduction state 5, SW1L, SW4L, SW5L and SW2L are conducting current and in this scenario, the converter is in boosting operation so the inductor current is flowing away from the V_{LV} source. In order for the converter to be in conduction state 6, SW2L must be turned off and SW2H must be turned on with a dead time occurring between the two. In Figure 2-12(c), SW4L is also turned off at the same time as SW2L. (Note: SW5L is turned off as well due to the previously discussed need to have SW3, SW4, and SW5 all having their high-side FET on or all having their low-side FET on during conduction state 6.) The inductor current is then forced to flow through SW1L, the body diode of SW4H, C_2 and C_3 , and finally through the body diodes of SW5L and SW2L. This applies a voltage of $\frac{2V_{HV}}{3}$ to

SW2H. To resolve this, SW4L needs to remain on during the SW2 dead time, allowing the inductor current to flow in the path portrayed by Figure 2-13, which applies the desired maximum switch voltage stress of $\frac{V_{HV}}{3}$ across SW2H.

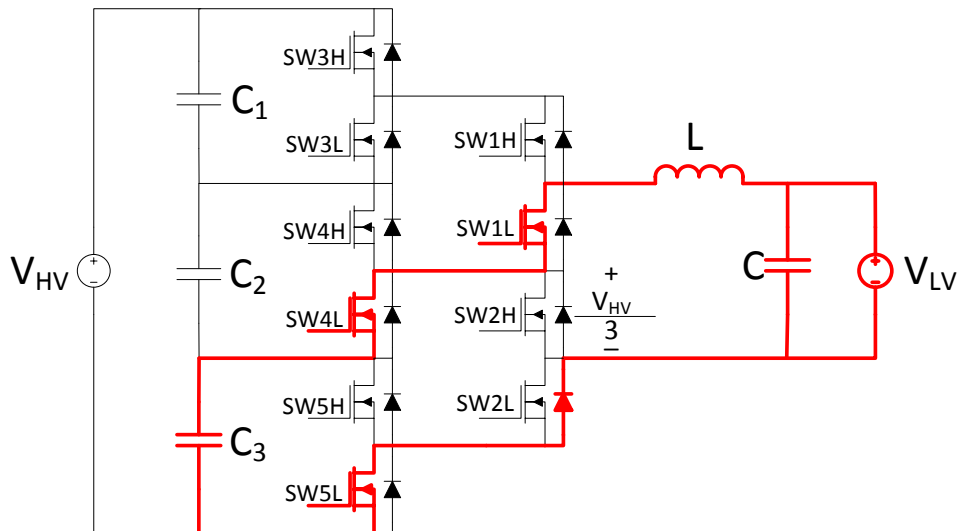


Figure 2-13 Desired maximum switch voltage stress during dead time between conduction state 5 and conduction state 6

An additional note on the dead time is that it makes sense to implement the dead time during the even conduction states if the converter is in bucking operation or during odd conduction states if the converter is in boosting operation. To illustrate this, Figure 2-14 shows conduction state 1, the dead time state for both bucking and boosting operation, and conduction state 2.

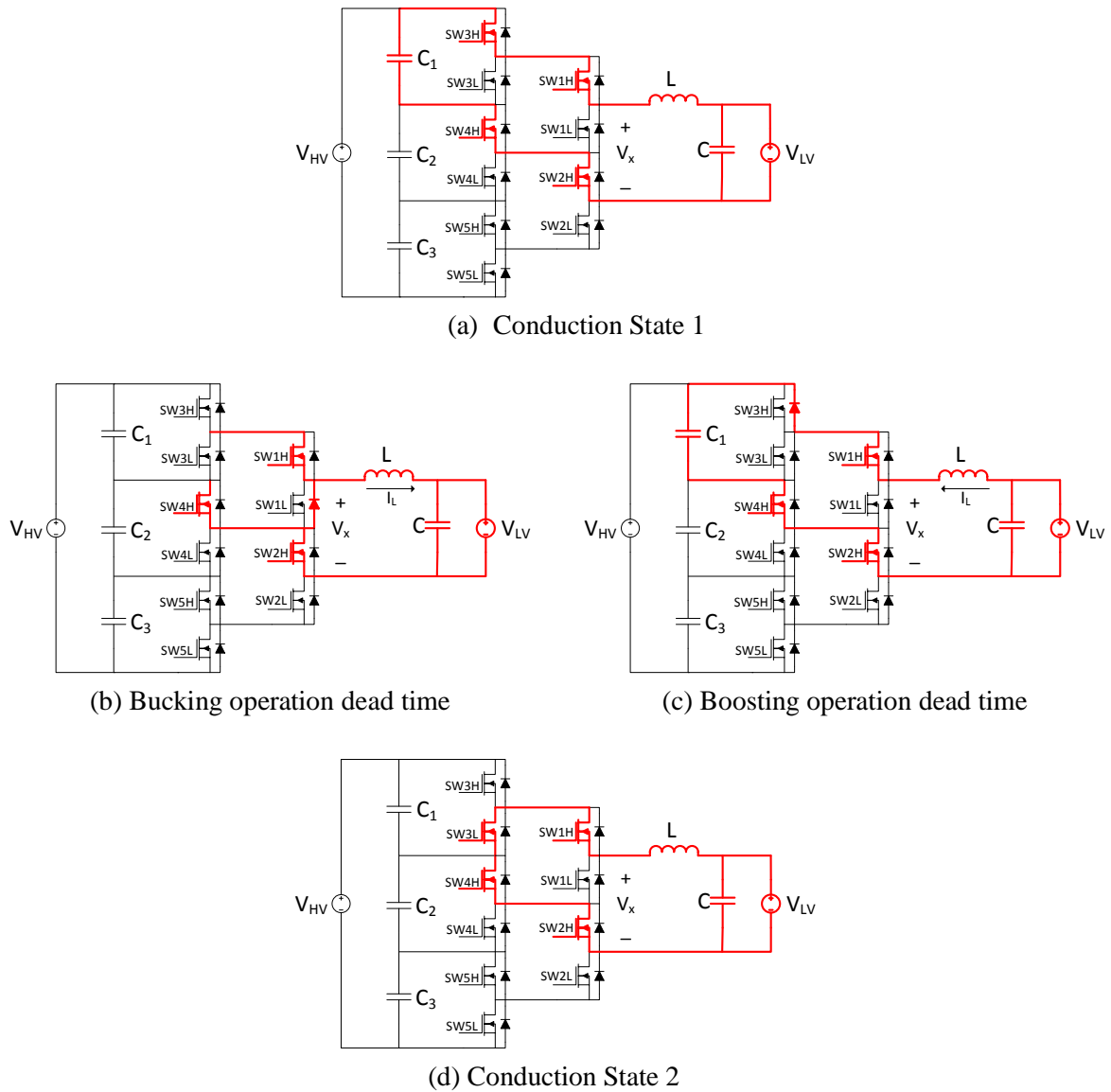


Figure 2-14 Dead time state for a four-level converter in (b) bucking operation and (c) boosting operation for the transition state between (a) conduction state 1 and (d) conduction state 2

Notice in the figure that during the bucking operation dead time, the inductor current is able to flow through the antiparallel diode connected to SW1L. This has the same functionality of conduction state 2 as they both apply 0 V to V_x . While during the boosting operation dead time, the current flows through the antiparallel diode of SW3H and has the same function of conduction state 1 as $\frac{V_{HV}}{3}$ is applied to V_x . Thus, it makes sense for the dead

time to take place during the time that would ideally be allocated to the even conduction states for bucking operation and the odd conduction states for boosting operation. A state diagram of the complete modulation scheme that limits the switch voltage stress to $\frac{V_{HV}}{3}$ and takes into account dead time is shown in Figure 2-15.

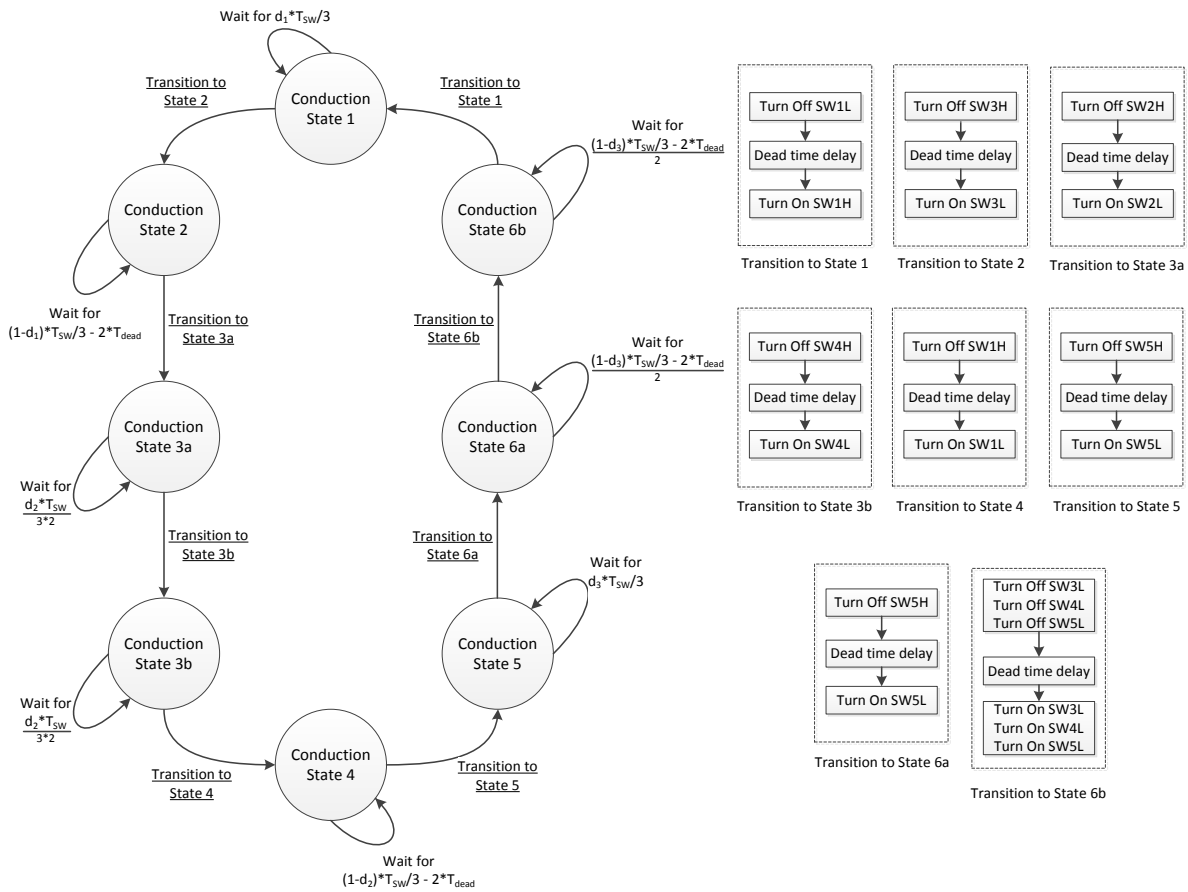


Figure 2-15 Modulation scheme state diagram including switch transitions and dead time for bucking operation

The diagram in Figure 2-15 is for bucking operation. In order to conceive the same diagram for boosting operation, the dead times simply needs to be moved to the odd conduction states. The conduction states 3 and 6 have been split into two conduction states of

equal duration and switch transitions occur in between the two halves of the conduction states. The fact that the transitions occur at the halfway point of those conduction states was arbitrarily chosen. The “Transition to State 3b,” which includes the turning off SW4H and turning on SW4L, was placed during conduction state 3 to allow for zero current transitions of those devices. The “Transition to State 6b” occurs halfway through conduction state 6 to prevent the applying excessive switch stress as previously shown in Figure 2-12.

Another thing to note about the figure is that the duty cycle d has been replaced by d_1 , d_2 , and d_3 . The new duty cycles relate to the duration in which each of the high voltage side divider capacitor is transferring energy with the low voltage side source or load. For instance, $d_1 * T_{SW}/3$ is the duration in which the converter is in conduction state 1. During that state, the capacitor C_1 is connected across V_x and the inductor current is either flowing into or out of the capacitor. In the ideal case, d_1 , d_2 , and d_3 would be equal do the overall duty cycle of the converter, d :

$$d_1 = d_2 = d_3 = d \quad (2-18)$$

However, due to tolerances and parasitic of the divider capacitor, PCB, gate drive circuitry, etc., there may be a need to adjust the duty cycles to take slightly more or less energy from a certain capacitor in order to balance the capacitor voltages.

Chapter 3 *Prototype converter design*

This chapter presents the details of a four-level prototype converter that was developed. A schematic of the four-level converter implemented with MOSFETs is shown in Figure 3-1.

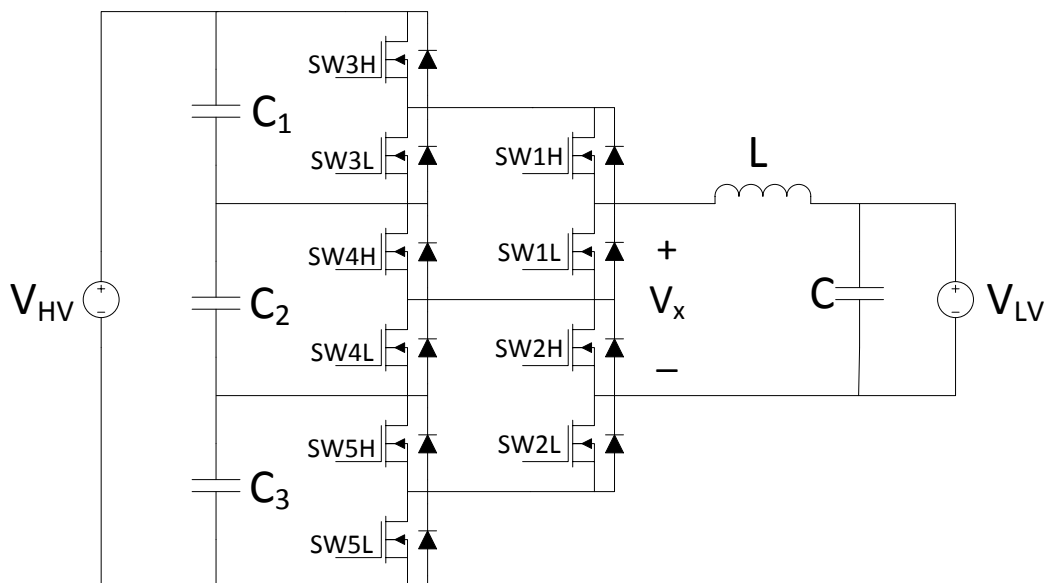


Figure 3-1 Schematic of a four-level converter with MOSFETs

The prototype's purpose was to serve as a proof of concept of the multilevel, buck-derived DC-DC converter typology. The hardware implementation concentrated purely on the bucking mode of operation of the converter. Section 3.1 presents the specifications the board was designed to and details the selection of the major components. In Section 3.2, the hardware and software that was used to generate the gate signals is described. Section 3.2 displays the completed hardware and presents the PCB schematics and top and bottom copper planes.

3.1 Design specifications and component selection

The converter was designed for the bucking mode of operation and the design specifications are displayed in Table 3-1.

Table 3-1 Design specifications of the prototype converter

Maximum V_{HV}	225 V
Range of V_{LV}	15V – 60 V
Maximum I_{LV}	8 A
Maximum Power	350 W
Switching Frequency	10 kHz
Inductor Peak-to-Peak Ripple Current	2 A
Output Peak-to-Peak Ripple Voltage	0.1 V

The inductor was designed around the 2 A inductor ripple specification. The inductor ripple current equation derived in Section 2.3 is

$$\Delta i_L = \frac{\left(\frac{V_{HV}}{3} - V_{LV}\right) d \frac{T_s}{3}}{L}. \quad (3-1)$$

If the transformation ratio of the four-level converter given in (2-6) is solved for V_{LV} and substituted into (2-8) while separating out the d terms, the ripple equation becomes

$$\Delta i_L = \frac{V_{HV} T_s}{3} \frac{1}{3L} (d - d^2). \quad (3-2)$$

The maximum ripple occurs at a 50% duty cycle. Using the 2 A inductor ripple specification and the 50% duty, the minimum inductance is found to be 312.5 μH . A nominally 330 μH inductor made by Bourns with part number 1140-331K-RC was chosen. The relevant specifications of the inductor are shown in Table 3-2.

Table 3-2 Bourns 1140-331K-RC inductor specifications [6]

Inductance	330 μ H
Tolerance	$\pm 20\%$
Max DC resistance	0.074 Ω
Max DC current	11.4 A

Next, the MOSFETs were selected. With a maximum high voltage of 225 V, the ideal maximum applied voltage across a single switch is 75 V. The maximum DC current is specified at 8 A. The MOSFETs chosen were Fairchild Semiconductor's FDP26N40 N-Channel MOSFETs which are rated for 400 V and 26 A. The voltage rating of the selected device is fairly conservative but the FDP26N40 was selected primarily since it is currently used in a power electronics lab course at the University of Wisconsin-Madison. Using that MOSFET, allowed for use of much of the same proven gate drive circuitry. Specifications of the MOSFETs are shown in Table 3-3.

Table 3-3 FDP26N40 N-channel MOSFET specifications [7]

Maximum V_{DS}	400 V
Maximum I_D	26 A
Typical $R_{DS,on}$	0.13 Ω
Typical Turn-On Delay Time	45 ns
Typical Turn-On Rise Time	100 ns
Typical Turn-Off Delay Time	115 ns
Typical Turn-Off Fall Time	66 ns
Maximum Continuous Diode Forward Current	26 A
Estimated Diode Forward Voltage	0.69 V
Estimated $R_{D,on}$	14.3m Ω

The estimated diode forward voltage drop and estimated $R_{D,on}$ were found by linearly approximating the 25°C curve from [7] shown in Figure 3-2 for currents from 1 A to 10 A.

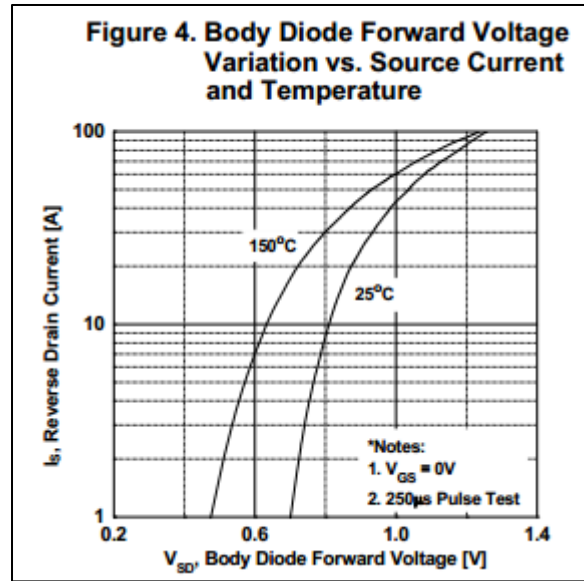


Figure 3-2 FDP26N40 reverse drain current versus body diode forward voltage [7]

The low voltage filter capacitance was chosen based on the specified output voltage ripple. From [8], the output voltage ripple of a two-pole low pass filter can be estimated by

$$\Delta v = \frac{\Delta i_L T_S}{8C} \quad (3-3)$$

where Δi_L is the peak ripple of the inductor current, T_S is the period of the inductor current, C is the filter capacitance, and Δv is the change in output voltage. Adapting Eqn. (3-3) for the three times the switching frequency that the inductor experiences in the four-level converter and using peak-to-peak quantities, the output voltage ripple becomes

$$\Delta v_{c,pk-pk} = \frac{\Delta i_{L,pk-pk} T_{SW}}{24C} \quad (3-4)$$

Rearranging Eqn. (3-4), the minimum capacitance is found by

$$C \geq \frac{\Delta i_{L,pk-pk} T_{SW}}{24\Delta v_{c,pk-pk}} \quad (3-5)$$

Using the specifications given in Table 3-1, the minimum capacitance is 83.3 μ F. The capacitor also had to be capable of handling the ripple current. The ripple current seen by the capacitor is the ripple current of the inductor. The maximum specified inductor ripple current is 2 A_{pk-pk}. The RMS value of the triangular inductor current is $\frac{V_{pk}}{\sqrt{3}}$ and thus the capacitor must be rated for a ripple current greater than 0.333 A_{RMS}. The low voltage capacitor was selected to be a 100 μ F capacitor from Panasonic with part number EEUEE2E101S. The specifications for that capacitor are shown in Table 3-4.

Table 3-4 Specifications of the EEUEE2E101S capacitor used in the low voltage output filter

Nominal Capacitance	100 μ F
Tolerance	$\pm 20\%$
Voltage Rating	250 V
Ripple Current Rating (@100kHz)	2.1 A _{RMS}

The high voltage capacitors were selected to be 330 μ F, 250 V rated capacitors made by EPCOS Inc. with part number B43504C2337M. Since the bucking mode of operation was concentrated on for the hardware designed, these capacitors were chosen mainly for their high ripple current rating based on the ripple currents seen in the simulation of the converter.

Also, due to the impact on the efficiency of the converter, it's worth mentioning, RCD snubbers were also designed for each MOSFET. The snubbers were designed using an application guide from [9]. Details of the snubber components are shown in Table 3-5

Table 3-5 Snubber components and component parameters

Resistor	Resistance	6.2 Ω
	Power Rating	1 W
Capacitor	Capacitance	12 nF
	Part number	US1M
Diode	Voltage	1 kV
	Peak forward surge current	30 A
	Estimated Forward Voltage Drop	0.925 V
	Estimated On Resistance	50 m Ω

3.2 Gate signal generation

A Stellaris LM3S1968 Evaluation Board from Texas Instruments shown in Figure 3-3 was used to generate the gate signals for the converter. The board only possesses an 8 MHz clock and even though that is multiplied to 50 MHz by an internal PLL for core clocking, the board is still fairly slow by the capabilities of today's microcontrollers.

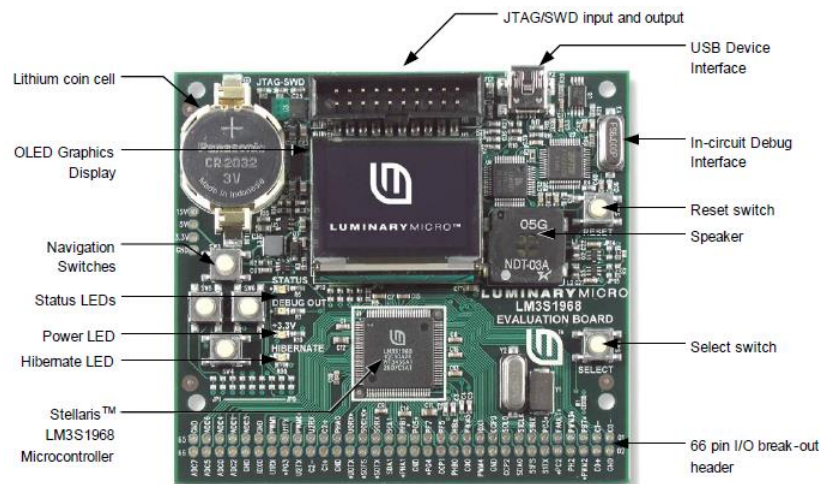


Figure 3-3 Stellaris LM3S1968 Evaluation Board [10]

The gate signals were generated by implementing a state machine that functioned similarly to that of the state machine previously illustrated in Figure 2-1. A dead time of 1.25 μ s was implemented between turn-off and turn-on transitions of MOSFETs of the same

half-bridge. All eight of the LM3S1968's Port F GPIO ports and two of the Port D GPIO ports were used to output the signal side gate signals. The signals then passed through a SI8420 digital isolator generate a 0 to 5 V signal referenced to the source of the low side power MOSFET of each half-bridge. The signals were then level shifted to 0 to 15 V using a UCC37324 MOSFET driver to become the input to the actual gate driver.

3.3 PCB design

The completed prototype converter is pictured in Figure 3-4. The right half of the board contains all of the power components with all ten N-channel MOSFETs seen attached to heat sinks in line vertically near the center of the board, the inductor and high side and low side capacitors to the right of the heat sinks, and the high voltage and low voltage connectors on the far right of the board. All signal level circuitry is on the left side of the board.



Figure 3-4 Hardware of the prototype four-level converter

The schematics of the hardware PCB are shown in Figure 3-5 through Figure 3-10.

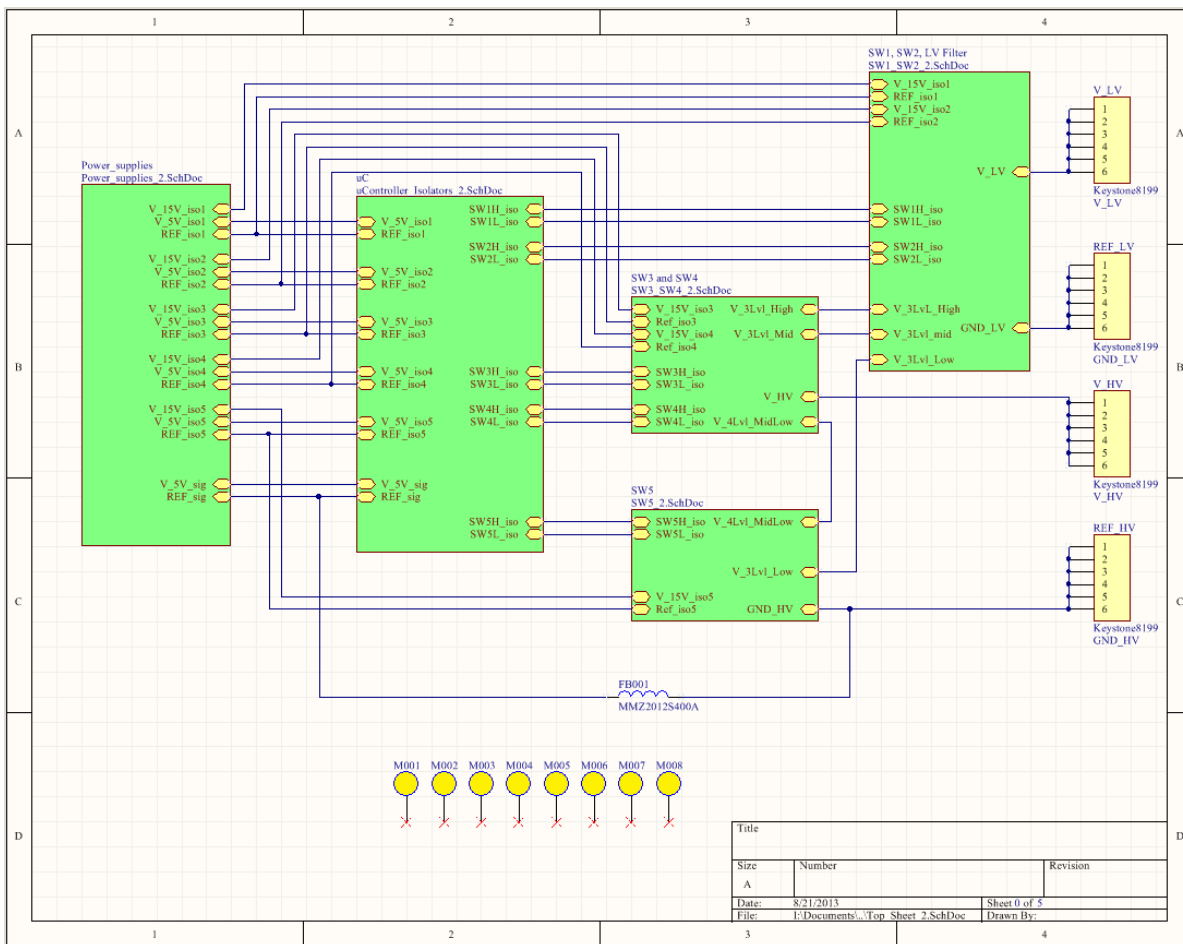


Figure 3-5 Top sheet schematic showing interconnections of daughter sheets

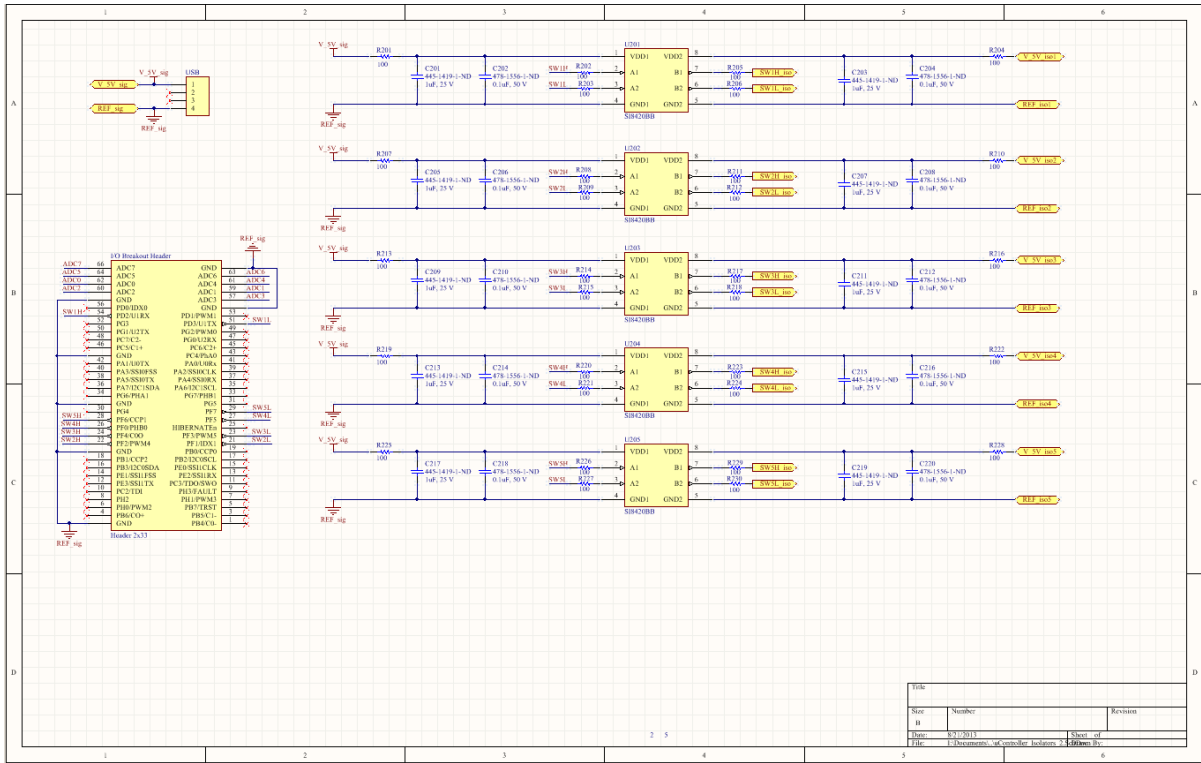


Figure 3-6 uC daughter sheet containing the microcontroller header and digital isolators

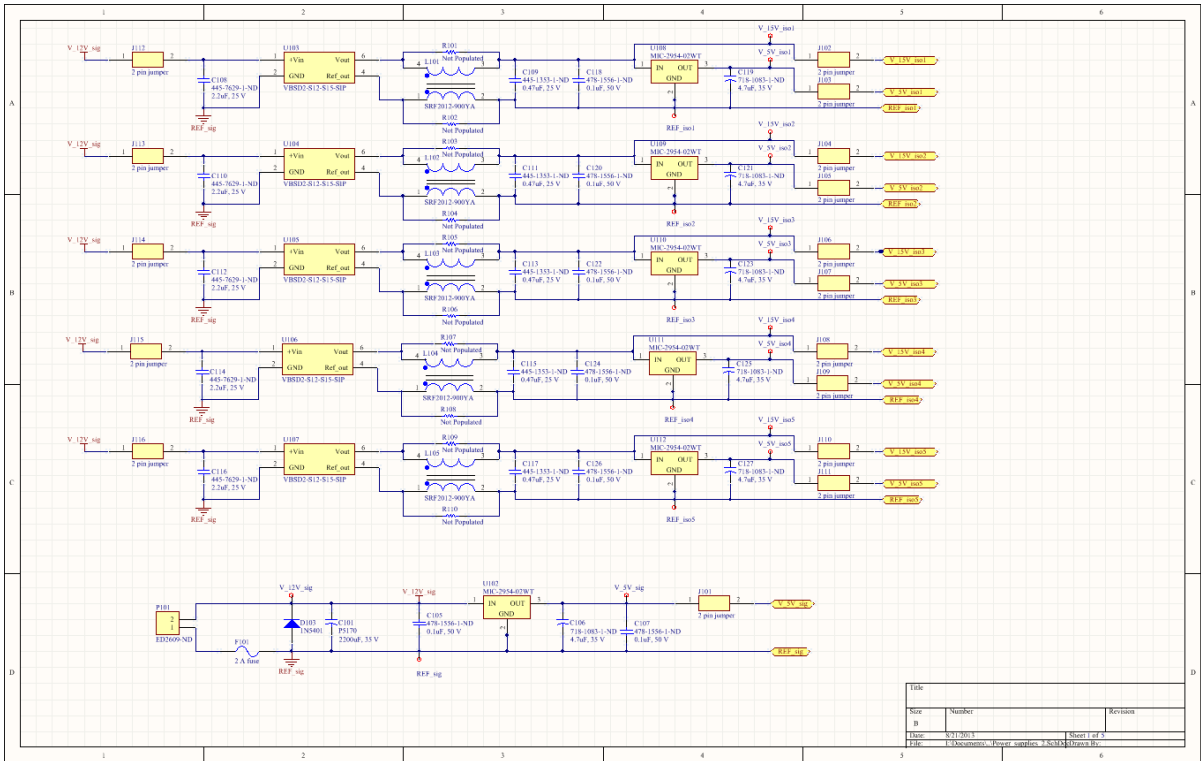


Figure 3-7 Power_supplies daughter sheet containing the microcontroller power supply and five isolated 12 V and 5 V supplies for each half-bridge

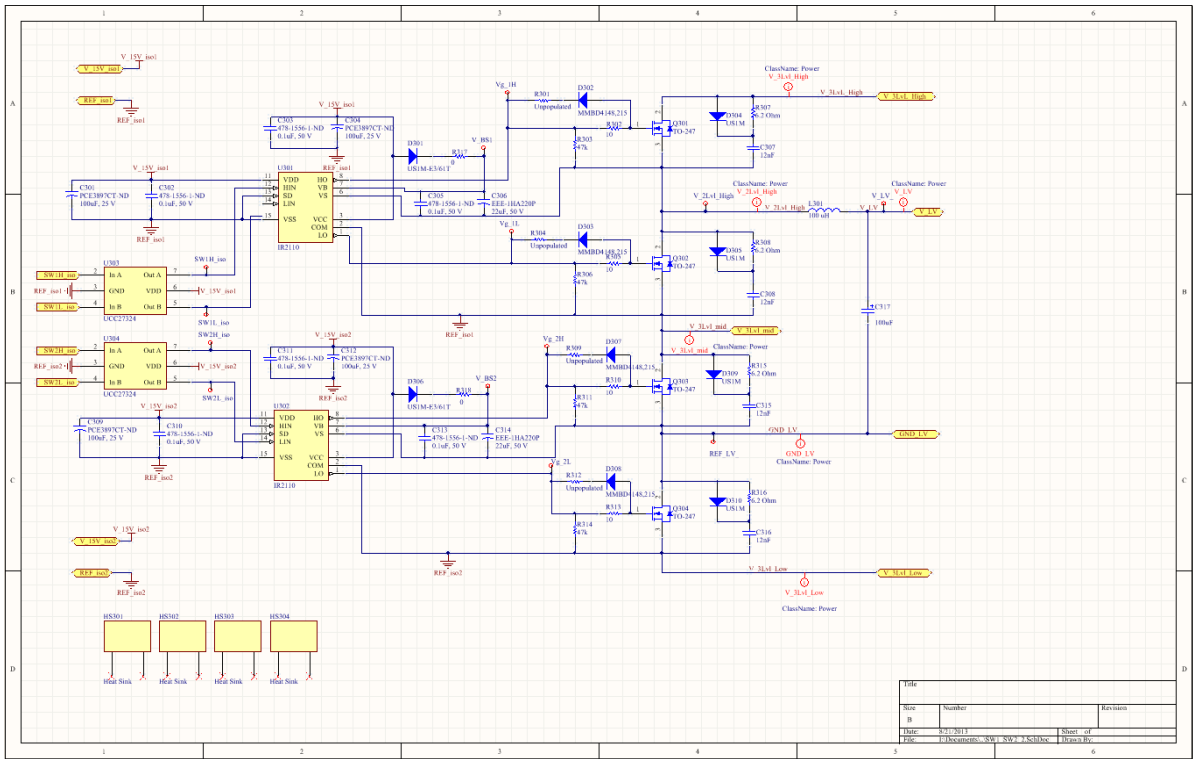


Figure 3-8 SW1 and SW2 daughter sheet containing the gate drive circuitry and switches for SW1 and SW2 as well as the low voltage filter

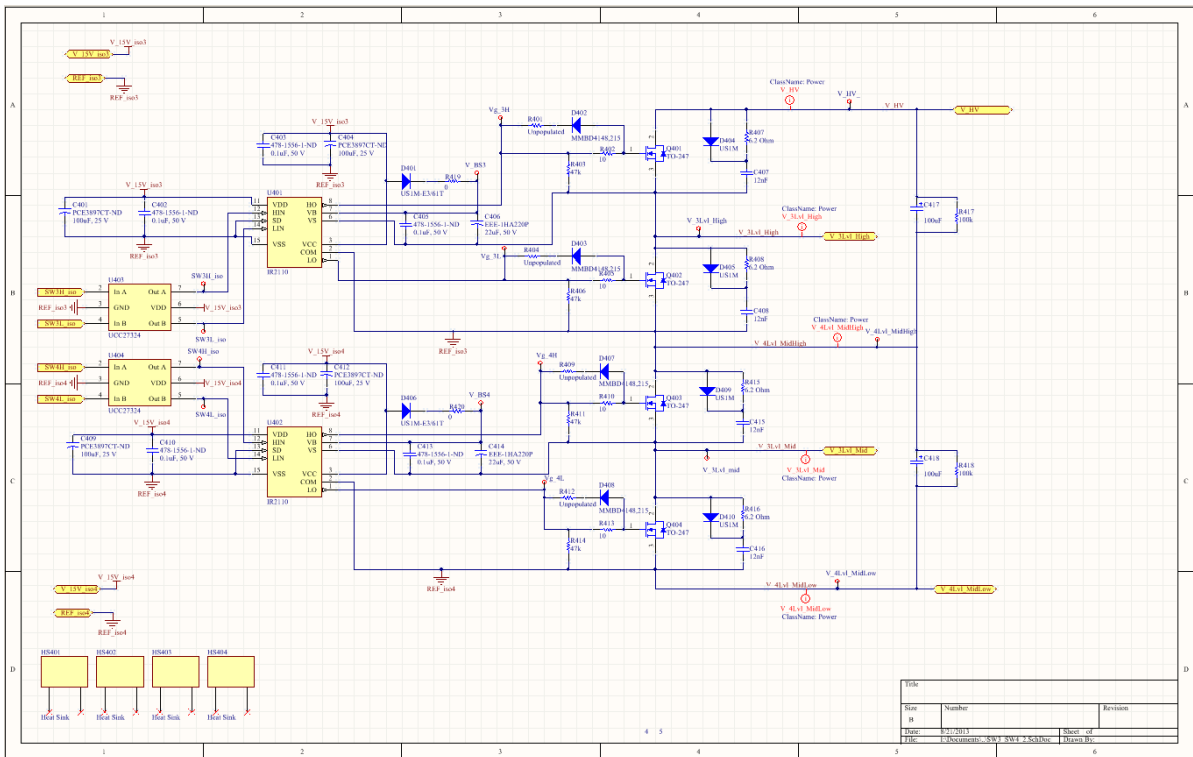


Figure 3-9 SW3 and SW4 daughter sheet containing the gate drive circuitry and switches for SW3 and SW4 as well as the divider capacitors C₁ and C₂

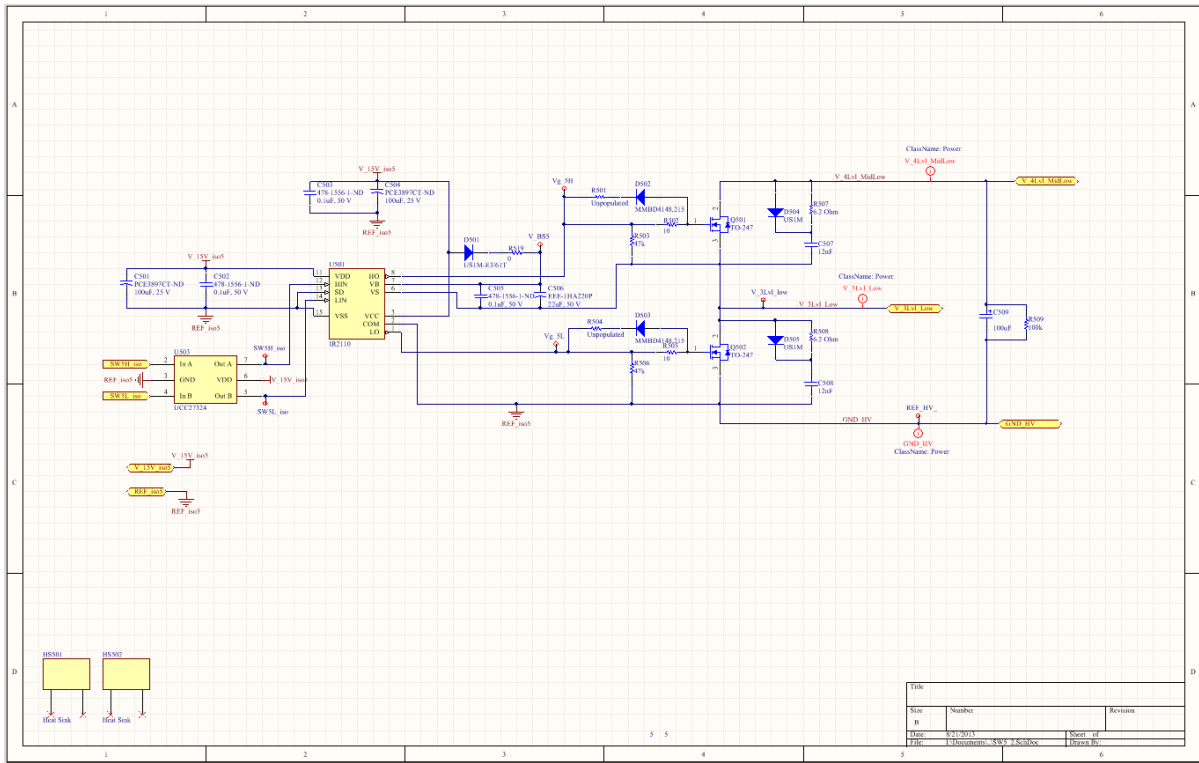
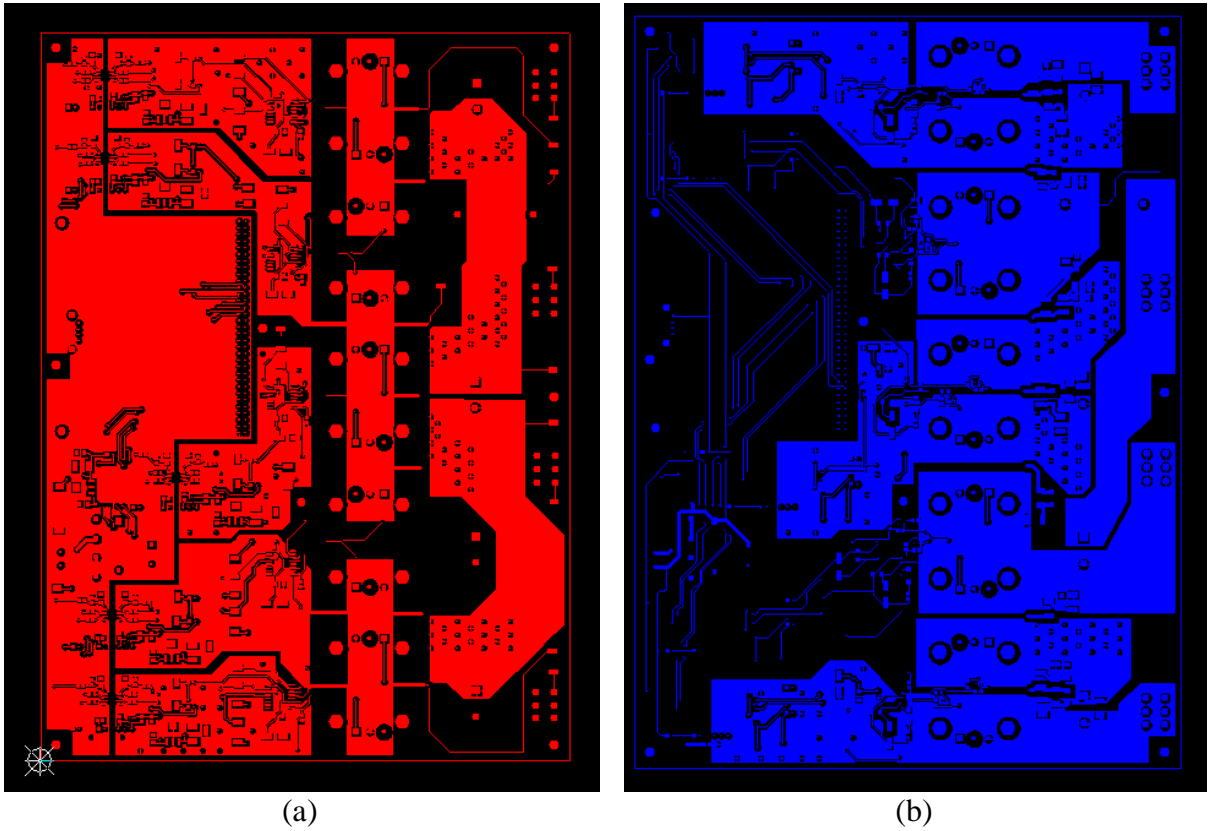


Figure 3-10 SW5 daughter sheet containing the gate drive circuitry and switches for SW5 as well as the divider capacitor C₃

The top and bottom copper layers are shown in Figure 3-11.



(a) (b)
Figure 3-11 Copper layers on the (a) top and (b) bottom of the PCB

The major loss mechanisms of the converter in operating in bucking mode are discussed in this section. In section 4.1 the numerous zero current and zero voltage transitions that occur with the four-level converter are documented and equations describing the MOSFET switching losses are presented. Section 4.2 describes the conduction losses of the power MOSFET and diode.

4.1 MOSFET switching losses

The switching losses will be approximated assuming linear drain-to-source voltage and drain current transitions. The turn-on and turn-off power loss can then be approximated by

$$P_{FET,sw,on} = \frac{1}{2} v_{DS} i_d (t_{delay,on} + t_{rise}) * f_{SW} \quad (4-1)$$

$$P_{FET,sw,off} = \frac{1}{2} v_{DS} i_d (t_{delay,off} + t_{fall}) * f_{SW} [8]. \quad (4-2)$$

With control scheme previously described and shown in Figure 2-15, there are a number of switch transitions that occur in which the switch is not conducting current or in which there is virtually no voltage across the switch. In those situations, the switching loss can be ignored. To illustrate this, the switching power loss equations of the transition state between the conduction states 1 and 2 will be observed. These states are shown in Figure 4-1.

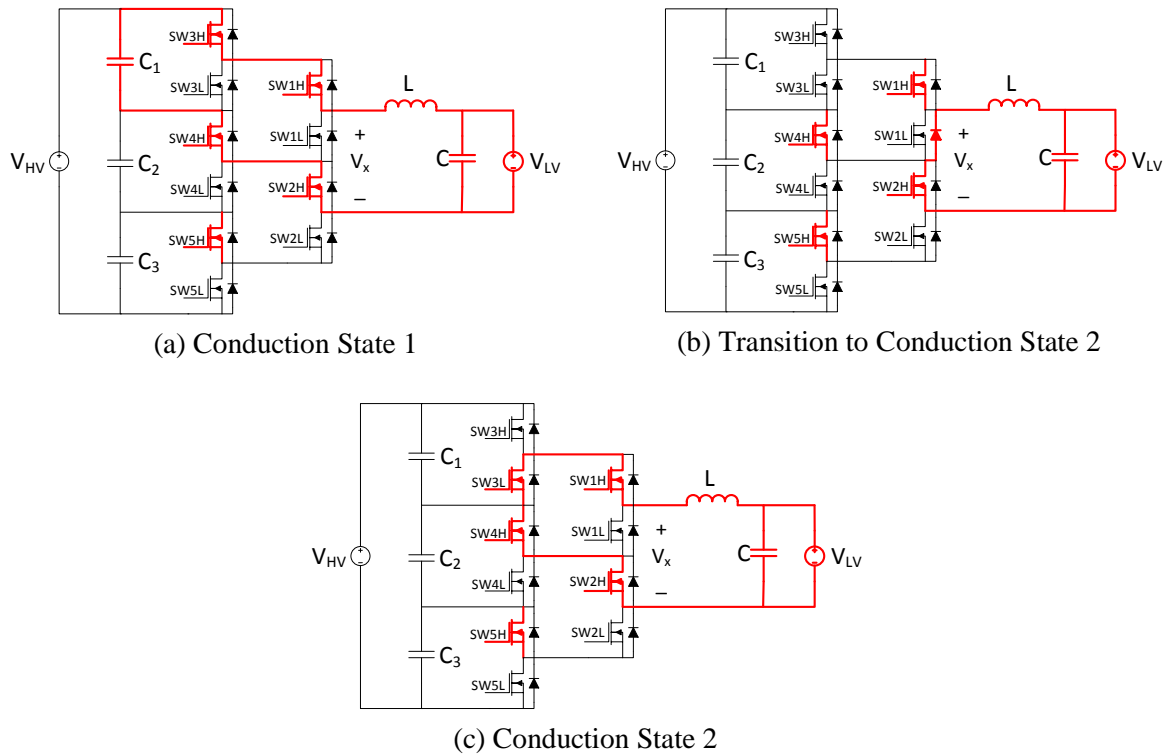


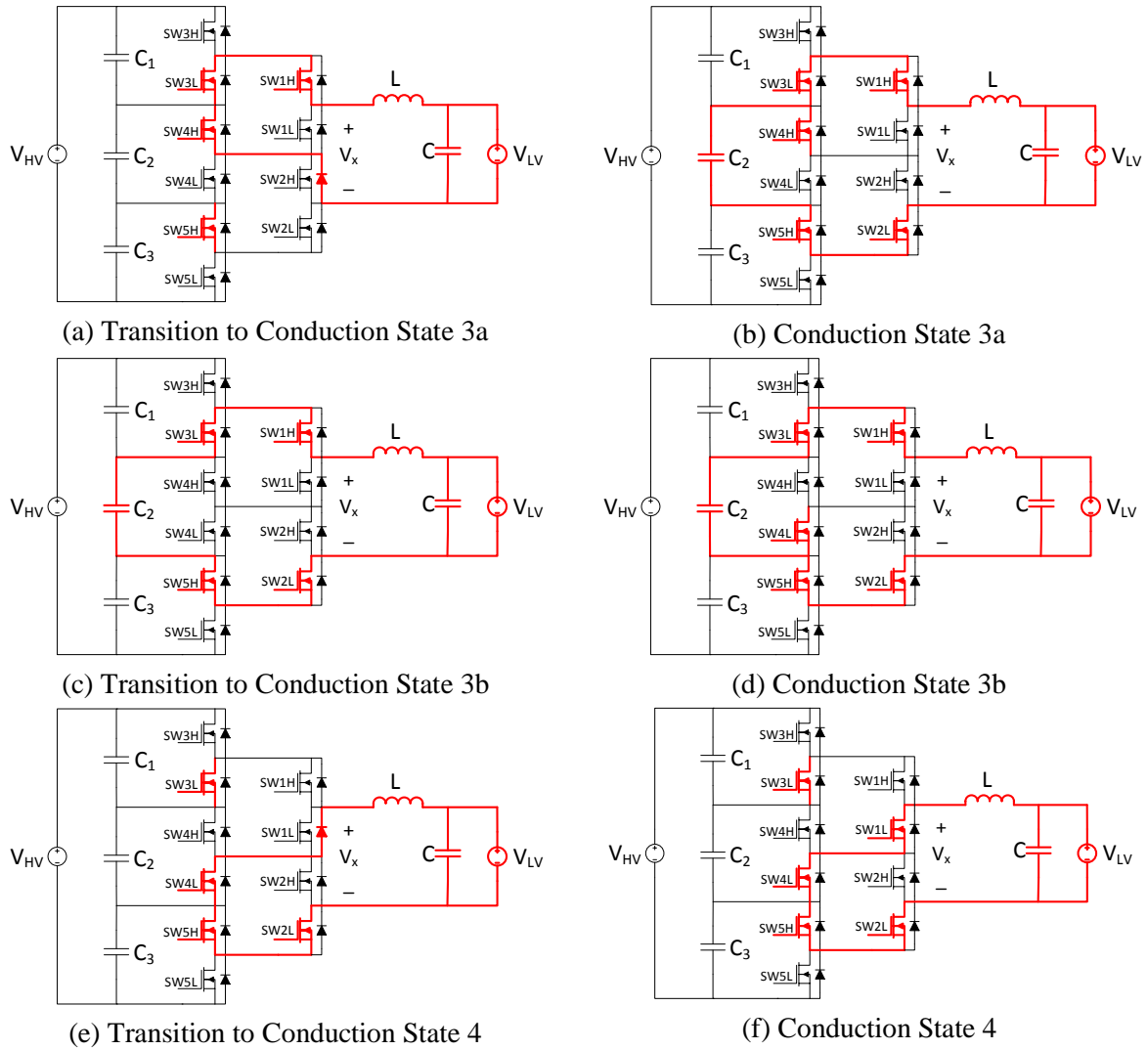
Figure 4-1 Conduction states 1 and 2 and then transition state between them

For this analysis, the switches and diodes will be assumed to be ideal. The schematics in the figure show in red the switches that are on during each state as well as the inductor current conduction path. In Figure 4-1 (a), the inductor voltage is $\frac{V_{HV}}{3} - V_{LV}$, meaning the inductor current is at its peak value at the end of the conduction period 1, and the current conducted by SW3H is equal to $I_{Load} + 0.5 \cdot i_{L,pk-pk}$, or $i_{L,max}$, just prior to turning off. In Figure 4-1 (b), it can be seen that the combination of SW1H, SW4H and SW1L's antiparallel diode create a short across SW3L. This results in the voltage across SW3L being ideally 0 V prior to its turn on and the V_{DS} of SW3H equal to $\frac{V_{HV}}{3}$ following its turn off. Following the transition state that lasts for the duration of the dead time, SW3L is turned on. Assuming the dead time is small, it can be assumed that the inductor current is still $i_{L,max}$. The resulting turn-off loss and turn-on loss equations for SW3H and SW3L, respectively, are

$$P_{SW3H,off} = \frac{1}{2} \frac{V_{HV}}{3} i_{L,max} (t_{delay,off} + t_{fall}) f_{SW} \quad (4-3)$$

$$P_{SW3L,on} = \frac{1}{2} (0) i_{L,max} (t_{delay,on} + t_{raise}) f_{SW} = 0 \quad (4-4)$$

Similarly, the relevant v_{DS} and i_D can be found for all other switches. The remaining conduction states and transition states are shown in Figure 4-2.



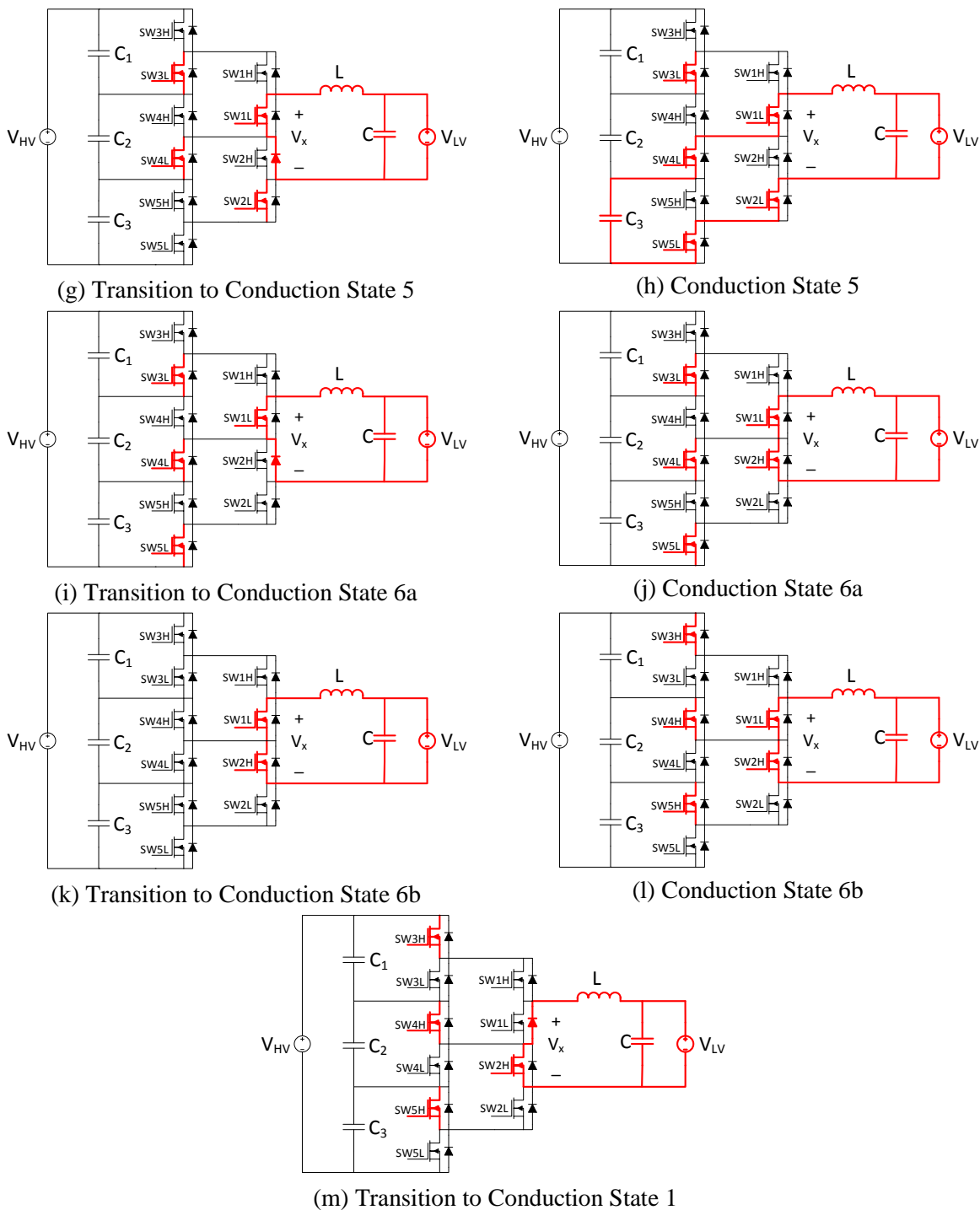


Figure 4-2 Remaining conduction and transition states

Using the conduction and transitions states in the figure, it can be determined that of the 20 switch transitions per period, 14 of them experience either zero current through the switch

or zero voltage across the switch during the transition. The switch voltage and current for each transition are displayed in Table 4-1.

Table 4-1 Switch voltage and current for switching transitions

Switch	Transition	v_{DS}	i_D
SW1H	Turn-on	$V_{HV}/3$	$i_{L,min}$
	Turn-off	$V_{HV}/3$	$i_{L,max}$
SW1L	Turn-on	0	N/A
	Turn-off	0	N/A
SW2H	Turn-on	0	N/A
	Turn-off	0	N/A
SW2L	Turn-on	$V_{HV}/3$	$i_{L,min}$
	Turn-off	$V_{HV}/3$	$i_{L,max}$
SW3H	Turn-on	N/A	0
	Turn-off	$V_{HV}/3$	$i_{L,max}$
SW3L	Turn-on	0	N/A
	Turn-off	N/A	0
SW4H	Turn-on	N/A	0
	Turn-off	N/A	0
SW4L	Turn-on	N/A	0
	Turn-off	N/A	0
SW5H	Turn-on	N/A	0
	Turn-off	0	N/A
SW5L	Turn-on	$V_{HV}/3$	$i_{L,min}$
	Turn-off	N/A	0

In the table, zero current and zero voltage transitions are grayed out. The parameter which is zero for those transitions is listed with a '0' while the corresponding voltage or current for that transition is listed as 'N/A.' After accounting for the zero voltage and zero current transitions, there are only six transitions that have non-zero current and voltage, three of which are turn-on with a current equal to the minimum inductor current and three of which are turn-off with a current equal to the maximum inductor current. All of six transitions have a voltage of $\frac{V_{HV}}{3}$ across the switch. Thus, the total turn-on and turn-off switching loss can be found by

$$P_{FET,turn-on\ total} = 3 \left[\frac{1}{2} \frac{V_{HV}}{3} i_{L,min} (t_{delay,on} + t_{rise}) f_{SW} \right] \quad (4-5)$$

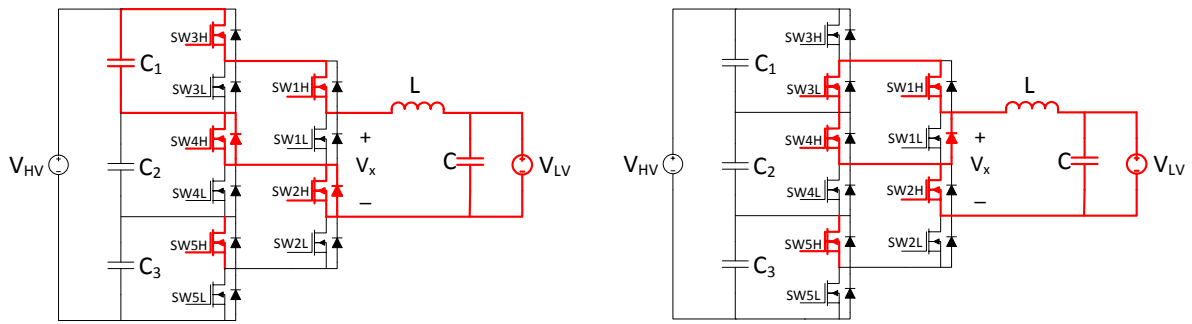
$$P_{FET,turn-off\ total} = 3 \left[\frac{1}{2} \frac{V_{HV}}{3} i_{L,max} (t_{delay,off} + t_{fall}) f_{SW} \right] \quad (4-6)$$

Summing (4-5) and (4-6), the total switching loss is found by

$$P_{FET,sw\ total} = \frac{V_{HV}}{2} f_{SW} [i_{L,min} (t_{delay,on} + t_{rise}) + i_{L,max} (t_{delay,off} + t_{fall})]. \quad (4-7)$$

4.2 Power MOSFET and diode conduction losses

The conduction loss calculations of the power MOSFET and diode are very dependent on the on resistance of the MOSFET, turn-on voltage of the anti-parallel diode, and operating point of the converter. Every conduction and transition state has at a minimum, a MOSFET conducting current from source to drain in which the body diode of that MOSFET may also be conduction current depending on whether the current through the on resistance of the MOSFET is sufficient to turn on the diode. For example, Figure 4-3(a) shows the inductor current being conducted through the MOSFET and body diode of SW2H and SW4H. There are also multiple states in which a diode is in parallel with three on MOSFETs. An example of this is conduction state 2 as shown in Figure 4-3(b). In the figure, if the current through the on resistance of SW4H, SW3L and SW1H creates a voltage large enough to turn on the body diode of SW1L, the inductor current will flow in both paths.



(a) Conduction State 1

(b) Conduction State 2

Figure 4-3 Examples of parallel MOSFET/diode paths

Since the MOSFET and diode parameters are known, it is certainly possible to derive conduction loss expressions taking into account the parallel paths. However, simulations taking into account the MOSFET on resistance, forward voltage drop of the diode and on resistance of the diode will be used to estimate the conduction losses. Simplified conduction losses expressions were derived that assumed the on resistance of the MOSFET and/or the current through the MOSFET was small enough that the parallel diode would not be turned on. Those derivations are shown in *Appendix A*.

This chapter details simulations of a four-level converter typology done in MATLAB/Simulink and PLECS. The component values and operating conditions of the simulation were based of the prototype converter that was built. Section 5.1 briefly details the simulation model that was used. Section 5.2 presents the simulations of ideal converter for both directions of power flow. Next, in Section 5.2.1 the major loss components of the MOSFET conduction loss, diode conduction loss, and snubber loss are added into the model and converter efficiency is observed over duty cycles from 20% to 80%.

5.1 Simulation model

The simulation model was built in MATLAB/Simulink with the use of the PLECS blockset. The basic PLECS circuit models for the four-level converter is shown Figure 5-1.

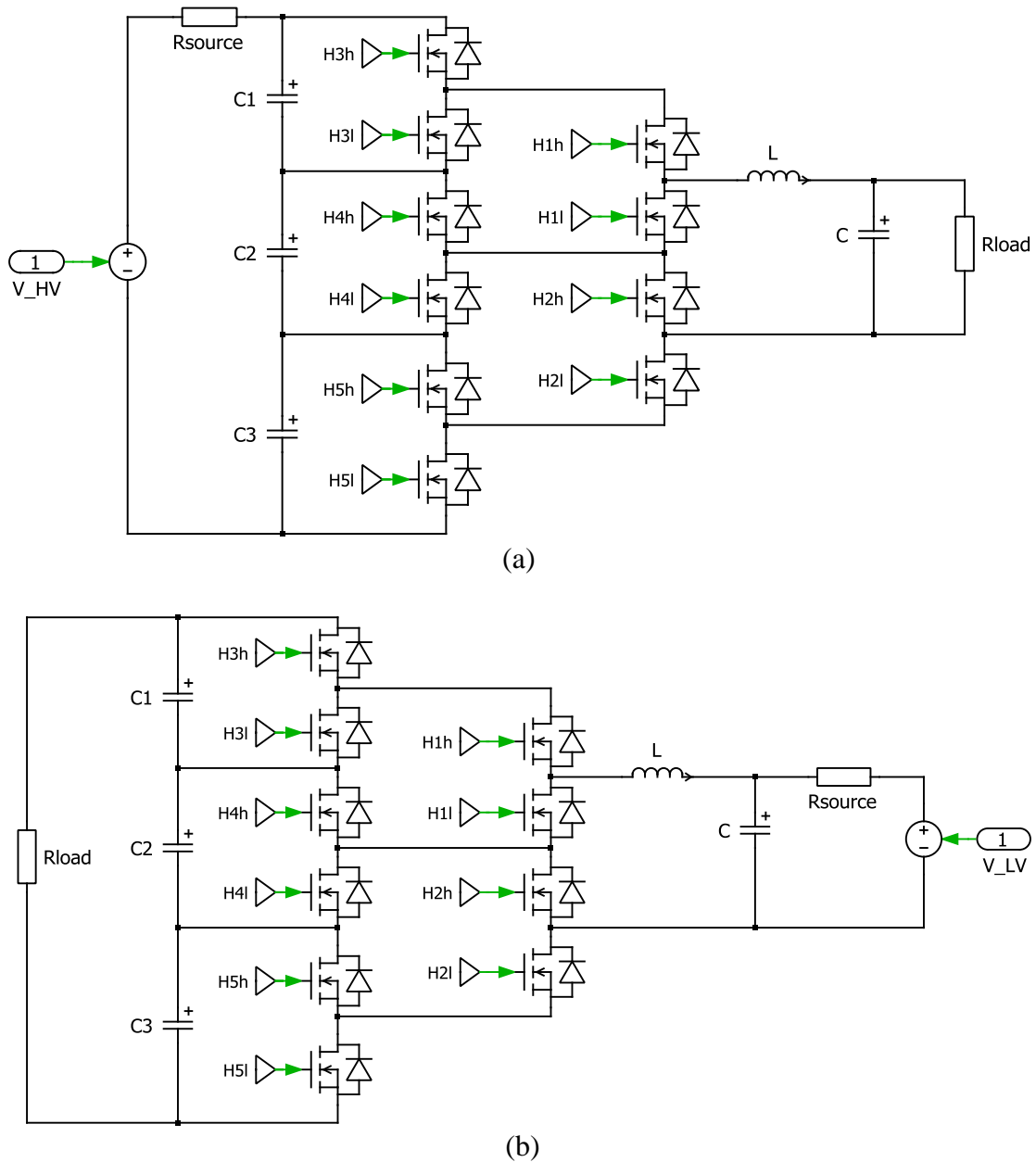


Figure 5-1 Four-level converter PLECS circuit model of the converter in (a) bucking operation and (b) boosting operation

The gate signals were generated by implementing a state machine into Simulink that was identical in function to the state machine outlined in Figure 2-15. The Simulink block diagrams for the gate signal generation as well as the MATLAB code used and more detailed versions of the PLECS circuit models used can be seen in *Appendix B*.

5.2 Ideal circuit simulations

Results of the simulation of the four-level converter with ideal components are presented here. Section 5.2.1 shows the results of the converter operating in bucking mode and Section 5.2.2 shows the results of the converter operating in boosting mode.

5.2.1 Bucking operation

The PLECS circuit model of the converter used to simulate the converter in bucking operation is shown in Figure 5-2.

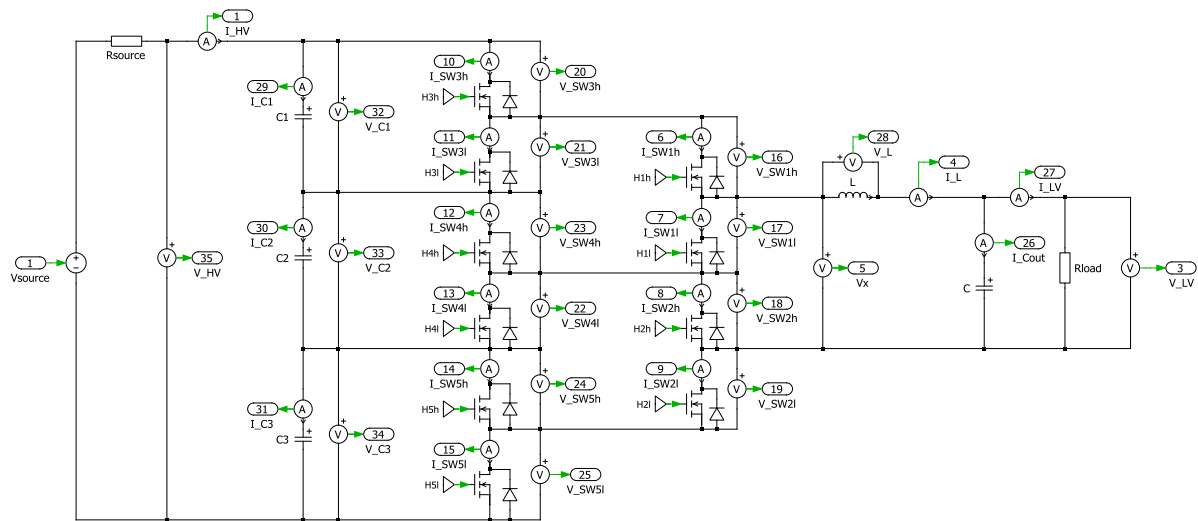


Figure 5-2 PLECS model used for ideal simulation of the four-level converter in bucking operation

Notice that a non-ideal source resistance is included but the high voltage side voltage measurement is made after the source resistance. The simulation results for the converter simulated at $d=25\%$, 50% and 75% with a constant resistance load of $10\ \Omega$ will be shown. The $10\ \Omega$ load was used as that was also used with the actual hardware. The parameters used in the ideal simulation are shown in Table 5-1.

Table 5-1 Simulation parameters for ideal four-level converter in bucking operation

Input Voltage	225 V
Switching Frequency	10kHz
R_{Source}	50 m Ω
R_{Load}	10 Ω
L	330 μ H
$C_1, C_2,$ and C_3	470 μ F
C	100 μ F
Dead time	0 s
MOSFET $R_{DS,on}$	0 Ω
Diode V_F	0 V

The gate signals of the ideal converter operating with a duty ratio, d , of 75% are shown in Figure 5-3.

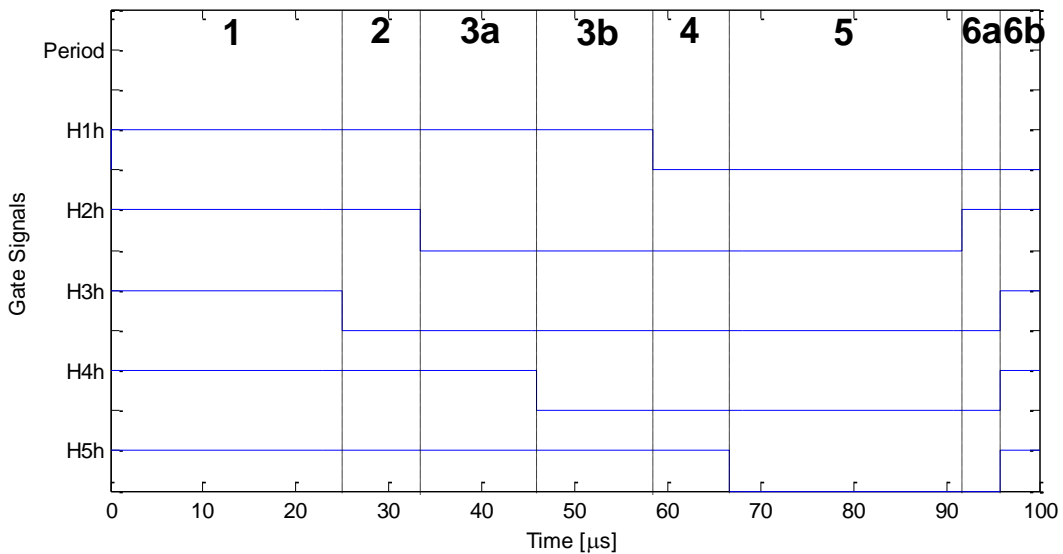


Figure 5-3 Simulation gate signals for 75% duty cycle

The figure displays only the high side gate signals for each half bridge as the dead time is zero so the low side gate signals are simply the inverse of those shown in the figure. With the overall duty cycle of 75%, the converter is in conduction states 1, 3a/3b and 5 for 25 μ s and in conduction states 2, 4, and 6a/6b for 8.33 μ s, as calculated by (2-1) and (2-2),

respectively. The gate signals along with the inductor voltage, dividing capacitor, and output voltages and currents are plotted for two periods in Figure 5-4.

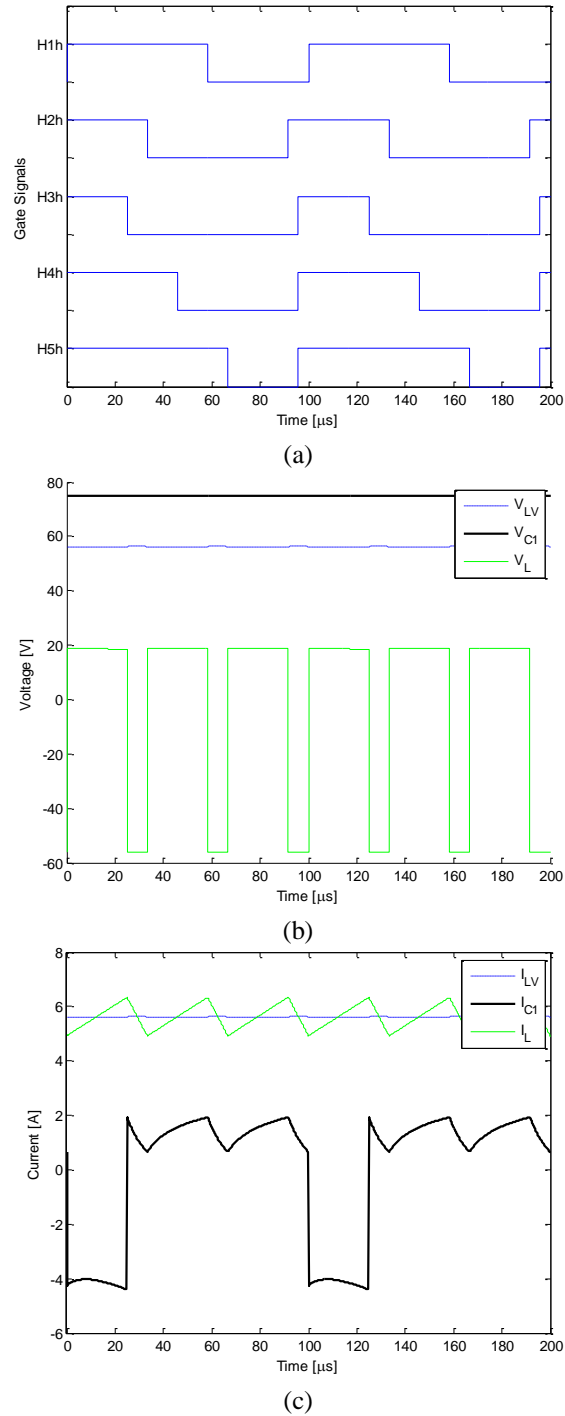


Figure 5-4 Simulation waveforms for the ideal four-level converter in bucking operation for $d = 75\%$, $V_{HV} = 225 \text{ V}$ and $R_{Load} = 10 \Omega$

In Figure 5-4(a), the low side voltage is 56.24 V with a peak-to-peak ripple of 0.06 V. This corresponds to a transformation ratio of 0.25. Notice that the inductor waveforms are at three times the switching frequency. In Figure 5-4(b), it can be seen that the capacitor C_1 only delivers energy during 25% of the switching period. The simulation was repeated for duty cycles of 50% and 25% and the waveforms for the 50% and 75% simulations are shown in Figure 5-5 and Figure 5-6, respectively.

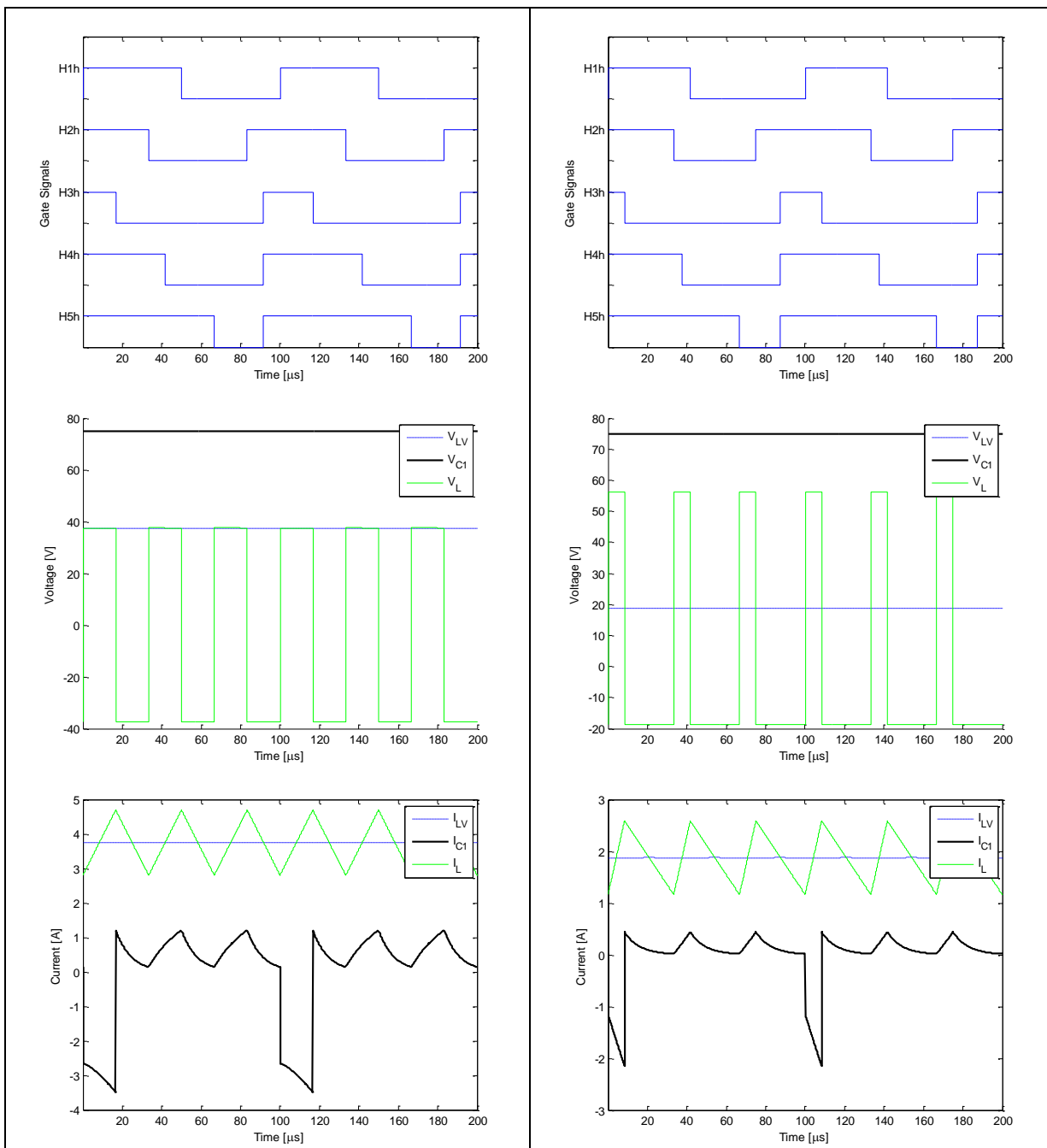


Figure 5-5 Simulation waveforms for the ideal four-level converter in bucking operation for $d=50\%$, $V_{HV} = 225$ V and $R_{Load} = 10\Omega$

Figure 5-6 Simulation waveforms for the ideal four-level converter in bucking operation for $d=25\%$, $V_{HV} = 225$ V and $R_{Load} = 10\Omega$

The low side voltage for the 50% and 25% simulations were 37.5 V and 18.75 V, respectively. Table 5-2 displays a summary of the simulation results.

Table 5-2 Four-level converter bucking operation simulated results for
 $V_{HV}=225\text{ V}$ and $R_{Load}=10\Omega$

Duty	V_{HV} [V _{RMS}]	V_{LV} [V _{RMS}]	ΔV_{LV} [V _{pk-pk}]	i_{LV} [A _{RMS}]	P_{out} [W]	$\frac{\langle V_{LV} \rangle}{\langle V_{HV} \rangle}$	$\Delta i_{C1,rms}$ [A _{RMS}]	$\Delta i_{C,rms}$ [A _{RMS}]	$i_{L,RMS}$ [A _{RMS}]	Δi_L [A _{pk-pk}]
25%	225.0	18.75	0.059	1.87	35.06	0.083	0.52	0.42	1.92	1.42
50%	225.0	37.50	0.079	3.75	140.6	0.167	1.37	0.55	3.79	1.90
75%	224.9	56.24	0.060	5.62	316.2	0.250	2.40	0.42	5.64	1.43

Next, simulation results will be shown of the ideal circuit with all the same component values and operation conditions shown in Table 5-1 with the exception that instead of zero dead time, $1.25\ \mu\text{s}$ was used. The gate signals and conduction periods for d equal to 75% are shown in Figure 5-7.

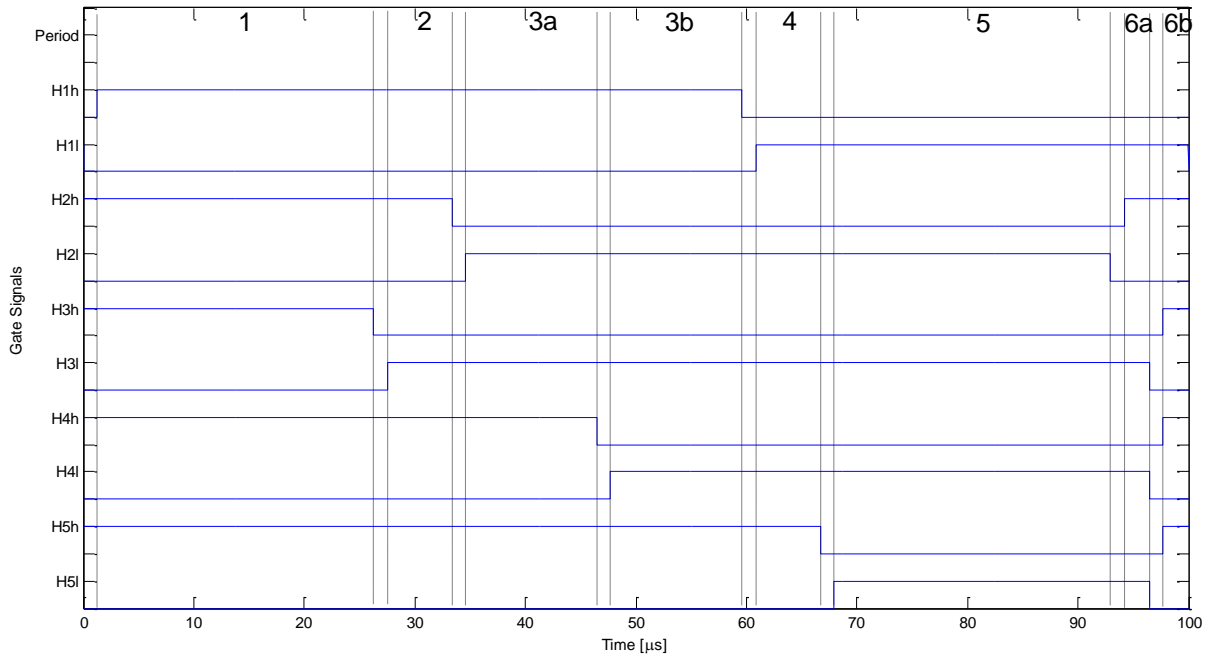


Figure 5-7 Simulation gate signals for 75% duty cycle with a $1.25\ \mu\text{s}$ dead time

The gate signal, switch current and switch voltage for SW5H and SW5L are shown in Figure 5-8.

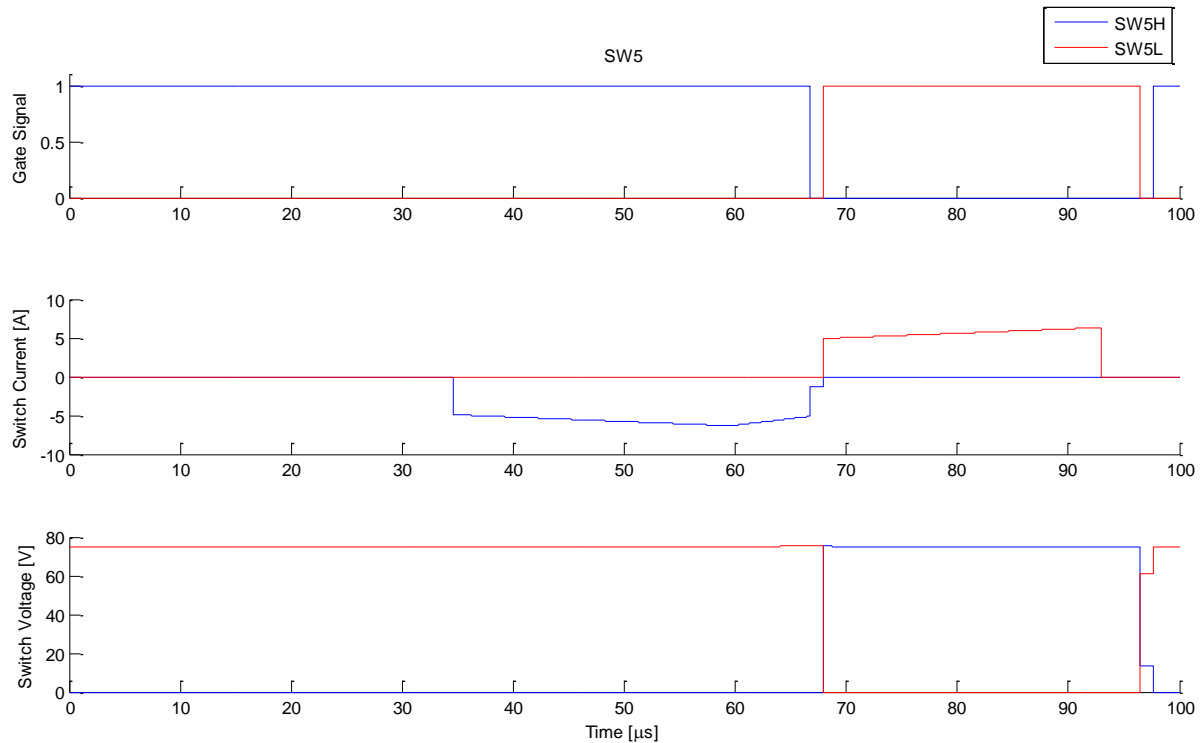


Figure 5-8 SW5H and SW5L gate signal, switch current and switch voltage

The switch SW5H turns off at the 66.6 μs mark. During the 1.25 μs dead time following the turn off, the switch voltage remains at zero and become 75 V when SW5L turns on following the dead time. Looking at the SW5L turn off and SW5H turn on transitions, it can be seen that the current through both switches is zero during those transitions. Thus, the simulation confirms that SW5L experiences zero current during its turn-off transition, SW5H experiences zero current during its turn-on transition, and SW5H experiences zero voltage during its turn-off transition. Note that the switch current plotted in the figure corresponds to the current through both the MOSFET and body diode of the switch. Thus, the current in SW5H during the dead time between the SW5H turn-off and

SW5L turn-on beginning at time equal to $66.6 \mu\text{s}$ is the body diode current. The switch voltage and current plots for the remaining switches are shown in Figure 5-9 through Figure 5-12.

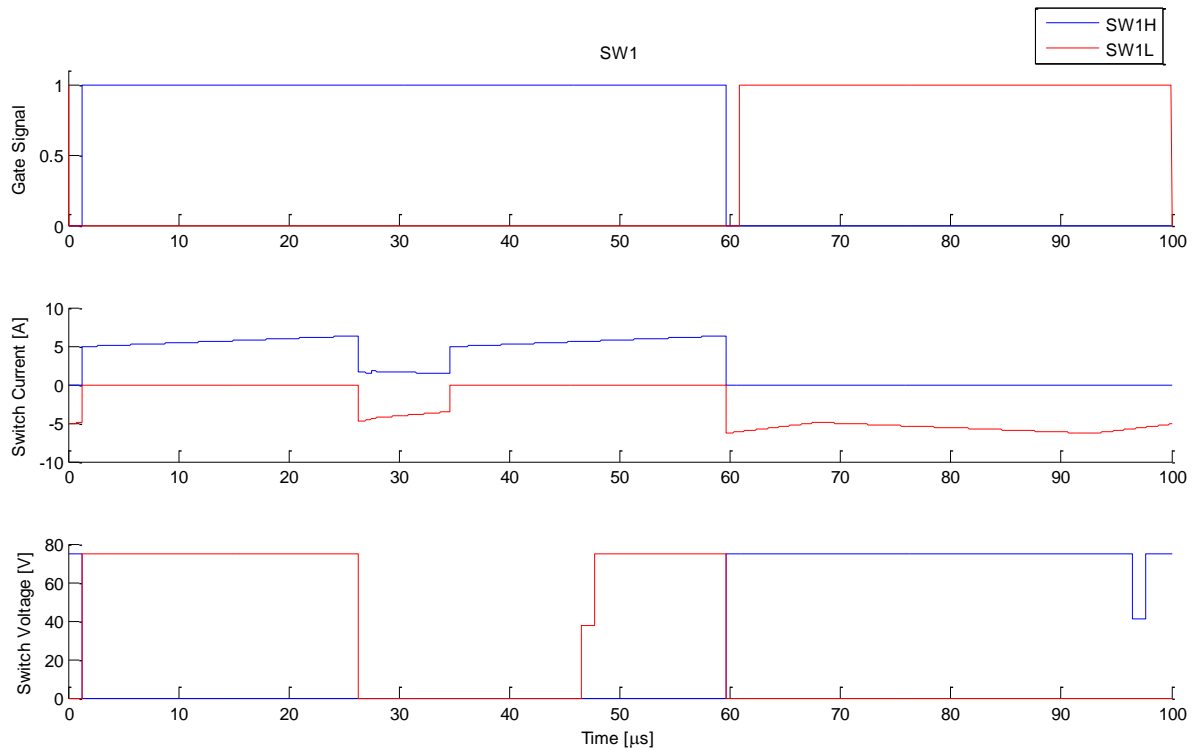


Figure 5-9 SW1H and SW1L gate signal, switch current and switch voltage

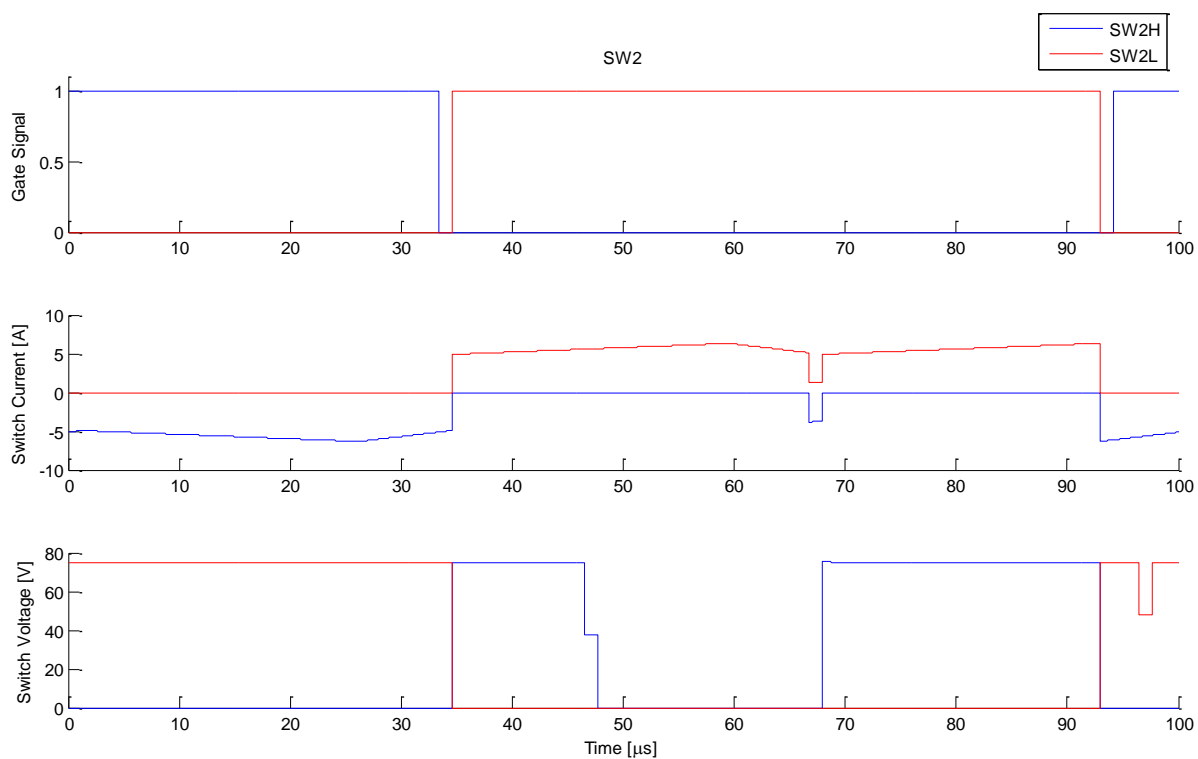


Figure 5-10 SW2H and SW2L gate signal, switch current and switch voltage

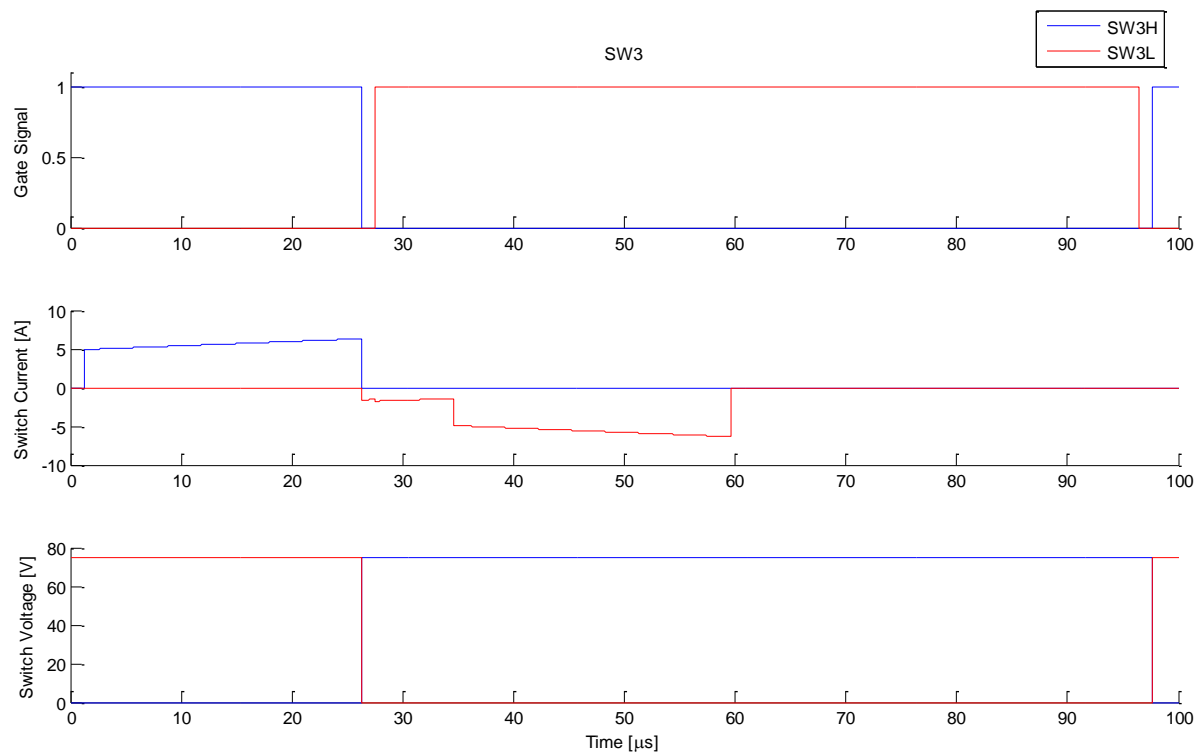


Figure 5-11 SW3H and SW3L gate signal, switch current and switch voltage

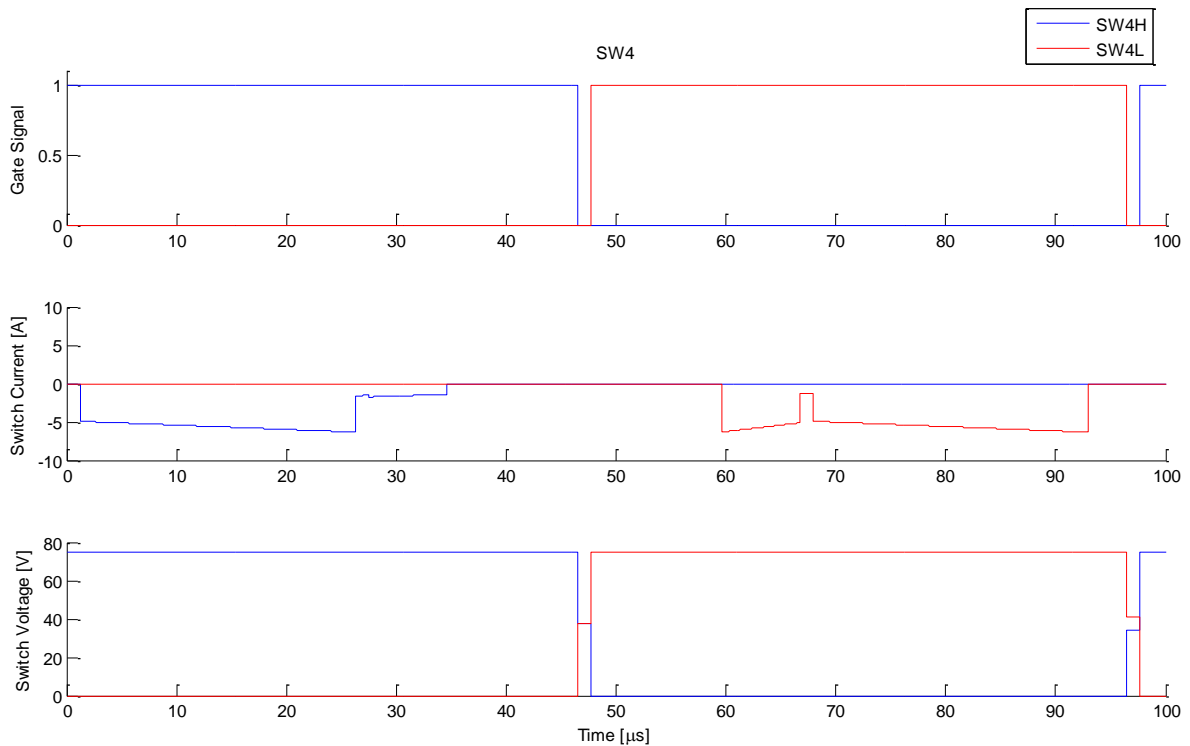


Figure 5-12 SW4H and SW4L gate signal, switch current and switch voltage

From the figures, the 14 zero voltage or zero current transitions in Table 4-1 can be verified. Also, notice that the maximum voltage stress for all switches is in fact 75 V or $\frac{V_{HV}}{3}$.

5.2.2 Boosting operation

The PLECS circuit model of the converter used to simulate the converter with power flow in the opposite direction of the power flow in Section 5.2.1 is shown in Figure 5-13. Notice the direction of current and voltage meters for the high voltage side current, low voltage side current, inductor voltage and inductor current have been flipped from the bucking mode of operation simulation circuit.

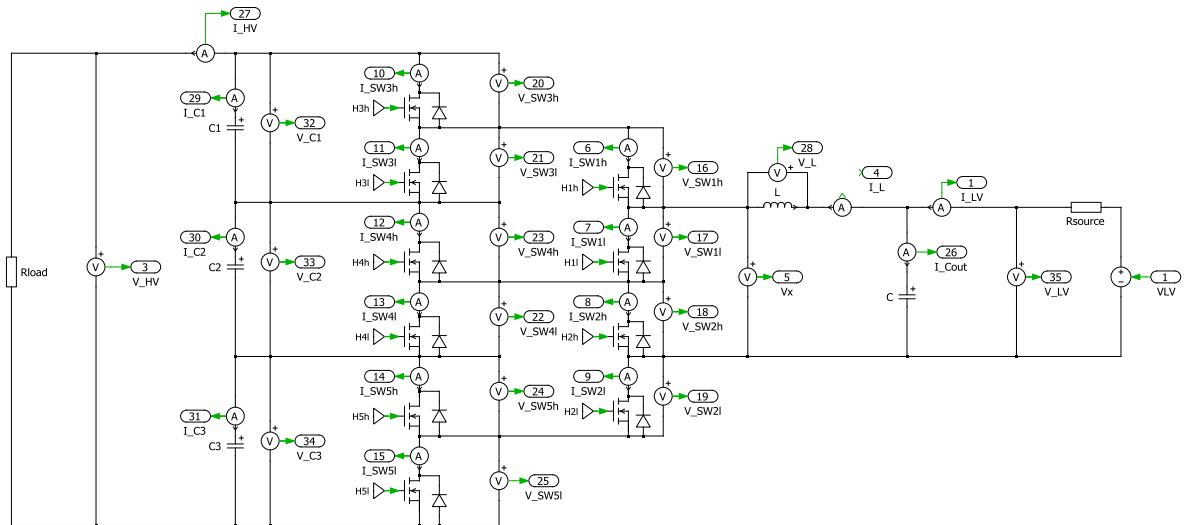


Figure 5-13 PLECS model used for ideal simulation of the four-level converter in boosting operation

The converter was simulated at $d=25\%$, 50% and 75% with a constant resistance load of 250Ω with the same capacitor and inductor values as the bucking mode simulations and a V_{LV} of 24 V. A list of the component values and parameters used in the simulation are shown in Table 5-3.

Table 5-3 Simulation parameters for ideal four-level converter in boosting operation

Input Voltage	24 V
Switching Frequency	10kHz
R_{Source}	5 m Ω
R_{Load}	250 Ω
L	330 μ H
C_1 , C_2 , and C_3	470 μ F
C	100 μ F
Dead time	0 s
MOSFET $R_{DS,on}$	0 Ω
Diode V_F	0 V

The simulation waveforms for the converter operating with a 75% duty cycle are shown in Figure 5-14.

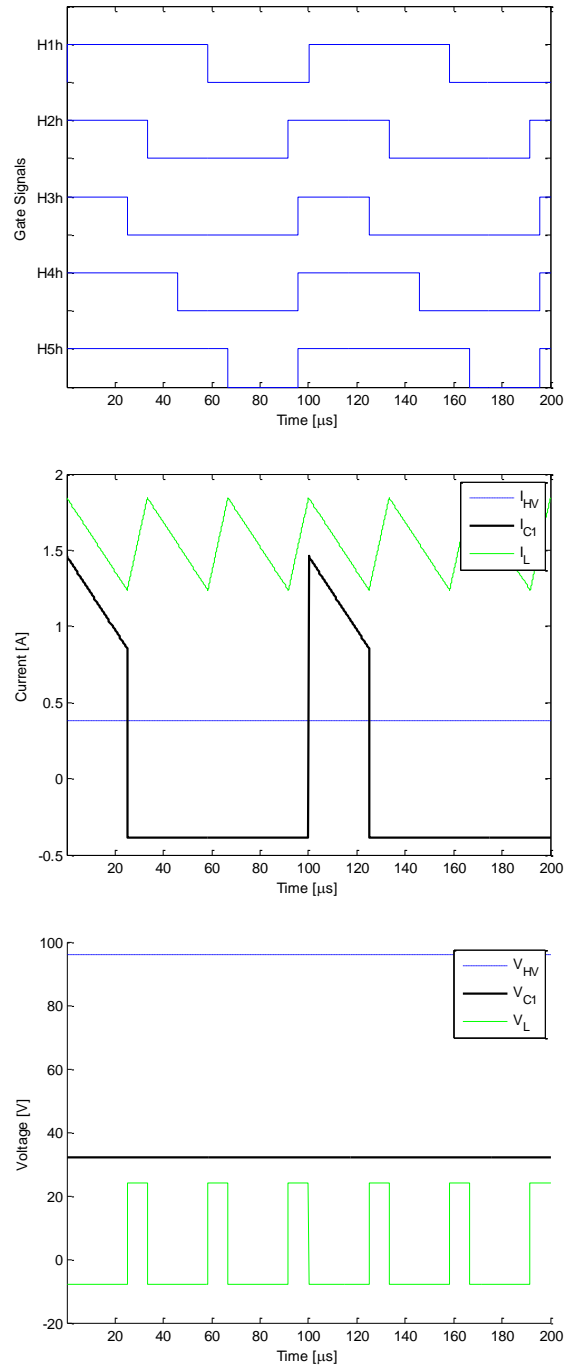


Figure 5-14 Simulation waveforms for the ideal four-level converter in boosting operation for $d = 50\%$, $V_{LV} = 24 \text{ V}$ and $R_{Load} = 250\Omega$

In the figure, with the 24 V input and 75% duty cycle, the output voltage is 96 V. The inductor waveforms again have a frequency of three times the switching frequency. Since the

duty cycle is defined the same in boosting and bucking operation and there is no dead time, the gate signals of Figure 5-14 are identical to the gate signals for the converter in bucking mode of operation with a duty cycle of 75% shown in Figure 5-4. The simulation waveforms of the converter with duty cycles of 50% and 25% are shown in Figure 5-15 and Figure 5-16, respectively.

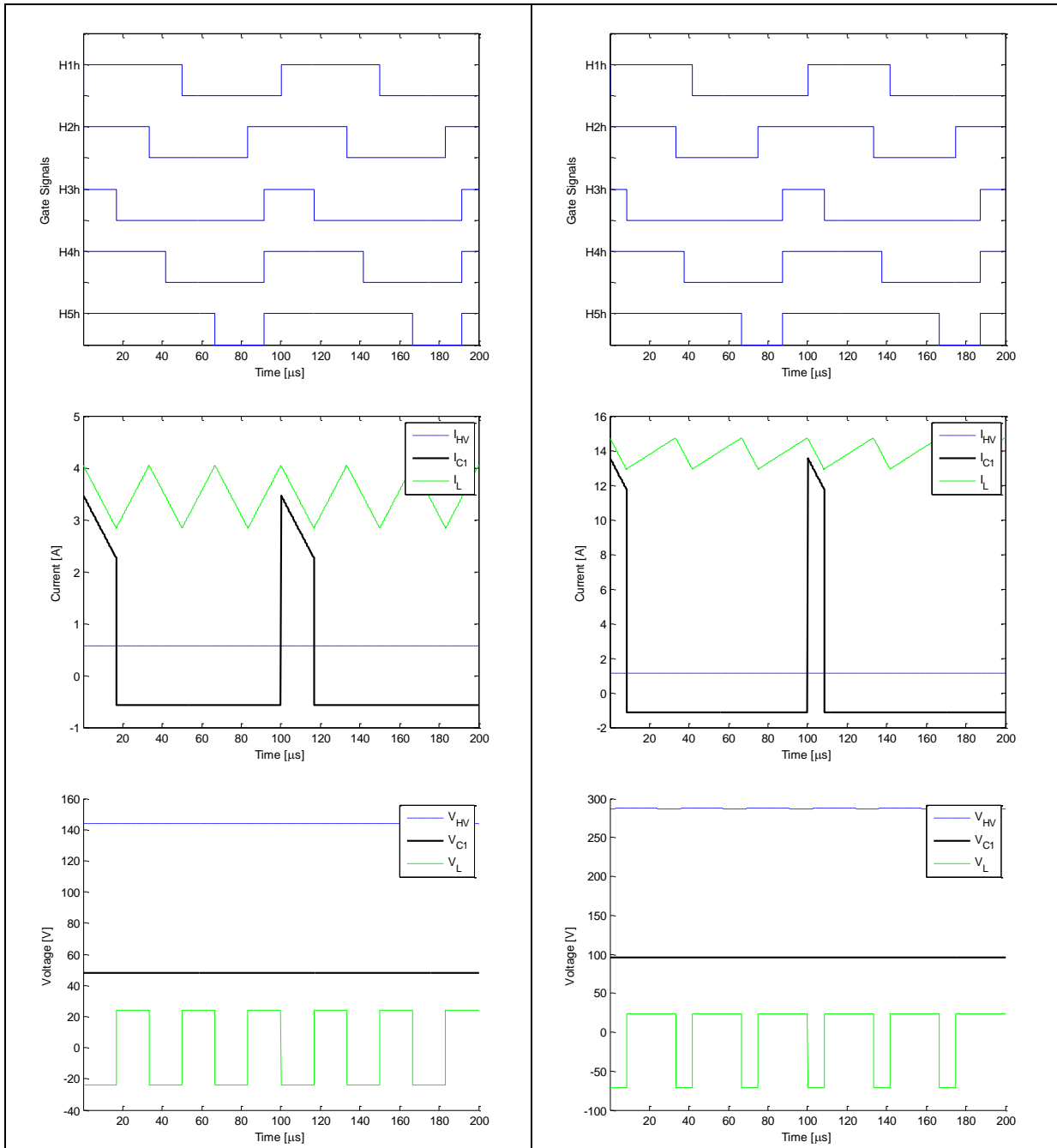


Figure 5-15 Simulation waveforms for the ideal four-level converter in boosting operation for $d=50\%$, $V_{LV} = 24\text{ V}$ and $R_{Load} = 250\Omega$

Figure 5-16 Simulation waveforms for the ideal four-level converter in boosting operation for $d=25\%$, $V_{HV} = 24\text{ V}$ and $R_{Load} = 250\Omega$

The output voltage for the 50% and 25% simulations were 143.9 V and 287.2 V, respectively. The theoretical values for a V_{LV} of 24 V are 144 V and 288 V. The deviation

from those theoretical values is caused by the non-zero source resistance. Table 5-2 displays a summary of the simulation results of the converter in boosting operation.

Table 5-4 Four-level converter boosting operation simulated results for $V_{LV}=24$ V and $R_{Load}=250\Omega$

Duty	V_{LV} [V _{RMS}]	V_{HV} [V _{RMS}]	ΔV_{HV} [V _{pk-pk}]	$\frac{\langle V_{LV} \rangle}{\langle V_{HV} \rangle}$	$\Delta i_{C1,rms}$ [A _{RMS}]	$\Delta i_{C,rms}$ [A _{RMS}]	$i_{L,RMS}$ [A _{RMS}]	Δi_L [A _{pk-pk}]	i_{HV} [A _{RMS}]	P_{out} [W]
25%	23.93	287.2	0.187	0.083	3.86	0.061	13.83	1.81	1.15	329.8
50%	23.98	143.9	0.063	0.16	1.29	0.035	3.46	1.21	0.58	82.8
75%	24.0	95.96	0.022	0.25	0.67	0.020	1.55	0.607	0.38	36.8

5.3 Non-ideal simulations

The four-level converter was simulated in bucking operation with a PLECS model that included the MOSFET $R_{DS,on}$, the forward voltage drop and series resistance of the body diode, and the RCD snubber circuitry. The parameters of those components and the simulation parameters used for these non-ideal simulations are shown in Table 5-5 and the PLECS circuit model is shown in Figure 5-17.

Table 5-5 Simulation parameters for non-ideal four-level converter in bucking operation

Input Voltage	225 V
Switching Frequency	10kHz
R_{Source}	50 m Ω
R_{Load}	10 Ω
L	330 μ H
$C_1, C_2,$ and C_3	470 μ F
C	100 μ F
Dead time	1.25 μ s
MOSFET $R_{DS,on}$	130 m Ω
Diode Forward Voltage	0.69 V
Diode Series Resistance	14.3 m Ω
Snubber Diode Forward Voltage	0.925 V
Snubber Diode Series Resistance	50 m Ω
Snubber Resistance	6.2 Ω

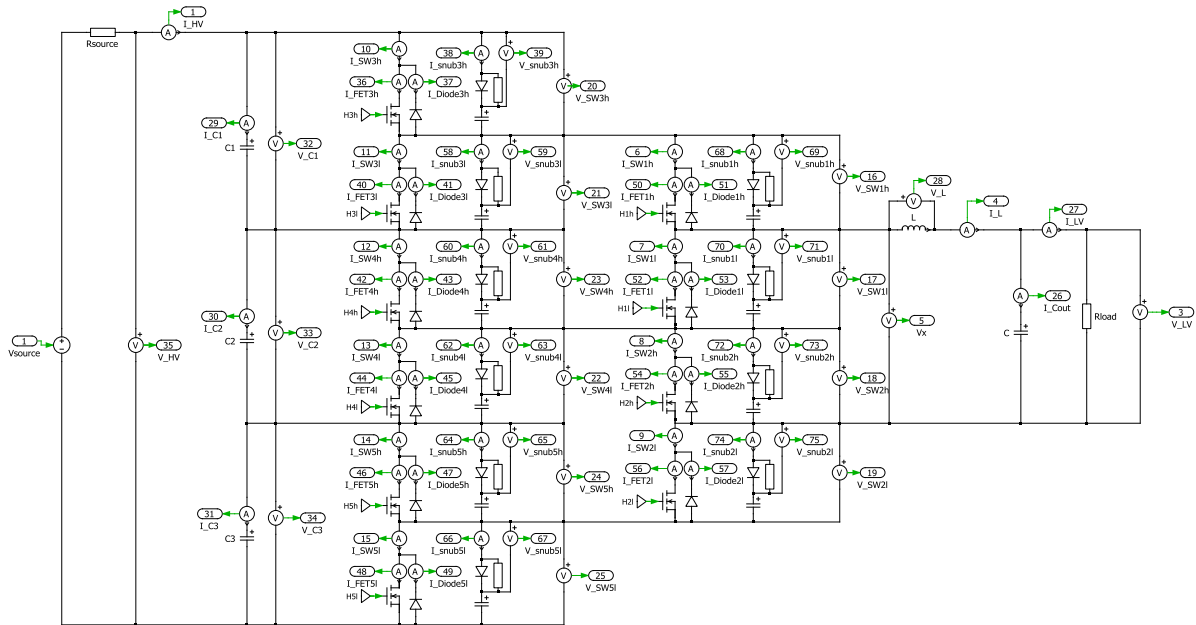


Figure 5-17 PLECS model used for non-ideal simulations of the four-level converter in bucking operation

The simulated results for duty cycles in the range of 20% to 80% are shown in Table 5-6.

Table 5-6 Simulation results including MOSFET conduction, diode forward voltage and conduction losses, and snubber losses

Duty Cycle	Input Voltage [V]	Input Current [A]	Input Power [W]	Output Voltage [V]	Output Current [A]	Output Power [W]	Calculated Switching Loss [W]	Total Losses [W]	Efficiency
20%	225.0	0.14	30.7	15.3	1.53	23.4	0.59	7.9	74.9%
35%	225.0	0.33	75.2	25.8	2.58	66.3	0.98	9.8	87.1%
50%	225.0	0.64	143.9	36.4	3.64	132.6	1.37	12.6	91.3%
65%	224.9	1.05	236.8	47.1	4.71	221.7	1.76	16.9	92.9%
80%	224.9	1.57	353.3	57.8	5.78	333.7	2.14	21.7	93.9%

In the table, the input and output voltage, current and power are the simulated values. Since the PLECS model does not take into account the switching losses, the switching loss was calculated from Eqn. (4-7) using the voltage and current values from the simulation. The total losses column in the table is the sum of the calculated switching losses and the

difference of the simulation input and output powers which include losses of the conduction losses of the power MOSFET, conduction losses of the power diode and the conduction losses in the snubber resistor and snubber diode. As seen in the table, the efficiency ranges from 74.9% at the 20% duty cycle to 93.9% at the 80% duty cycle.

The converter efficiency could be greatly improved. For one, the poor efficiency at the low load is mostly due to the snubber circuitry. Repeating the simulations with just the snubber circuitry removed, a ~6 W improvement in power losses was achieved across the duty cycle range. At the 20% duty cycle, that accounts for ~75% of the losses. A second major improvement in the converter efficiency could come from using a MOSFET with lower voltage rating to take advantage of better conduction and switching loss characteristics. For example, consider the IRFB4115PbF 150 V N-Channel MOSFET by International Rectifier with parameters shown in Table 5-7.

Table 5-7 IRFB4115PbF N-channel MOSFET specifications [11]

Maximum V_{DS}	150 V
Maximum I_D	104 A
Max $R_{DS,on}$	11 m Ω
Typical Turn-On Delay Time	18 ns
Typical Turn-On Rise Time	73 ns
Typical Turn-Off Delay Time	41 ns
Typical Turn-Off Fall Time	39 ns
Maximum Continuous Diode Forward Current	104 A
Diode Forward Voltage	0.6 V
Estimated $R_{D,on}$	16.6 m Ω

The simulations for duty cycle from 20% to 80% were repeated using the parameters of the IRFB4115PbF MOSFET and with the snubber circuitry still removed. The results of the simulations are shown in Table 5-8.

Table 5-8 Simulation results without RCD snubbers and with 150 V rated MOSFETs

Duty Cycle	Input Voltage [V]	Input Current [A]	Input Power [W]	Output Voltage [V]	Output Current [A]	Output Power [W]	Calculated Switching Loss [W]	Total Losses [W]	Efficiency
20%	225.0	0.10	22.4	14.9	1.49	22.2	0.28	0.44	98.1%
35%	225.0	0.30	68.5	26.1	2.61	68.1	0.49	0.87	98.7%
50%	225.0	0.62	139.9	37.3	3.73	139.1	0.71	1.45	99.0%
65%	224.9	1.05	236.3	48.5	4.85	235.2	0.92	2.08	99.1%
80%	224.9	1.59	357.9	59.7	5.97	356.1	1.14	2.86	99.2%

Figure 5-18 shows a plot of the efficiency versus duty cycle for all three cases.

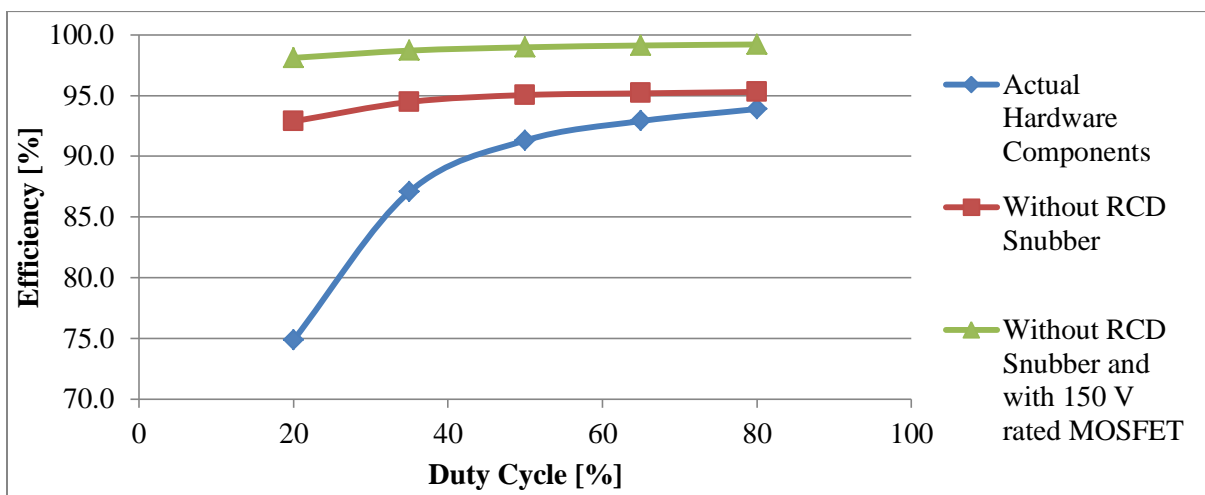


Figure 5-18 Efficiency vs. duty cycle for the three simulation cases with a constant load of 10Ω

Obviously as the major loss mechanisms of the currently designed board are minimized, a number of other losses become significant. However, these results do show that significant efficiency improvements to the current design are possible and that the efficiency numbers of the current design are not reflective of what is possible with this typology.

Chapter 6 Experimental results and analysis

This chapter presents the experimental results that were obtained with the prototype converter. Section 6.1 displays the results of the prototype converter for a 225 V input and 10 Ω load and compares those results with the simulation results from Chapter 5. In section 6.2, results of the prototype converter for a number of different input voltages and load conditions are shown. Finally, section 6.3 presents the imbalance in the divider capacitor voltages that was seen in the prototype testing and the results obtained by implementing open loop control of d_1 , d_2 and d_3 .

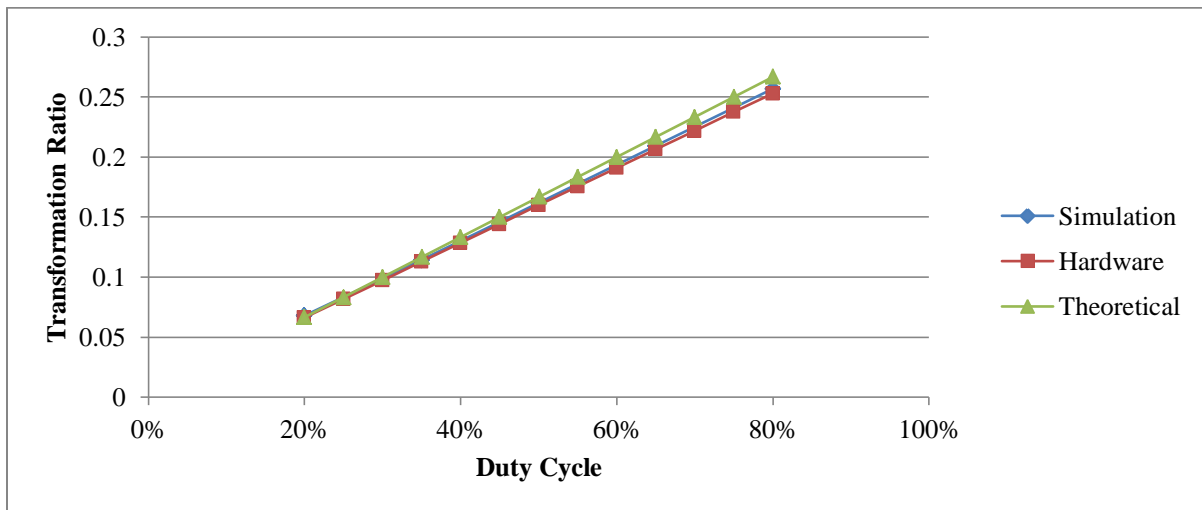
6.1 Hardware versus simulation results

With a high voltage input of 225 V, a nominally 10 Ω resistive load was used for the low voltage load of the hardware as the duty cycle was varied in 5% increments from 20% to 80%. Table 6-1 displays the input and output measured values.

Table 6-1 Hardware input and output data for 225 V input and 10 Ω load

Duty Cycle	Input Voltage [V]	Input Current [A]	Input Power [W]	Output Voltage [V]	Output Current [A]	Output Power [W]	Converter Efficiency
20.0%	225.4	0.15	32.7	15.0	1.56	23.3	71.3%
25.0%	225.1	0.20	45.9	18.4	1.92	35.2	76.7%
30.0%	225.1	0.28	61.9	21.9	2.28	49.8	80.5%
35.0%	225.1	0.36	81.0	25.4	2.65	67.3	83.0%
40.0%	225.1	0.46	102.6	28.9	3.01	87.1	84.9%
45.0%	225.1	0.56	126.9	32.4	3.38	109.5	86.3%
50.1%	225.1	0.69	154.2	36.0	3.75	135.0	87.6%
55.0%	225.3	0.82	183.8	39.5	4.11	162.5	88.4%
60.0%	225.1	0.96	215.7	43.0	4.47	192.2	89.1%
65.0%	225.2	1.11	250.6	46.5	4.84	225.0	89.8%
70.0%	225.1	1.28	287.9	49.9	5.19	259.1	90.0%
75.1%	225.1	1.46	328.6	53.5	5.56	297.3	90.5%
80.0%	225.1	1.65	371.2	56.9	5.92	337.0	90.8%

The transformation ratio versus duty cycle is plotted in Figure 6-1 for the hardware results as well as the simulation results and theoretical values.

Figure 6-1 Transformation ratio versus duty cycle for 225 V input and 10 Ω load

The hardware transformation ratio corresponds well with the theoretical values and simulation results. There is noticeable deviation of the hardware transformation ratio from

the theoretical at the higher duty cycles due to the converter losses. The efficiency of the hardware is plotted, along with the simulated efficiency, versus duty cycle in Figure 6-2 and versus output power in Figure 6-3.

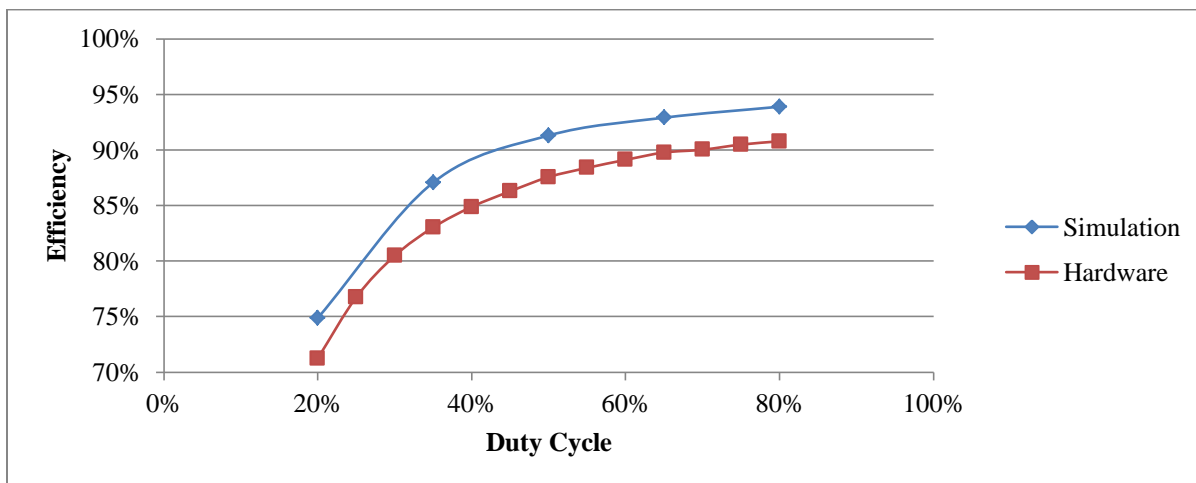


Figure 6-2 Hardware and simulated efficiency versus duty cycle for a 225 V input and 10 Ω load

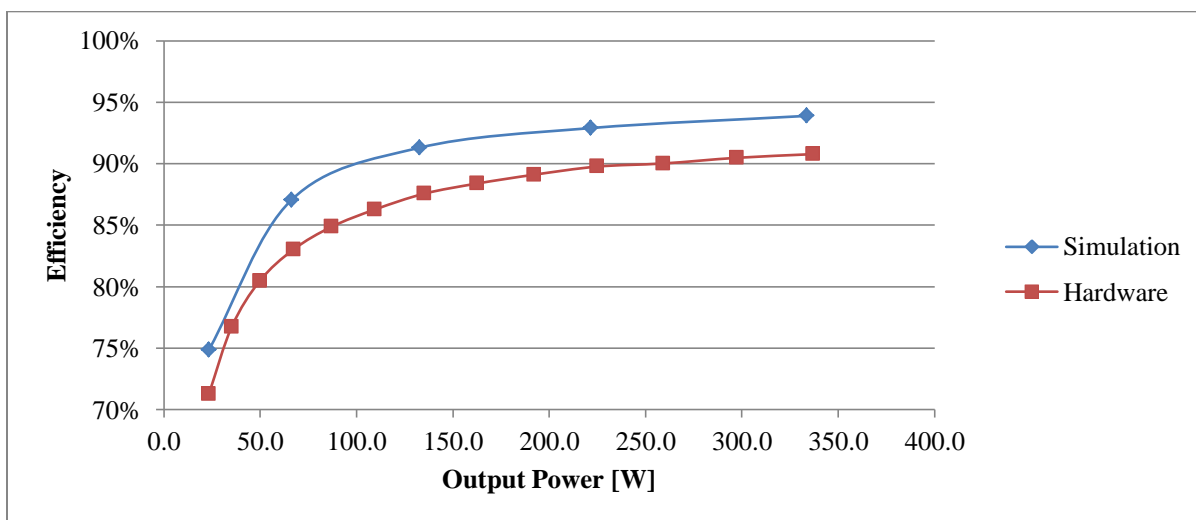


Figure 6-3 Hardware and simulated efficiency versus output power for a 225 V input and 10 Ω load

The curve of the simulated efficiency has the same general shape as the hardware efficiency but the hardware roughly 3%-5% less efficient at all points. However, the

simulations only accounted for the snubber loss, the MOSFET and body diode conduction losses and the switching losses. Other losses including any inductor losses or capacitor losses were not taken into account.

6.2 Other input voltages and load conditions

Hardware test data was taken for the converter under five other input voltage and load conditions: 75 V input and 10 Ω load, 75 V input and 5 Ω load, 150 V input and 10 Ω load, 150 V input and 5 Ω load, and 225 V input and 20 Ω load. The transformation ratio curve for all conditions is shown in Figure 6-4.

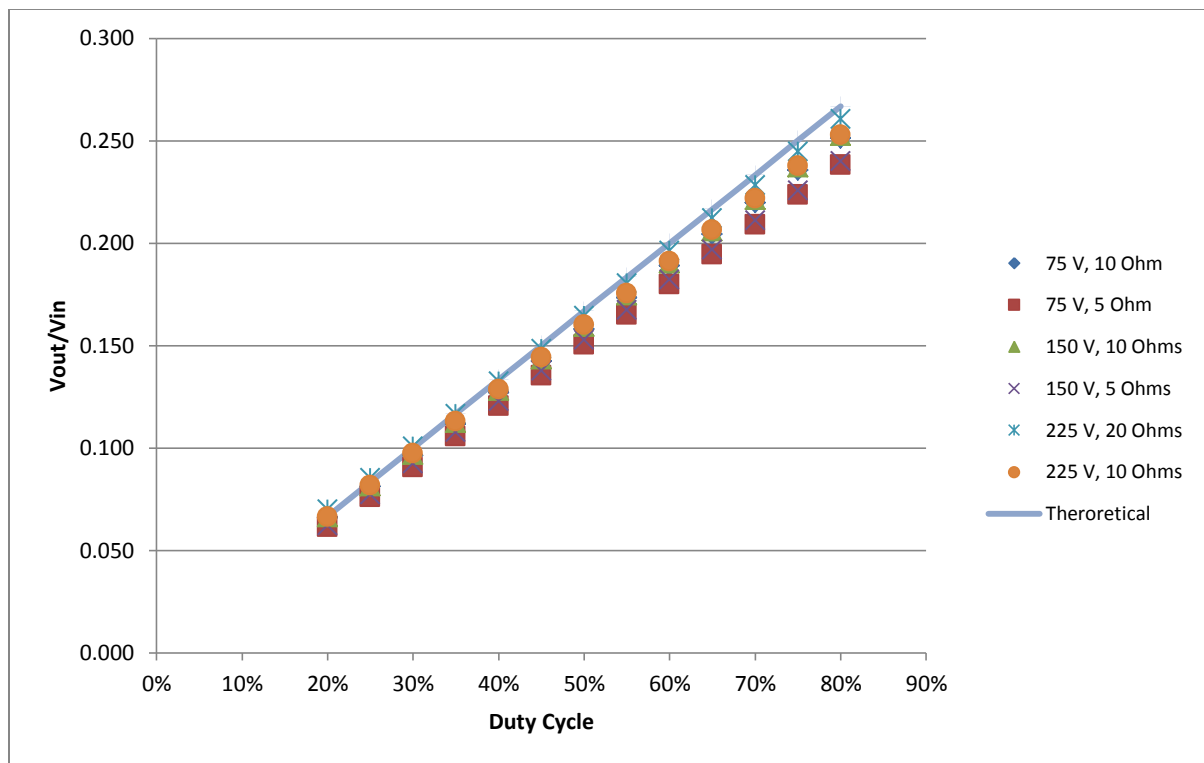


Figure 6-4 Transformation ratio versus duty cycle for all input and load conditions

Again the hardware results corresponded fairly well with the theoretical transformation ratio. The 75 V input and 5 Ω load had the greatest percent error from the

theoretical values with a 10.8% percent error at the 80% duty cycle while the 225 V input and 20 Ω load best paralleled the theoretical curve with an error of 2.3% at the 80% duty cycle. The plots of the efficiency versus duty cycle and versus output power are shown in Figure 6-5 and Figure 6-6, respectively.

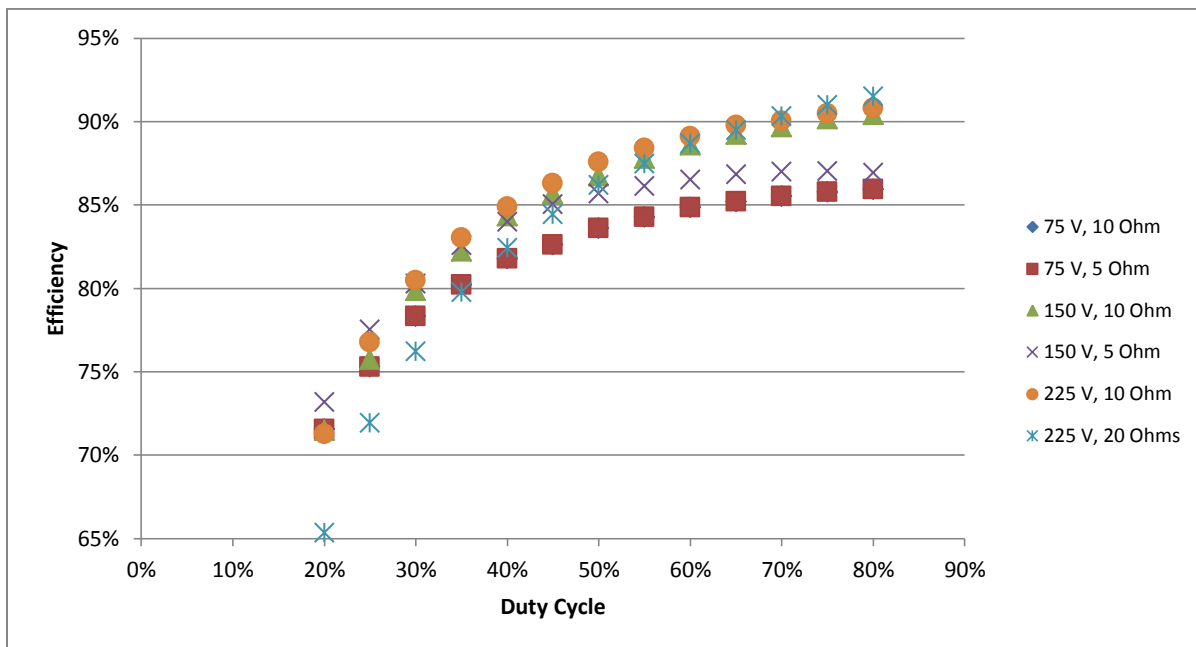


Figure 6-5 Efficiency versus duty cycle for all input and load conditions

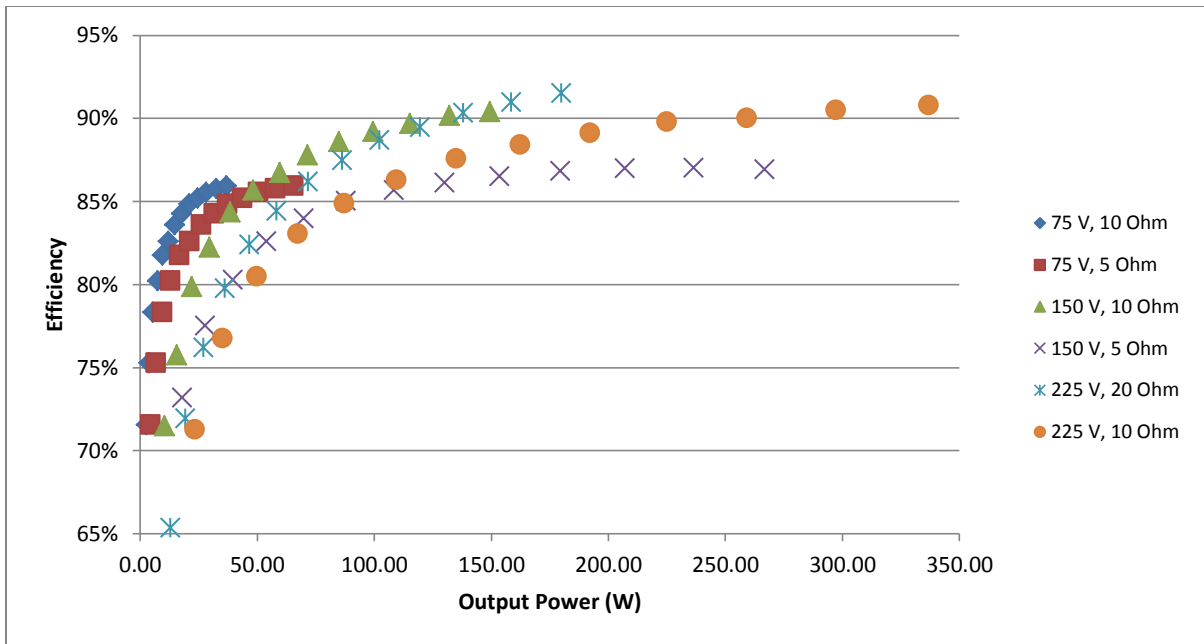


Figure 6-6 Efficiency versus output power for all input and load conditions

The peak efficiency of all the conditions tested was 91.5% at the 225 V input, 20 Ω load and 80% duty cycle in which the output power was 180 W. For all tests, the efficiency increased with duty cycle. However, with the constant resistance loads, the low duty cycles correspond to low power outputs and as was previously shown in simulation results that the low efficiency at low power levels was mainly due to the snubber circuitry losses.

6.3 Imbalance of divider capacitor voltages

It was observed throughout the testing of the hardware that the divider capacitor voltages experienced significant imbalance at times. Oscilloscope screen shots showing the inductor current and capacitor voltages for an input voltage of 225 V, load of 10 Ω and for duty cycles of 20%, 50% and 80% are shown in Figure 6-7.

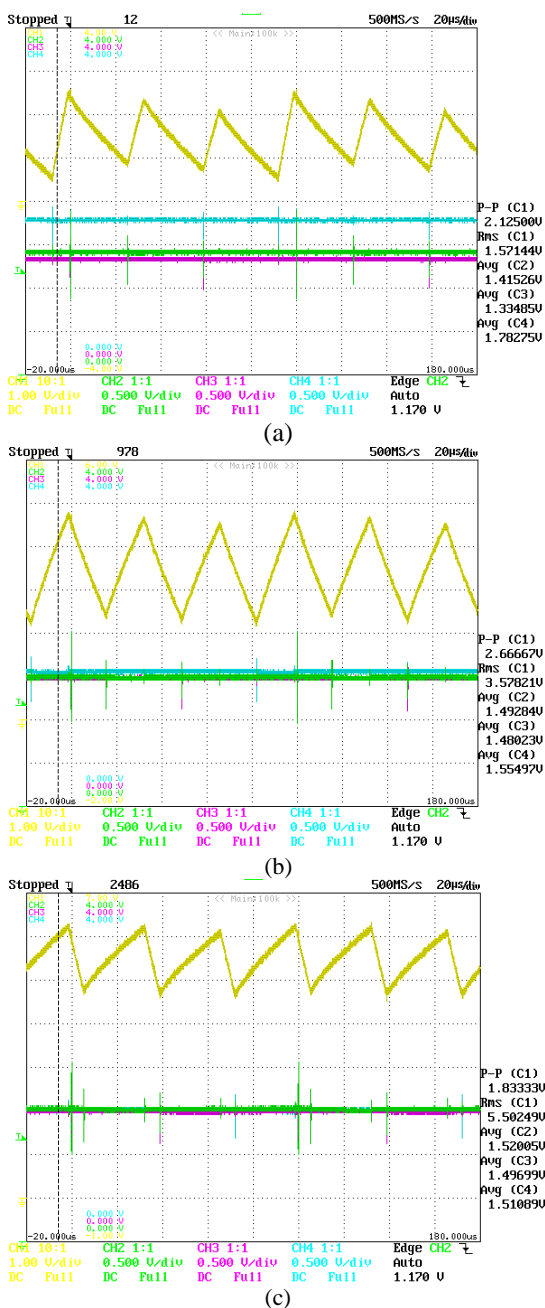


Figure 6-7 Oscilloscope screen shots showing the inductor current (CH 1), and voltages of C_1 (CH 2), C_2 (CH 3) and C_3 (CH 4) for duty cycles of (a) 20%, (b) 50% and (c) 80%

The proper scaling for the capacitor voltages in the figures is 50:1, such that one 0.5 V division corresponds to an actual voltage of 25 V. It is easily observed from the figures that the capacitor voltages are not balanced, especially at the 20% duty cycle in Figure 6-7(a)

where there is nearly a full 25 V division between the highest and lowest capacitor voltage waveforms. However, the voltages do appear more balance in Figure 6-7(b) and Figure 6-7(c) as the duty cycles increases. The measured capacitor voltages at all duty cycles for the 225 V input and 10 Ω load as well as the average value of all three capacitor voltages and the percent error of each capacitor voltage from the average value are shown in Table 6-2.

Table 6-2 Capacitor voltage test data for 225 V input, 10 Ω load

Duty Cycle	$V_{C,AVG}$ [V]	V_{C1} [V]	V_{C1} Percent Error	V_{C2} [V]	V_{C1} Percent Error	V_{C3} [V]	V_{C1} Percent Error
20%	75.50	71.0	-5.96%	66.5	-11.92%	89.0	17.88%
25%	75.38	70.9	-5.95%	69.8	-7.47%	85.5	13.42%
30%	75.67	72.0	-4.85%	72.0	-4.85%	83.0	9.69%
35%	75.33	72.5	-3.76%	72.5	-3.76%	81.0	7.52%
40%	75.33	73.5	-2.43%	73.0	-3.10%	79.5	5.53%
45%	75.33	74.0	-1.77%	73.5	-2.43%	78.5	4.20%
50%	75.33	74.5	-1.11%	74.0	-1.77%	77.5	2.88%
55%	75.50	75.0	-0.66%	74.5	-1.32%	77.0	1.99%
60%	75.50	75.5	0.00%	74.5	-1.32%	76.5	1.32%
65%	75.50	75.5	0.00%	74.5	-1.32%	76.5	1.32%
70%	75.67	76.0	0.44%	75.0	-0.88%	76.0	0.44%
75%	75.67	76.0	0.44%	75.0	-0.88%	76.0	0.44%
80%	75.50	76.0	0.66%	75.0	-0.66%	75.5	0.00%

The expected value of each of the capacitor voltages is a third of the high voltage, which will be equal to the average value of the three capacitor voltages. As seen in the table, the percent errors of the capacitor voltages from the average of the capacitor voltages are very large at the low duty cycle and improved as the duty cycle increased. This trend was also seen for all other input and load conditions as shown in Figure 6-8, which plots the percent error of each capacitor voltage from the mean of the capacitor voltages versus duty cycle.

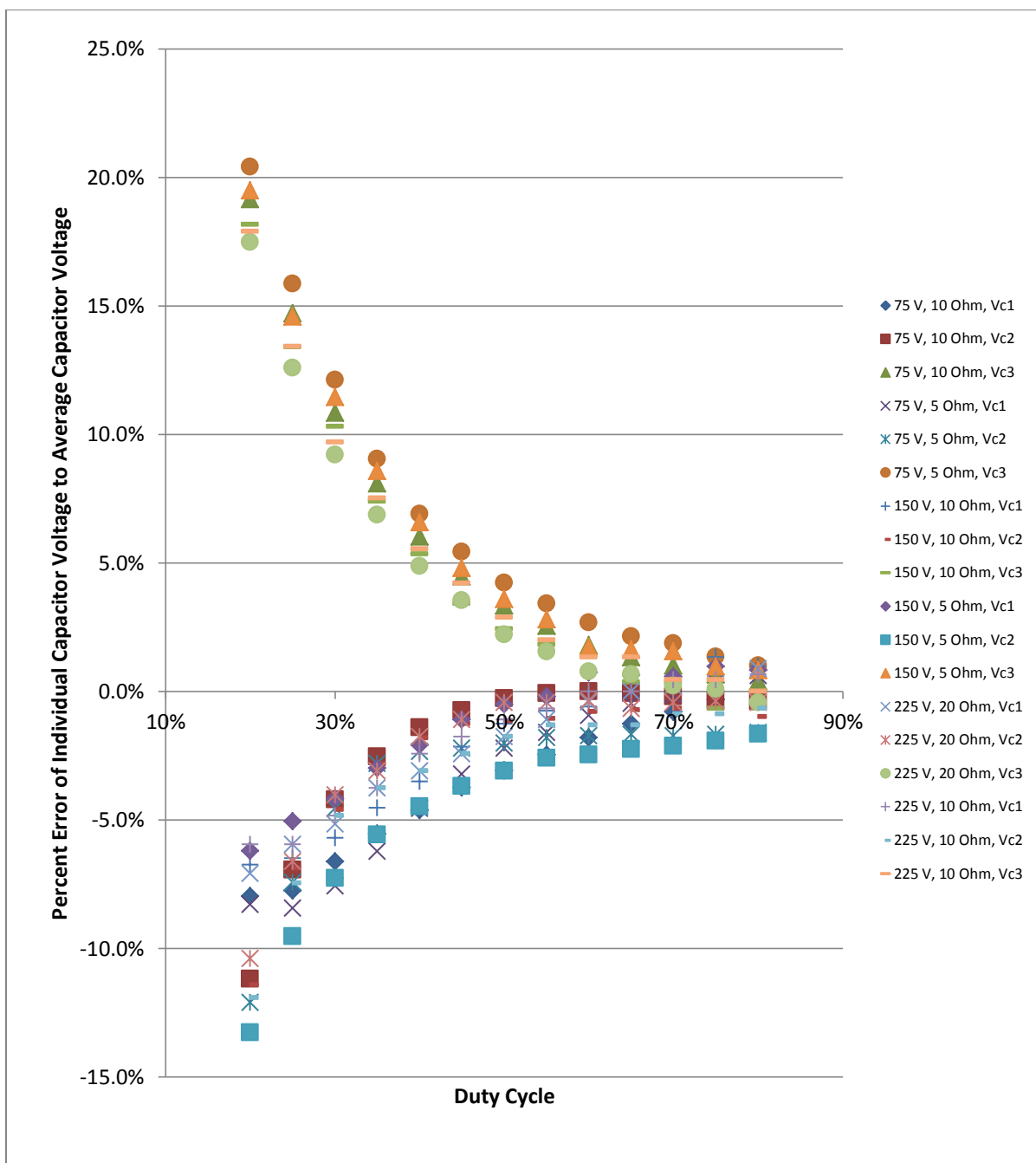


Figure 6-8 Percent error of each capacitor voltage from the mean versus duty cycle for all tested input voltage and load conditions

The data in Figure 6-8 is more cleanly shown in Figure 6-9 which plots the range of the absolute value of the percent errors in Figure 6-8. The data point for each duty cycle is

the average of all absolute values of the percent errors at a given duty cycle and the error bars show the positive and negative range of the absolute value of the percent errors from that average value. For example, for a duty cycle of 20%, across all input and load conditions, the average of the absolute value of the percent errors is 12.5%, with the maximum value being 20.4% and minimum being 6%.

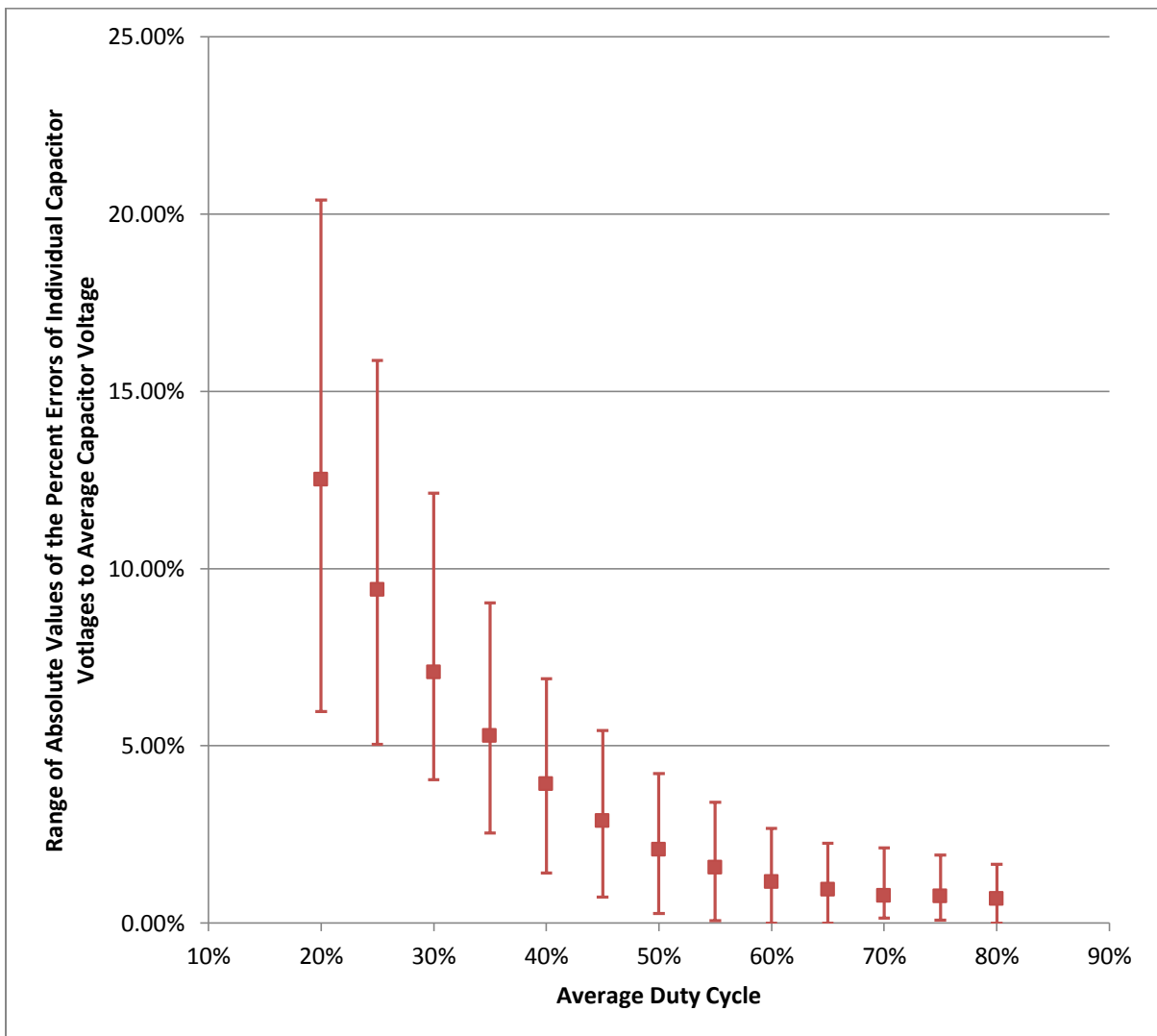


Figure 6-9 Absolute value of the percent error from the mean of each capacitor voltage versus duty cycle for all tested input voltage and load conditions

The significant imbalance of the capacitor voltages is a concern because it causes higher than desired voltage stress on the switching devices. However, the duty cycles of the can be modified to adjust the energy being take from each capacitor in order to balance the capacitor voltages. For all test results to this point, the duty cycles d_1 , d_2 and d_3 , which correspond to the duration in which energy is removed from each of the dividing capacitors as previously shown in Figure 2-15, have all been equal to the overall duty cycle of the converter d . For the following results, d_1 , d_2 and d_3 were modified in order to balance the capacitor voltages. Table 6-3 displays test data for the converter operating with a 225 V input voltage and 10 Ω load and in which duty cycles d_1 , d_2 and d_3 were individually modified by open loop control in increments/decrements of 0.25%.

Table 6-3 Capacitor voltage test data for 225 V input voltage and 10 Ω load in which open loop control of d_1 , d_2 and d_3 was implemented

d_1	d_2	d_3	Average Duty Cycle	$V_{C,AVG}$ [V]	V_{C1} [V]	V_{C1} Percent Error	V_{C2} [V]	V_{C1} Percent Error	V_{C3} [V]	V_{C1} Percent Error
20.50%	18.00%	21.50%	20.0%	75.5	75.2	-0.38%	75.9	0.55%	75.4	-0.18%
25.50%	23.25%	26.25%	25.0%	75.5	75.2	-0.44%	76.7	1.54%	74.7	-1.10%
30.50%	28.75%	30.75%	30.0%	75.5	74.2	-1.77%	76.3	1.08%	76.0	0.68%
35.50%	33.75%	35.75%	35.0%	75.5	75.1	-0.59%	76.7	1.58%	74.8	-0.99%
40.00%	39.25%	40.75%	40.0%	75.5	76.4	1.23%	74.2	-1.74%	75.9	0.51%
45.50%	44.00%	45.50%	45.0%	75.6	75.4	-0.26%	76.4	1.13%	74.9	-0.86%
50.25%	49.25%	50.50%	50.0%	75.6	76.0	0.53%	75.6	0.00%	75.2	-0.53%
55.50%	54.25%	55.25%	55.0%	75.5	75.4	-0.20%	76.2	0.86%	75.0	-0.66%
60.00%	59.75%	60.25%	60.0%	75.6	76.1	0.64%	74.8	-1.01%	75.9	0.37%
65.25%	64.50%	65.25%	65.0%	75.5	76.0	0.57%	75.5	-0.02%	75.1	-0.55%
70.25%	69.50%	70.25%	70.0%	75.5	76.1	0.79%	75.5	0.00%	74.9	-0.79%
75.00%	75.00%	75.00%	75.0%	75.7	76.0	0.44%	75.0	-0.88%	76.0	0.44%
80.00%	80.00%	80.00%	80.0%	75.5	76.0	0.66%	75.0	-0.66%	75.5	0.00%

The duty cycles were modified while still keeping the average d_1 , d_2 and d_3 at the nominal values of 20%, 25%, and so on. The worst percent error shown in the table is -1.77%

and better results could have been attained if smaller increments/decrements of d_1 , d_2 and d_3 than 0.25% were used. At the 75% and 80% duty cycles, smaller changes to the duty cycles than 0.25% would have been needed to improve upon the previous results. However, the overall balance of the capacitor voltages was drastically improved over the case with no open loop control as can be seen in Figure 6-10, which plots the 225 V input, 10 Ω load capacitor voltage results for the open loop control of d_1 , d_2 and d_3 case as well as the nominal case. The test data for the nominal case was previously shown in Table 6-2.

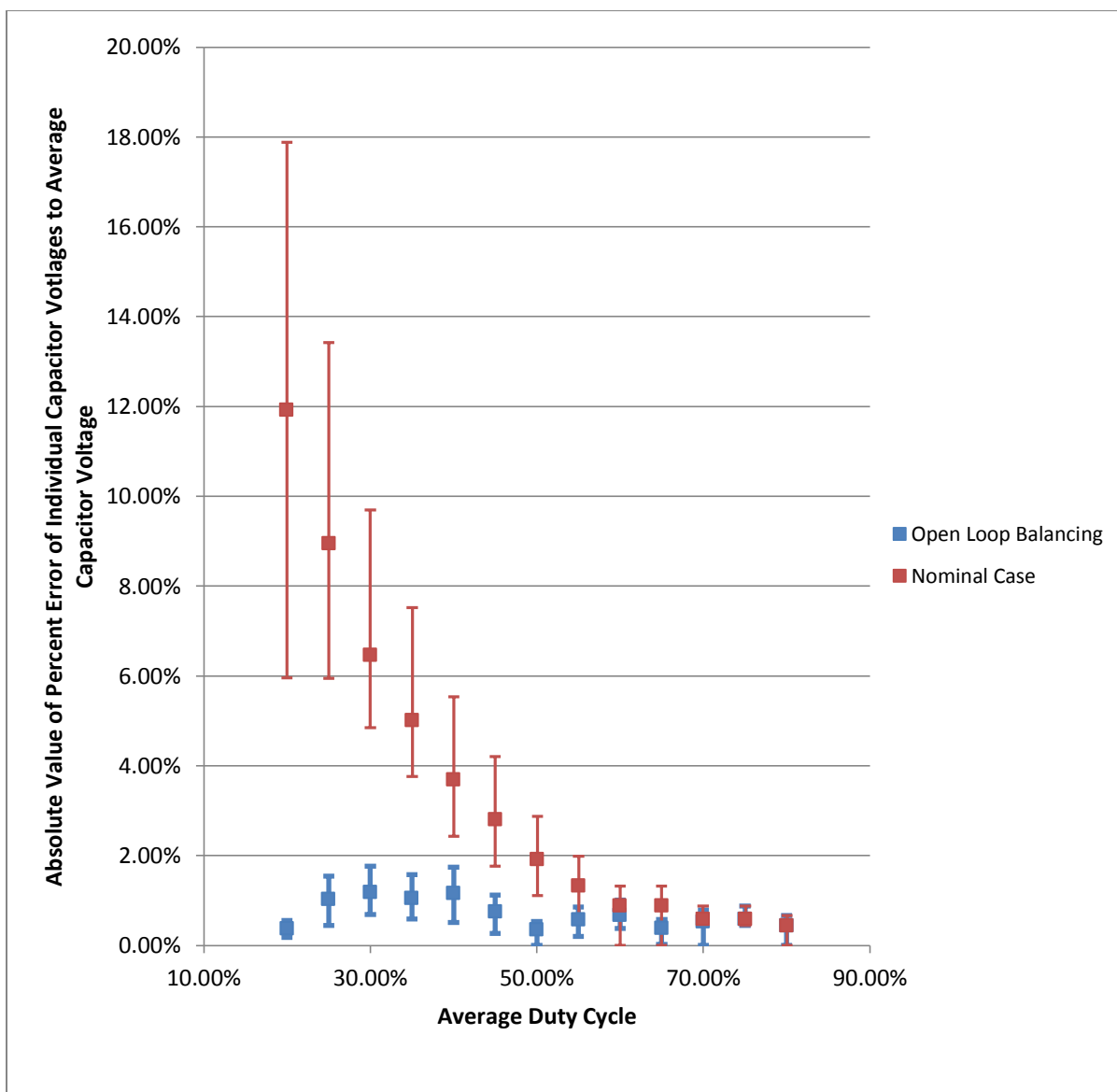


Figure 6-10 Absolute value of the percent error from the mean of each capacitor voltage versus duty cycle for 225 V input, 10 Ω load achieved with open loop balancing case as well as the nominal case

As previously mentioned, in the open loop control of d_1 , d_2 and d_3 case, the average of the duty cycles were equal to the nominal duty cycles previously test. Table 6-4 displays the input voltage, output voltage and transformation ratio for both the open loop balancing case as well as the nominal case.

Table 6-4 Voltage transformation data for the open loop balancing test and the nominal case for a 225 V input and 10 Ω load

Open Loop Balancing							Nominal Case			
d_1	d_2	d_3	Average Duty Cycle	V_{HV} [V]	V_{LV} [V]	V_{LV}/V_{HV}	d_1, d_2, d_3	V_{HV} [V]	V_{LV} [V]	V_{LV}/V_{HV}
20.50%	18.00%	21.50%	20.0%	225.0	15.0	0.067	20.0%	225.4	15.0	0.066
25.50%	23.25%	26.25%	25.0%	225.1	18.4	0.082	25.0%	225.1	18.4	0.082
30.50%	28.75%	30.75%	30.0%	225.0	21.9	0.097	30.0%	225.1	21.9	0.097
35.50%	33.75%	35.75%	35.0%	225.0	25.4	0.113	35.0%	225.1	25.4	0.113
40.00%	39.25%	40.75%	40.0%	225.0	29.0	0.129	40.0%	225.1	28.9	0.129
45.50%	44.00%	45.50%	45.0%	225.1	32.5	0.144	45.0%	225.1	32.4	0.144
50.25%	49.25%	50.50%	50.0%	225.1	36.0	0.160	50.1%	225.1	36.0	0.160
55.50%	54.25%	55.25%	55.0%	225.0	39.5	0.176	55.0%	225.3	39.5	0.175
60.00%	59.75%	60.25%	60.0%	225.1	43.0	0.191	60.0%	225.1	43.0	0.191
65.25%	64.50%	65.25%	65.0%	225.0	46.5	0.207	65.0%	225.2	46.5	0.206
70.25%	69.50%	70.25%	70.0%	225.1	50.0	0.222	70.0%	225.1	49.9	0.222
75.00%	75.00%	75.00%	75.0%	225.1	53.5	0.238	75.1%	225.1	53.5	0.238
80.00%	80.00%	80.00%	80.0%	225.1	56.9	0.253	80.0%	225.1	56.9	0.253

As seen in the table, with the average duty cycles of both cases being the same, the transformation ratios achieved were nearly identical.

In this thesis, concept a four-level, bidirectional buck-derived DC-DC converter was presented in detail and the implementation of a modulation scheme with considerations for dead time, both directions of power flow, and capacitor voltage balancing was presented. The design of a prototype converter was detailed. The numerous zero voltage and zero current transitions inherent in the scheme were presented by observing the converter conduction states and later verified by simulation results of a PLECS model of the converter within MATLAB/Simulink. Also through simulation, the bidirectional operation of the converter was confirmed.

A PLECS model of four-level converter that included the conduction losses of the power MOSFET and diode and snubber losses was used along with the derived converter switching loss equations to predict the efficiency of the hardware as well as provide confidence that efficiency of the converter could be greatly improved by eliminating the snubber circuitry and using a more suitably rated MOSFET with better loss characteristics. The prototype converter results corresponded fairly well with efficiency of the simulation model as well as the transformation ratios of the theoretical analysis and simulations.

The significant imbalance of the high voltage side divider capacitor voltages was shown to be an issue throughout the testing. The major issue with the imbalance is that it causes higher than desired voltage stress on the switching devices. However, it was shown through open loop control that the duty cycles of the converter can be modified to adjust the energy being take from each capacitor in order to better balance the capacitor voltages. For a

225 V input and 10Ω load condition in which the duty cycles were modified in increments/decrements of 0.25%, the open loop balancing achieved capacitor voltages that had a maximum percent error of less than 2% from the expected value of 75 V. That was down from the maximum of near 18% percent error for the testing that did not include the open loop control.

Through simulation and hardware results, the converter proved to be capable of high transformation ratio DC-DC conversion. Obviously, the converter uses a large number of switches in comparison to some of the other high transformation ratio typologies. However, for a certain application that trade off may be justifiable as the switches as only experience a voltage stress of a third of the high voltage, allowing for less costly switches with better loss characteristics than devices rated for the full high voltage, and as the converter typology tremendous scaling capability.

References

- [1] W. Li, X. Lv, Y. Deng and X. He, "A Review of Non-Isolated High Step-up DC/DC Converters in Renewable Energy Applications," in *Applied Power Electronics Conference and Exposition*, Washington, DC, 2009.
- [2] K. A. Corzine and S. K. Majeetha, "Analysis of a novel Four-Level DC/DC boost converter," in *Industry Applications Conference*, Phoenix, AZ, 1999.
- [3] J. Morren, S. W. H. de Haan and J. A. Ferreira, "Design study and scaled experiments for high-power DC-DC conversion for HVDC-systems," in *Power Electronics Specialists Conference*, Vancouver, 2001.
- [4] J. K. Reed and G. Venkataramanan, "Bidirectional high conversion ratio DC-DC converter," in *Power and Energy Conf. at Illinois (PECI)*, Champaign, IL, 2012.
- [5] X. Ruan, B. Li, Q. Chen, S.-C. Tan and C. K. Tse, "Fundamental Considerations of Three-Level DC-DC Converters: Topologies, Analyses, and Control," *IEEE Transactions on Circuits and Systems I*, vol. 55, no. 11, pp. 3733-3743, 2008.
- [6] Bourns, "1140 Series High Current Chokes Datasheet," 2008.
- [7] Fairchild Semiconductor, "FDP26N40 N-Channel UniFET MOSFET Datasheet," 2008.

- [8] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 2nd ed., Norwell, Massachusetts: Kluwer Academic Publishers, 2004.
- [9] Cornell Dubilier, "Application Guide: Snubber Capacitors," [Online]. Available: <http://www.cde.com/catalogs/igbtAPPguide.pdf>. [Accessed 1 March 2013].
- [10] Texas Instruments, "Stellaris® LM3S1968 Evaluation Board User's Manual," 2006.
- [11] International Rectifier, "IRFB4115PbF Datasheet," 2011.

Appendix A *Simplified conduction loss equations*

The conduction losses of a four-level converter are derived here. For this analysis, the bucking mode of operation will only be addressed and it will be assumed that when a given MOSFET is on and conducting current from source to drain that the MOSFET $R_{DS,on}$ and/or the current flowing through the MOSFET is small enough that the body diode of the MOSFET will not conduct current. For example, in conduction state 1, shown again in Figure A-1(a), it will be assumed that all current flowing through SW2H and SW4H is flowing through the MOSFET of the switch and none through the body diodes. The same will be assumed for situations in which three on MOSFETs are in parallel with a single body diode. For example, in conduction state 2, shown again in Figure A-1(b), it will be assumed that all inductor current flows through SW4H, SW3L and SW1H as opposed to current flowing through the body diode of SW1L in addition to SW4H, SW3L and SW1H. While this assumption will certainly not hold true for all operating conditions, this approach simplifies analysis and provides for an upper limit of the conduction losses as including the diode would reduce the losses.

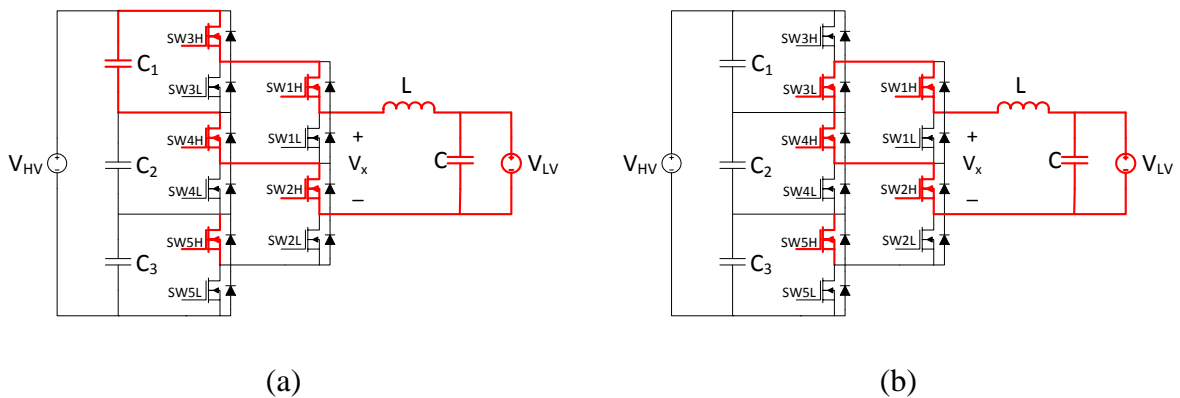


Figure A-1 Repeated conduction states 1 and 2

A.1 Conduction state losses

The conduction losses of a MOSFET can be approximated by

$$P_{FET,cond} = (I_{RMS})^2 R_{DS,on} \quad [8] \quad (A-1)$$

where I_{RMS} is the RMS value of the current through the switch, and $R_{DS,on}$ is the on resistance of the switch. The current through the switches will be trapezoidal similar to that show in Figure A-2, as the switch current will equal the inductor current during conduction states a given switch is conducted or the switch current will equal zero.

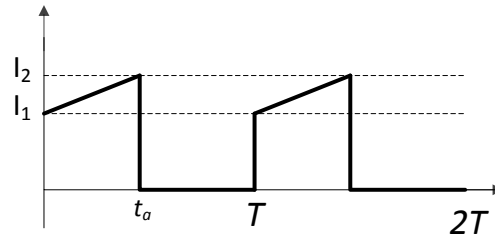


Figure A-2 Trapezoidal current waveform

The RMS value of a trapezoidal waveform can be found by

$$I_{RMS, trapezoid} = \sqrt{\frac{t_a (I_2^2 + I_1 I_2 + I_1^2)}{T}} \quad [8]. \quad (A-2)$$

If the inductor current is approximated by $i_L = I_{Load} + i_{ripple}$, the RMS of the switch current can be found to be

$$I_{RMS, trapezoid} = \sqrt{\frac{t_a}{T} \left(I_{load}^2 + \frac{\Delta i_{L,pk-pk}^2}{3} \right)} \quad (A-3)$$

The RMS current during odd conduction states is then

$$I_{RMS,cond. state k} = \sqrt{d_k \left(I_{load}^2 + \frac{\Delta i_{L,pk-pk}^2}{3} \right)} \quad (A-4)$$

where $k = 1, 3$ and 5 and d_k is the duty cycle for the k^{th} conduction state. Similarly, the RMS current during the even conduction states is

$$I_{RMS,cond. state k} = \sqrt{\left(\frac{1}{3} - d_k - \frac{2t_{dead}}{T_{sw}} \right) \left(I_{load}^2 + \frac{\Delta i_{L,pk-pk}^2}{3} \right)} \quad (A-5)$$

During conduction states 1 through 5, the inductor current passes through a total of four switches and the conduction losses in each of those states can be found by

$$P_{FET,cond. state 1} = d_1 \left(I_{load}^2 + \frac{\Delta i_{L,pk-pk}^2}{3} \right) 4R_{DS,on} \quad (A-6)$$

$$P_{FET,cond, state 2} = \left(\frac{1}{3} - d_1 - \frac{2t_{dead}}{T_{sw}} \right) \left(I_{load}^2 + \frac{\Delta i_{L,pk-pk}^2}{3} \right) 4R_{DS,on} \quad (A-7)$$

$$P_{FET,cond, state 3} = d_2 \left(I_{load}^2 + \frac{\Delta i_{L,pk-pk}^2}{3} \right) 4R_{DS,on} \quad (A-8)$$

$$P_{FET,cond, state 4} = \left(\frac{1}{3} - d_2 - \frac{2t_{dead}}{T_{sw}} \right) \left(I_{load}^2 + \frac{\Delta i_{L,pk-pk}^2}{3} \right) 4R_{DS,on} \quad (A-9)$$

$$P_{FET,cond, state 5} = d_3 \left(I_{load}^2 + \frac{\Delta i_{L,pk-pk}^2}{3} \right) 4R_{DS,on} \quad (A-10)$$

During conduction state 6, the inductor current only passes through two switches so the resulting conduction loss is

$$P_{FET,cond, state 6} = \left(\frac{1}{3} - d_3 - \frac{2t_{dead}}{T_{sw}} \right) \left(I_{load}^2 + \frac{\Delta i_{L,pk-pk}^2}{3} \right) 2R_{DS,on} \quad (A-11)$$

Summing (A-6) through (A-11), the total conduction loss is found to be

$$P_{FET,cond, total} = \left(\frac{5}{6} + \frac{d_3}{2} - \frac{5t_{dead}}{T_{sw}} \right) \left(I_{load}^2 + \frac{\Delta i_{L,pk-pk}^2}{3} \right) 4R_{DS,on} \quad (A-12)$$

A.2 Transition state conduction losses

Additional losses occur during the transition states in which the inductor current is freewheeling for a duration equal to the dead time. It is a reasonable assumption that the inductor current remains constant during the transition period as the dead time should be significantly smaller than the inductor waveform period. Conduction losses occur in six of the eight transitions states. Those states are the transition to state 1, transition to state 2, transition to state 3a, transition to state 4, transition to state 5, and transition to state 6a. During the transitions to conduction states 1, 2, 5 and 6a, the inductor current flows through a one on MOSFET and one diode. The loss during those states can be approximated by

$$P_{cond,trans. \text{ to state 1}} = t_{dead}f_{SW}[i_{L,min}V_{FD} + i_{L,min}^2(R_{DS,on} + R_{D,on})] \quad (\text{A-13})$$

$$P_{cond,trans. \text{ to state 2}} = t_{dead}f_{SW}[i_{L,max}V_{FD} + i_{L,max}^2(R_{DS,on} + R_{D,on})] \quad (\text{A-14})$$

$$P_{cond,trans. \text{ to state 5}} = t_{dead}f_{SW}[i_{L,min}V_{FD} + i_{L,min}^2(R_{DS,on} + R_{D,on})] \quad (\text{A-15})$$

$$P_{cond,trans. \text{ to state 6a}} = t_{dead}f_{SW}[i_{L,max}V_{FD} + i_{L,max}^2(R_{DS,on} + R_{D,on})] \quad (\text{A-16})$$

where V_{FD} is the forward voltage drop of the diode and $R_{D,on}$ is the diode on resistance.

During the transitions to state 3a and 4, the inductor current flows through a three on MOSFET and one diode. The loss during those states can be approximated by

$$P_{cond,trans. \text{ to state 5}} = t_{dead}f_{SW}[i_{L,min}V_{FD} + i_{L,min}^2(3R_{DS,on} + R_{D,on})] \quad (\text{A-17})$$

$$P_{cond,trans. \text{ to state 6a}} = t_{dead}f_{SW}[i_{L,max}V_{FD} + i_{L,max}^2(3R_{DS,on} + R_{D,on})] \quad (\text{A-18})$$

The total MOSFET and body diode conduction loss during the

$$P_{cond,trans. \text{ state total}} = t_{dead}f_{SW}[6i_{L,min}V_{FD} + i_{L,min}^2(10R_{DS,on} + 6R_{D,on})] \quad (\text{A-19})$$

A.1 Ideal bucking mode MATLAB code and Simulink files

The MATLAB code for the ideal simulation of the converter in bucking operation is shown below:

```

% Ideal Simulation for bucking operation

clear all; close all; clc; format longg;

duty = 0.5;           %<----- choose duty cycle
duty1 = duty/3;
duty2 = duty/3;
duty3 = duty/3;
Rload = 10;          % Load resistance
V_HV = 225;          % High Voltage
dead time = 0;       % Dead time b/w high side and low side
Rds_on = 0;
V_fd = 0;

Fs = 10e3;           % Switching Frequency
Ts = 1/Fs;           % Switching Period
L = 330e-6;          % Inductor
V_LV_nom = V_HV/3*duty; % nominal Low Voltage
C = 100e-6;          %
C1 = 470e-6;         %
C2 = C1;              %
C3 = C1;              %

Vc_init = V_LV_nom;
Rsource = 0.05;
Il_init = Vc_init/Rload;

Vc1_init = V_HV/3;
Vc2_init = V_HV/3;
Vc3_init = V_HV/3;

%cond. period:1 2 3a 3b 4 5 6a 6b
SW1_table = [ 1; 1; 1; 1; 0; 0; 0; 0;];
SW2_table = [ 1; 1; 0; 0; 0; 0; 1; 1;];
SW3_table = [ 1; 0; 0; 0; 0; 0; 0; 1;];
SW4_table = [ 1; 1; 1; 0; 0; 0; 0; 1;];
SW5_table = [ 1; 1; 1; 1; 1; 0; 0; 1;];

% Run Simulink Model

```

```

t_end = 200*Ts;
t_step_max = Ts/1e3;
data_points = 800000; % number of data points saved

sim('Ideal_4_level_HV_to_LV');
    
```

The Simulink model “Ideal_4_level_HV_to_LV” is shown in Figure B-1.

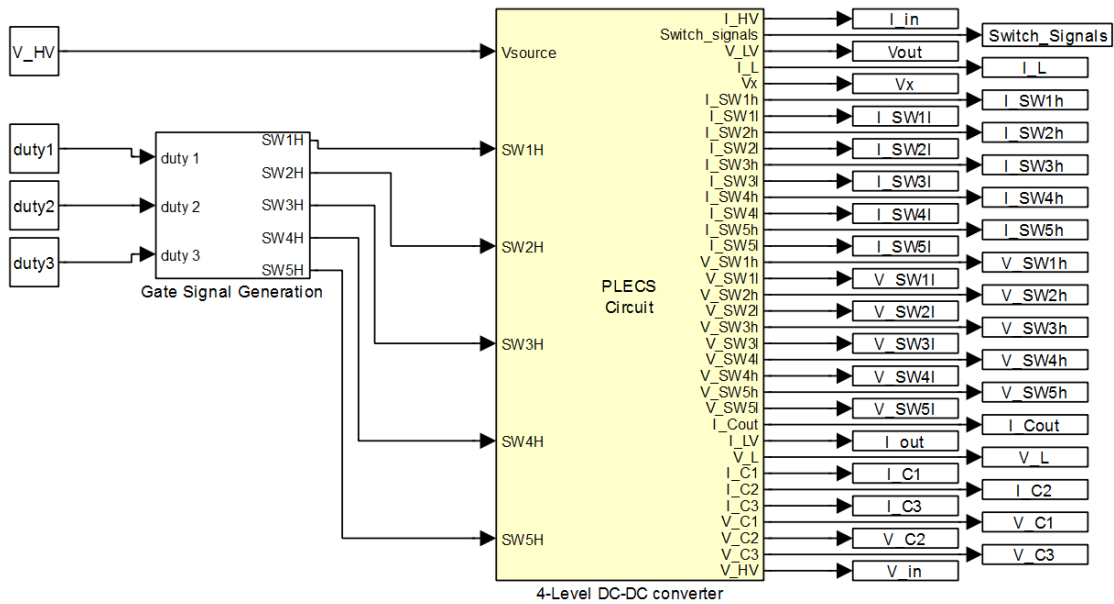


Figure B-1 Ideal converter in bucking mode Simulink model

The subsystems of “4-Level DC-DC converter” and “Gate Signal Generation” are shown in Figure B-2 and Figure B-3, respectively.

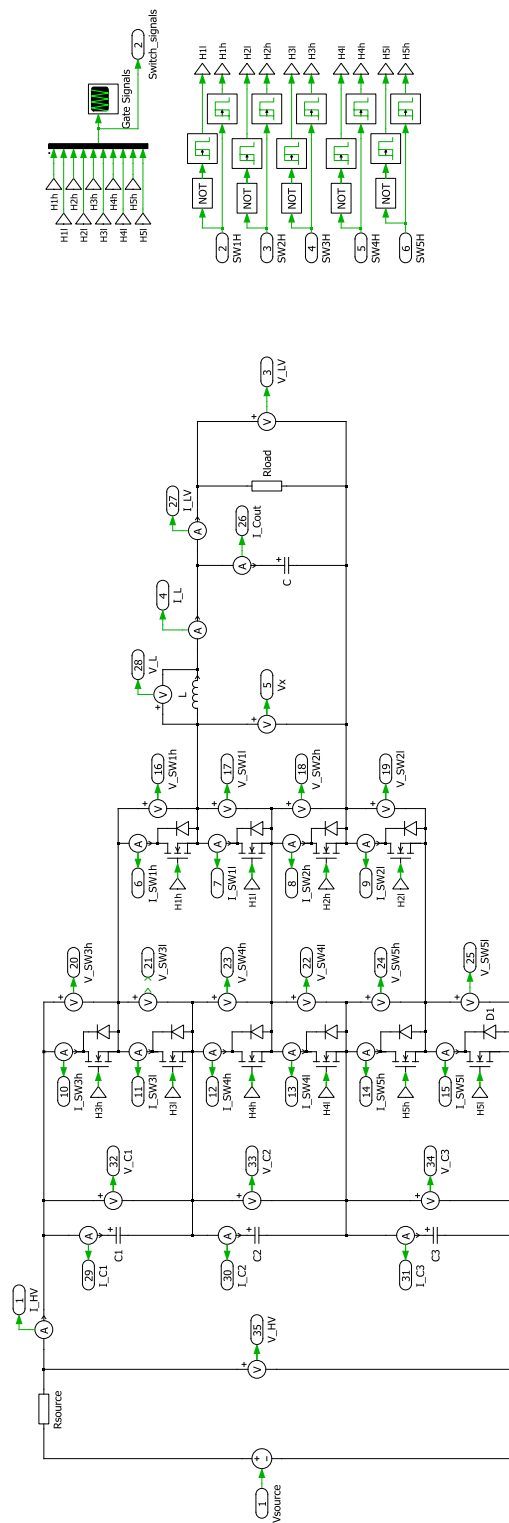


Figure B-2 “4-Level DC-DC converter” subsystem for the ideal simulation of the converter in bucking operation

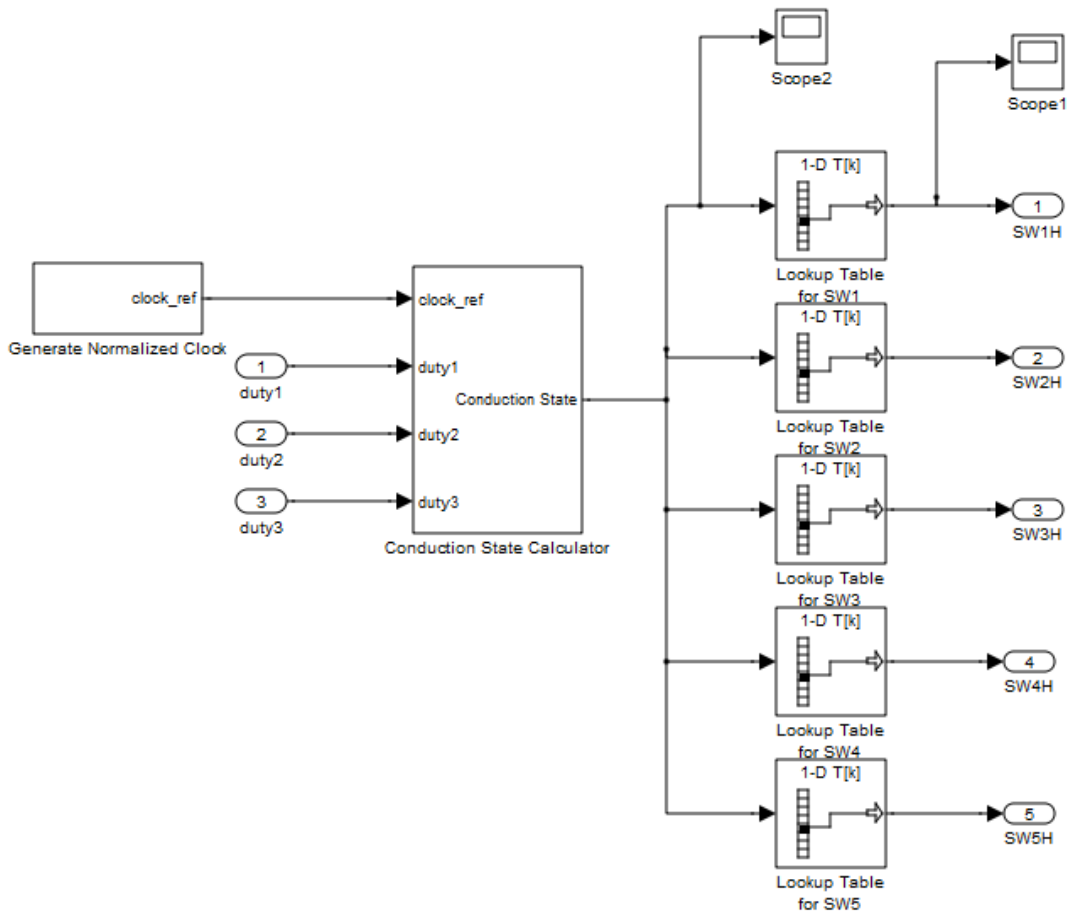


Figure B-3 “Gate Signal Generation” subsystem for the ideal simulation of the converter in bucking operation

The lookup tables in the figure are defined in the Matlab code. The “Conduction State Calculator” subsystem is shown Figure B-4.

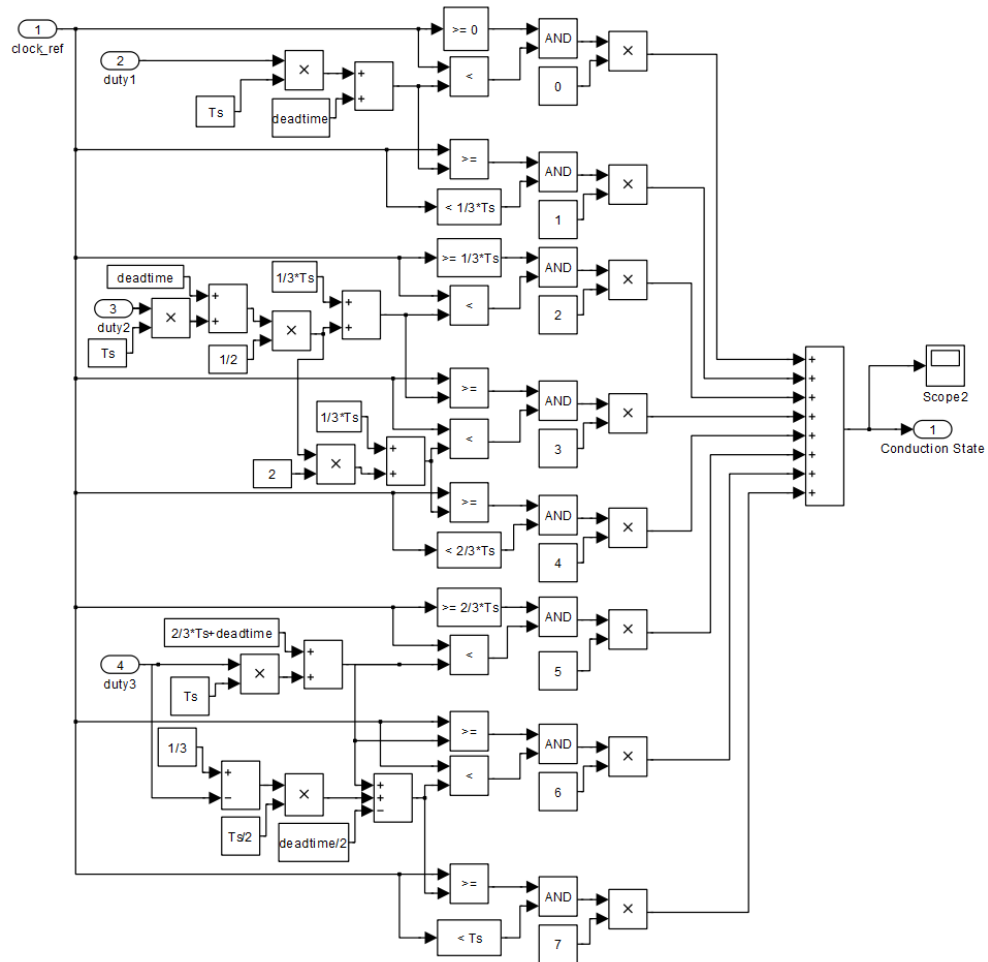


Figure B-4 “Conduction State Calculator” subsystem for the ideal simulation of the converter in bucking operation

A.2 Ideal boosting mode MATLAB code and Simulink files

The MATLAB code for the ideal boosting mode simulations is shown below:

```
% Initializes the 4 level LV to HV simulation

clear all; close all; clc; format longg;

duty = 0.75;          %<----- choose duty cycle
```

```

duty1 = duty/3;
duty2 = duty/3;
duty3 = duty/3;
Rload = 250;           % Load resistance
V_LV = 24;            % High Voltage
dead_time = 0;       % Dead time b/w high side and low side
Rds_on = 0;
V_fd = 0;

Fs = 10e3;           % Switching Frequency
Ts = 1/Fs;           % Switching Period
L = 330e-6;          % Inductor
V_HV_nom = V_LV*3/duty; % nominal Low Voltage
C = 100e-6;           %
C1 = 470e-6;          %
C2 = C1;              %
C3 = C1;              %

Vc_init = V_LV;
Rsource = 0.005;
Il_init = V_HV_nom/Rload;

%
Vc1_init = V_HV_nom/3;
Vc2_init = V_HV_nom/3;
Vc3_init = V_HV_nom/3;
%cond. period:1 2 3a 3b 4 5 6a 6b
SW1_table = [ 1; 1; 1; 1; 0; 0; 0; 0;];
SW2_table = [ 1; 1; 0; 0; 0; 0; 1; 1;];
SW3_table = [ 1; 0; 0; 0; 0; 0; 0; 1;];
SW4_table = [ 1; 1; 1; 0; 0; 0; 0; 1;];
SW5_table = [ 1; 1; 1; 1; 1; 0; 0; 1;];

% Run Simulink Model
t_end = 3000*Ts;
t_step_max = Ts/1e3;
data_points = 800000; % number of data points saved

sim('Ideal_4_level_LV_to_HV');

```

The Simulink model “Ideal_4_level_LV_to_HV” is shown in Figure B-5.

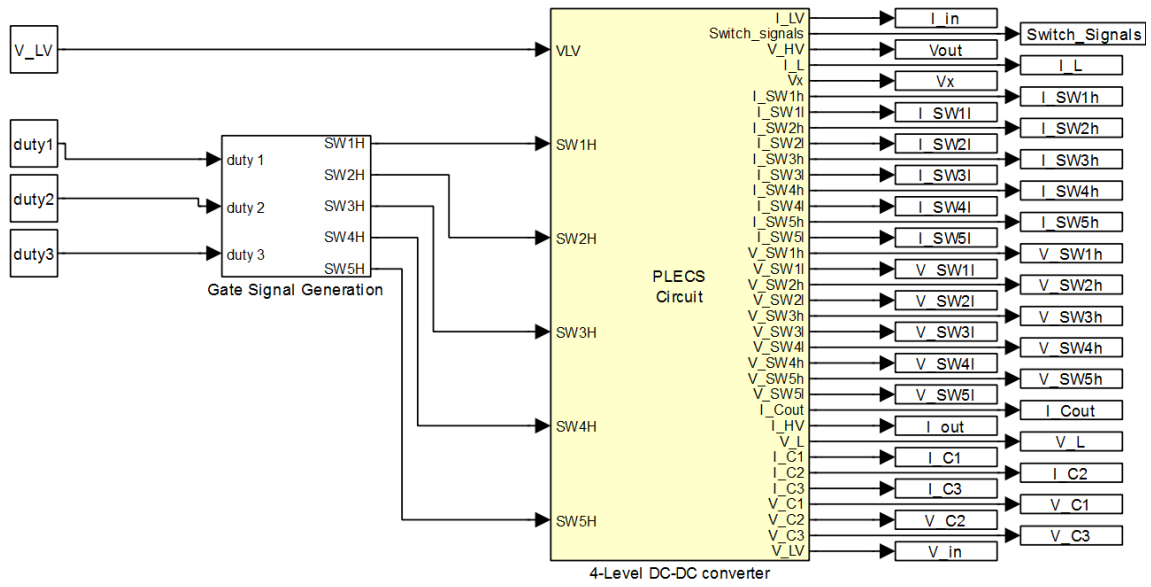


Figure B-5 Ideal converter in boosting mode Simulink model

The subsystems of “4-Level DC-DC converter” and “Gate Signal Generation” are shown in Figure B-6 and Figure B-7, respectively.

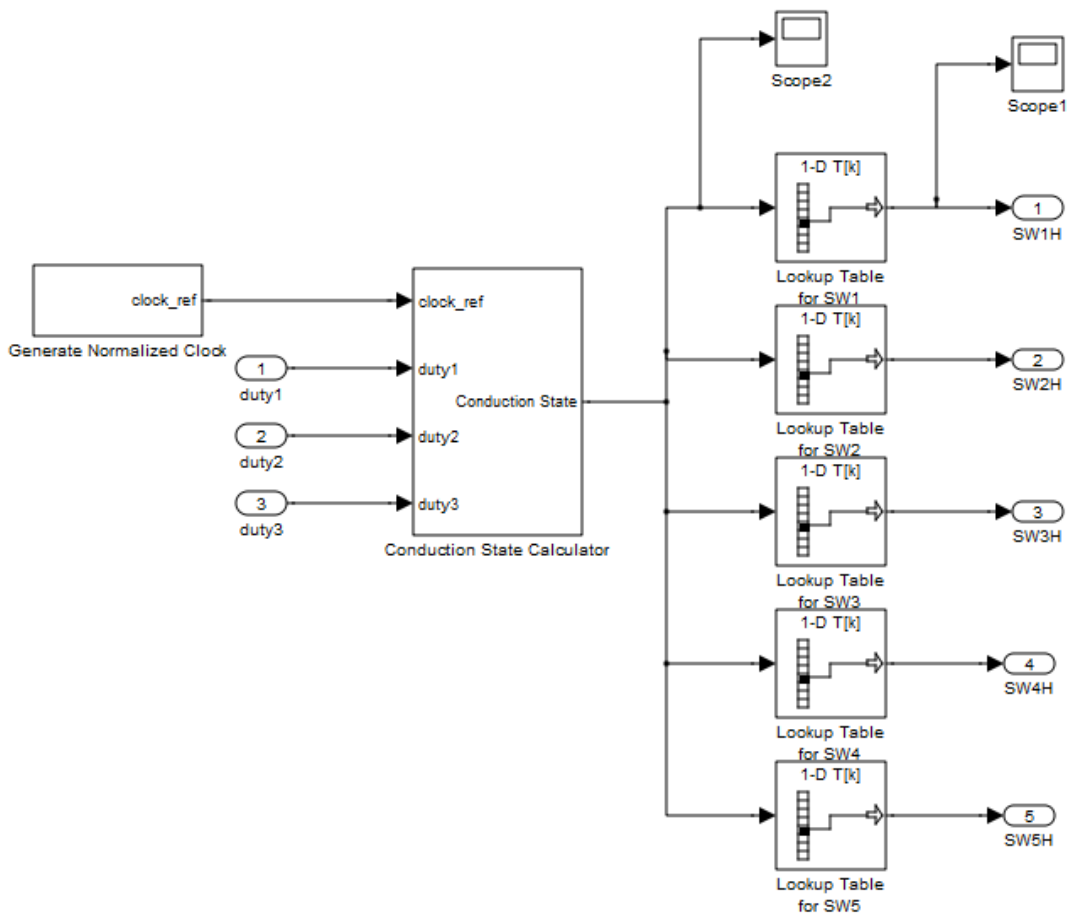


Figure B-7 “Gate Signal Generation” subsystem for the ideal boosting mode simulations

The lookup tables in the figure are defined in the Matlab code. The “Conduction State Calculator” subsystem is shown Figure B-8.

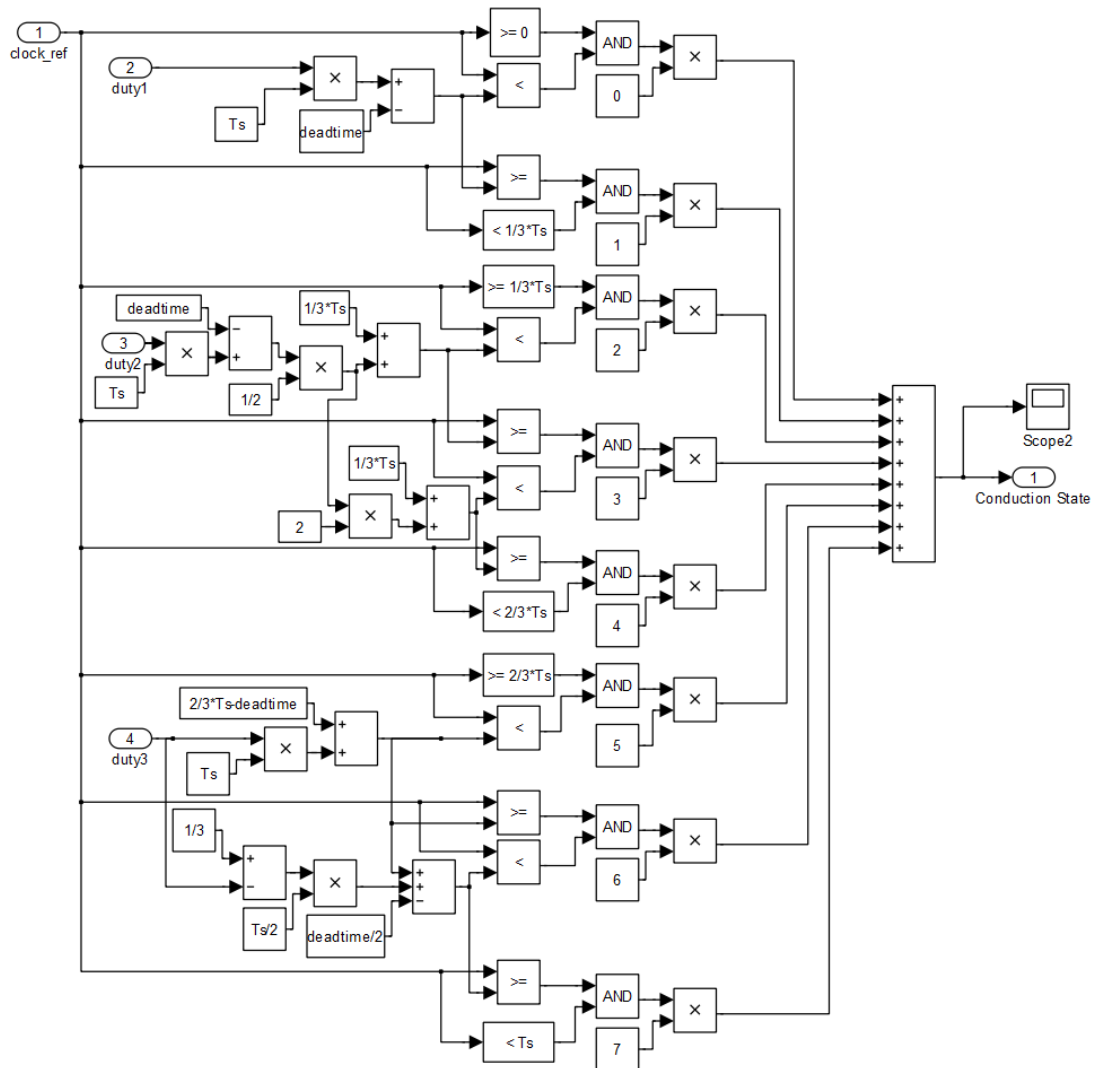


Figure B-8 “Conduction State Calculator” subsystem for the ideal boosting mode simulations

A.3 Non-ideal bucking mode MATLAB code and Simulink files

The MATLAB code for the non-ideal simulations is shown below:

```
% Initializes the non-ideal 4 level converter in bucking mode
```

```
clear all; close all; clc; format longg;
```

```

duty = 0.2           %<----- choose duty cycle
duty1 = duty/3;
duty2 = duty/3;
duty3 = duty/3;
Rload = 10;         % Load resistance
V_HV = 225;        % High Voltage
dead time = 1.25e-6; % dead time between switches in same half bridge

%FDP26N40 MOSFET
Rds_on = 0.13;     % on resistance
trise=100E-9;
tdelay_on = 45e-9;
tdelay_off = 115e-9;
tfall=66E-9;
V_fd = 0.6875;     % forward voltage drop of body diode
R_don = 14.3e-3;   % on resistance of body diode

% %IRFB4115PbF MOSFET
% Rds_on = 11e-3;   % MOSFET on resistance
% trise=73E-9;
% tdelay_on = 18e-9;
% tdelay_off = 41e-9;
% tfall=39E-9;
% V_fd = 0.6;      % forward voltage drop of antiparallel diode
% R_don = 16.6e-3;

Fs = 10e3;         % Switching Frequency
Ts = 1/Fs;        % Switching Period
L = 330e-6;       % Inductor
R_L = 0.074;      % Inductor resistance (using DC value)
V_LV_nom = V_HV/3*duty; % nominal Low Voltage
C = 100e-6;       %
C1 = 470e-6;     %
C2 = C1;         %
C3 = C1;         %
Rdivide = 100e3;

V_fd_snub = 0.925;
R_don_snub = 0.05;
R_snub = 6.2;
C_snub = 12e-9;

Vc_init = V_LV_nom;
Rsource = 0.05;
Il_init = Vc_init/Rload;

% for non-ideal simulation
Vc1_init = V_HV/3;
Vc2_init = V_HV/3;

```

```
Vc3_init = V_HV/3;
%cond. period:1 2 3a 3b 4 5 6a 6b
SW1_table = [ 1; 1; 1; 1; 0; 0; 0; 0;];
SW2_table = [ 1; 1; 0; 0; 0; 0; 1; 1;];
SW3_table = [ 1; 0; 0; 0; 0; 0; 0; 1;];
SW4_table = [ 1; 1; 1; 0; 0; 0; 0; 1;];
SW5_table = [ 1; 1; 1; 1; 1; 0; 0; 1;];

% Run Simulink Model
t_end = 170*Ts;
t_step_max = Ts/1e4;
data_points = 800000; % number of data points saved

sim('Fullconverter_4_level_HV_to_LV');
```

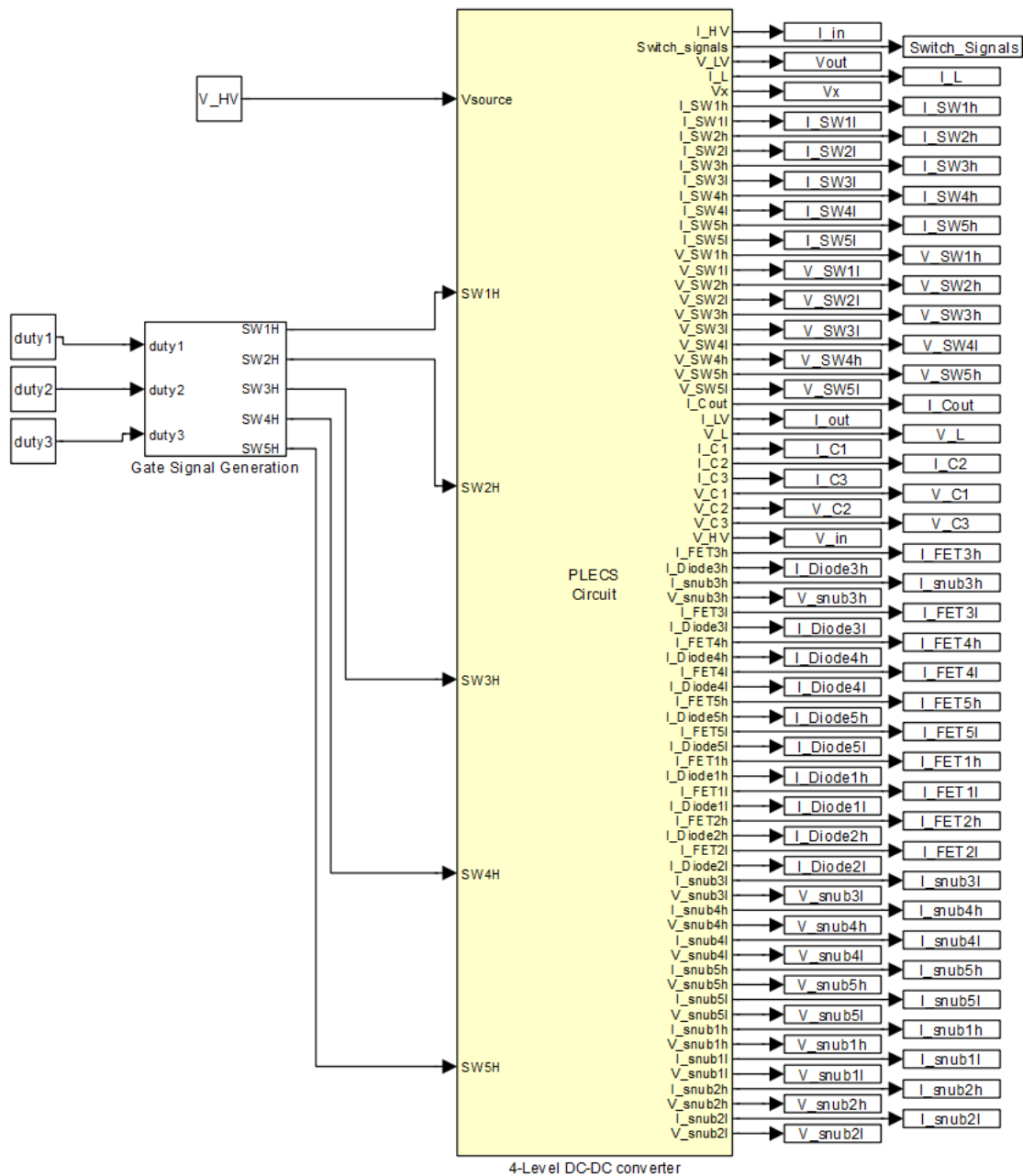


Figure B-9 Simulink model for the non-ideal simulations

The “Gate Signal Generation” subsystem is exactly as previously shown in Figure B-3 and Figure B-4 for the ideal bucking mode simulations. The “4 Level DC-DC converter” subsystem is shown in Figure B-10.

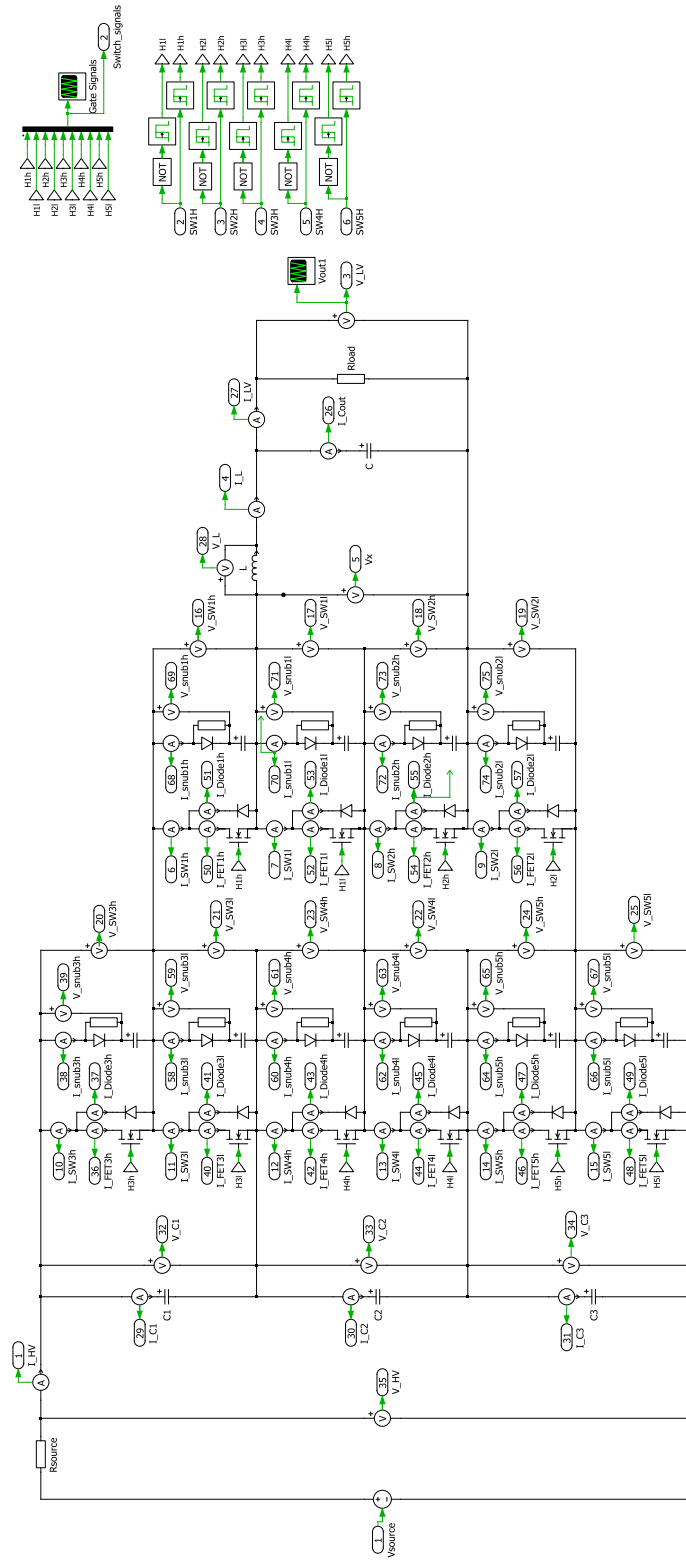


Figure B-10 “4 Level DC-DC converter” subsystem for the non-ideal simulations