Dynamic Analysis of Loss-Limited Switching Full-Bridge DC–DC Converter With Multimodal Control

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***Abstract*—Full-bridge dc–dc converters with one soft-switched leg and one hard-switched leg have recently been introduced as an attractive approach for realizing high-frequency power conversion at power levels greater than 100 kW. This paper presents a new variable-frequency multimodal control strategy for these converters for obtaining optimal operating characteristics. The controller extends the soft-switching operating region of the converter while lowering magnetic component core loss. Steady-state and dynamic analyses of the converter operation in the various modes are developed. Simulation and experimental results verifying the operation of the converter are presented.**

***Index Terms*—DC–DC converters, modal analysis, multimodal control, nonlinear dynamic modeling, soft switching.**

I. Introduction

REALIZATION of high-power ($>$100 kW) isolated dc–dc converters is a challenging task requiring numerous tradeoffs that involve topology selection, device utilization, and magnetics design. Recently, a loss-limited switching dc–dc converter employing one resonant soft-switching pole and one phase-shifted hard-switching pole was demonstrated to be an effective means of realizing the same [1]. Production units of this converter that provide 750 V at 180 A (135 kW) have been used to feed 18 isolated dc buses for a cascaded-multilevel-inverter-based motor drive system [2]. This drive operates from a dc input of 900 V. A photograph of one of these converters is shown in Fig. 1. An interesting feature of the dc–dc converter feeding a cascaded multilevel inverter is wide variation in the power throughput due to single phase loading posed to each of the dc buses [3].

It is common to employ a traditional fixed-frequency current-mode control for regulating the output of full-bridge isolated dc–dc converters. In this scheme, the devices in each leg of the full bridge are operated at fixed frequency with 50% duty cycle and a constant dead time. The peak current is regulated by controlling the phase shift between the two legs. To extend converter operation to higher power levels, capacitors are placed across the devices to control the dv/dt and reduce switching losses [4]. In the loss-limited topology, these are placed only on the resonant soft-switching pole. The placement of the capacitors leads to a load-current-dependent transition in the device voltages. At light-load conditions, this transition time can be longer than the dead time between devices on the same leg, and the incoming device shorts out the capacitor, with heavy losses. Furthermore, if the transition time exceeds the switching half-period, the frequency has to be lowered, otherwise, light-load operation is not possible. A traditional fixed-frequency current-mode controller at a lower frequency can be used to extend the operating range to light loads at the expense of a significant increase in core loss in the magnetic elements at rated conditions.

In order to address these issues, a new multimodal control strategy that increases the operating range without seriously expending the thermal budget is presented in this paper. At heavy load current levels, the controller behaves like a traditional fixed-frequency controller at 25 kHz. At light loads a constant off-time control that reduces the operating frequency,

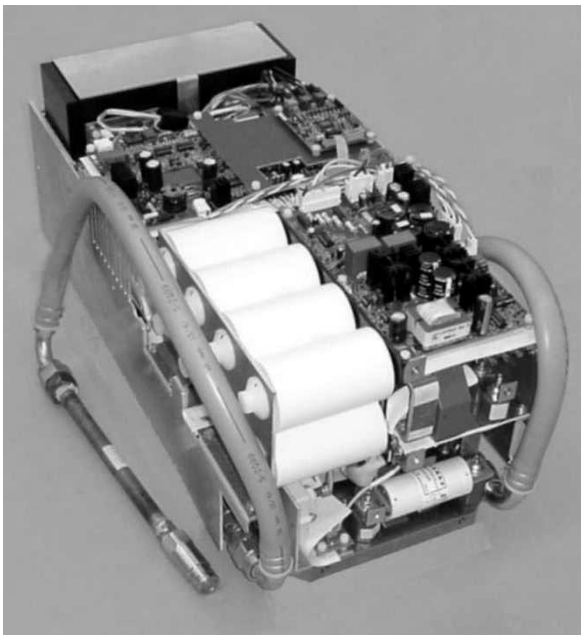

Fig. 1. Photograph of an isolated loss-limited dc–dc converter unit.

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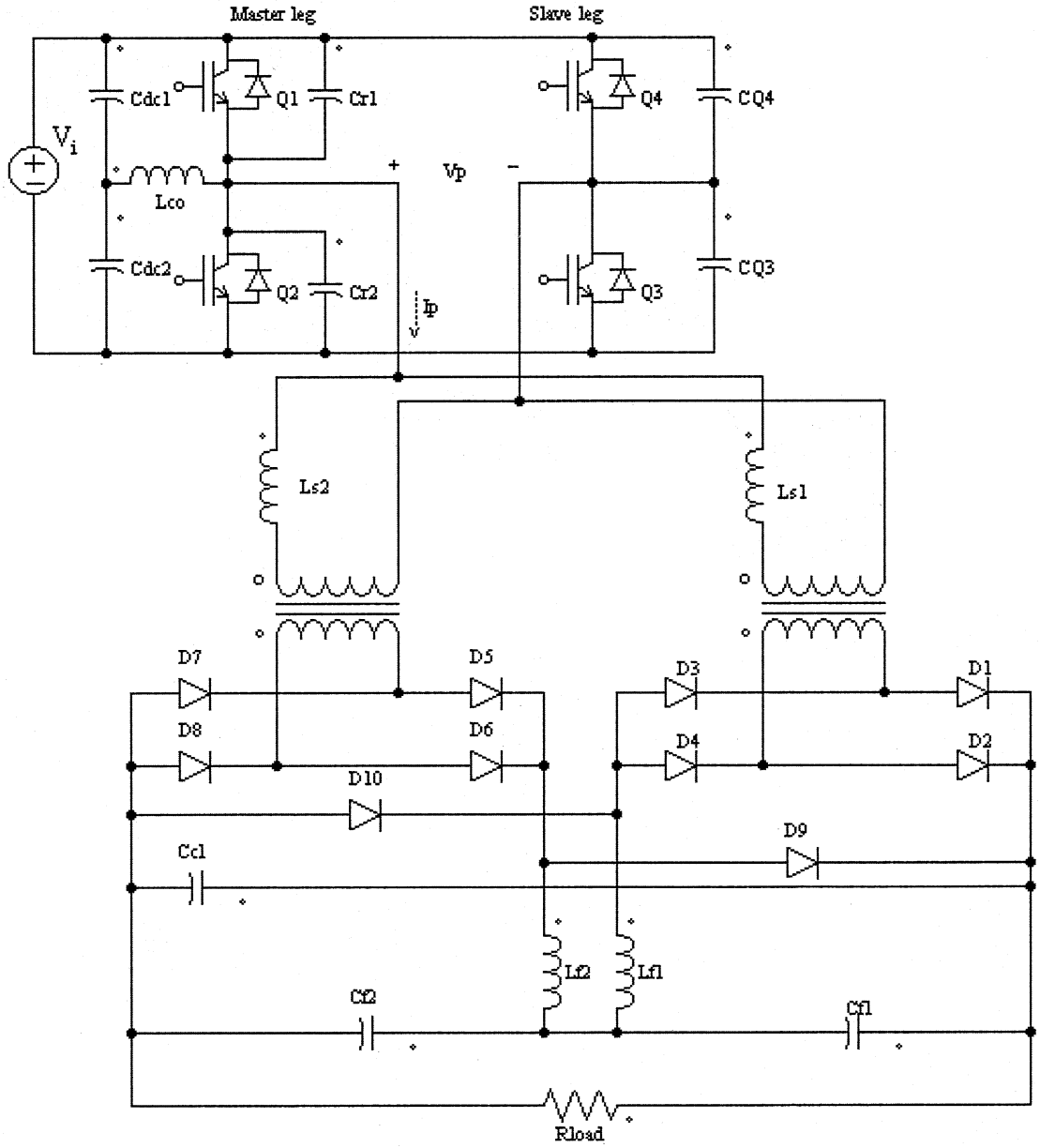

Fig. 2. Schematic of the isolated loss-limited dc–dc converter.

while maintaining loss-limited switching is adopted [5]. When the operating frequency drops to 20 kHz, it is not allowed to drop any further to prevent transformer core saturation. In this mode, the controller maintains balanced flux in the transformer, while providing the maximum possible voltage. The converter control transition between these modes takes place in a seamless manner. Thus, by using multimodal control, a balance is obtained between the core and copper losses in the magnetic components of the converter by minimizing the core loss at rated load levels.

Converter power topology and operation is discussed in Section II. Section III presents a simplified high-frequency steady-state analysis describing various switching modes of operation. A low-frequency dynamic model of the converter operation is developed in Section IV. The low-frequency dynamic model is used to solve for the static operating conditions in Section V, demonstrating the wide operating region using the multimodal control. Outer voltage loop controller design aspects are illustrated in Section VI along with the simulation results verifying the analysis. Operation of the controller in the open-loop mode at very light loads is presented in Section VII, and flux-balancing mechanisms are identified. Section VIII contains a summary of the concepts presented in the paper.

II. Converter Operation

Power device switching losses, loss of throughput due to transformer leakage, and diode reverse-recovery losses represent the major impediments to realization of high-frequency high-power dc–dc converters. The loss-limited dc–dc converter topology uses low-leakage coaxial-wound transformers along with a novel primary commutation scheme that limits the switching loss, a split secondary that permits the use of lower voltage diodes, and an energy recovery clamp for diode recovery [1]. The converter topology is shown in Fig. 2. Major parameters of the power circuit elements are shown in Table I.

TABLE I
POWER CIRCUIT PARAMETERS

Parameter	Symbol	Value
Transformer turns ratio	N_p:N_s	2:1
Transformer leakage inductance	L_{s1}, L_{s2}	500nH
Transformer magnetizing inductance	L_{m1}, L_{m2}	500uH
Device capacitance	C_{Q3}, C_{Q4}	4nF
Commutation inductance	L_{co}	250μH
Resonant capacitance	C_{r1}, C_{r2}	150nF
Output filter inductance	L_{f1}, L_{f2}	50μH
Output filter capacitance	C_{f1}, C_{f2}	13500μF
Rated input DC voltage	V_i	900V
Rated output DC voltage	V_{CF1}, V_{CF2}	375V
Rated output current	I_{LF1}, I_{LF2}	200A

The power throughput of the converter is controlled by phase shifting the drive waveforms of the master leg (Q1, Q2 pair) with respect to the drive waveforms of the slave leg (Q3, Q4 pair) of the primary H-bridge. The master or lagging leg transitions the transformer primary from an actively driven state to zero state. Resonant capacitors C_{r1}, C_{r2} are added across these lagging leg devices Q1, Q2 to limit dv/dt and switching loss during this transition. This leg obtains its commutation energy from the reflected load current flowing through the large output filter inductances (L_{f1}, L_{f2}). To effect commutation at no load, an additional commutation inductor L_{co} is connected from the master pole back to the midpoint of the dc bus. If successful commutation of the resonant capacitors is achieved, the turn-on loss is negligible for Q1, Q2, as the devices are turned on with their antiparallel diodes conducting.

The commutation of the slave or leading leg, which transitions the transformer primary from a zero state to an actively driven state, is not fueled by the load current as the load current is decoupled from the primary circuit in the zero state. The only energy for this transition is that stored in the small leakage inductance of the transformer, which is typically insufficient to commutate any resonant capacitance across the slave devices. If low-leakage coaxial-wound transformers are used, the stored inductive energy is even smaller and resonant capacitors cannot be used to limit switching losses in the slave leg. The total energy in the primary circuit in the zero state before the outgoing slave device is turned off is small $\left(1/2\left(L_{s1}+L_{s2}\right)I_p^2\right)$ and sets the upper limit on the energy that can be dissipated in slave switch if it is hard switched. This limit is utilized in the loss-limited converter by eliminating resonant capacitors on the slave leg devices Q3, Q4 and hard switching this leg with modest turn off losses. Furthermore, the hard-switched turn-on of Q3, Q4 also exhibits lower losses as the finite leakage inductance provides adequate turn-on snubbing.

Two coaxial transformers with a 2:1 turns ratio are connected in a parallel primary, series secondary arrangement to provide isolation. Two full-wave rectifier bridges D1–D4 and D5–D8 rectify the secondary voltage and inductors L_{f1}, L_{f2} and capacitors C_{f1}, C_{f2} serve as the output filter. The clamp arrangement consists of clamp diodes D9, D10 and clamp capacitor C_{cl}. When the primary voltage is zero, all diodes in the secondary side bridges are on and the load current freewheels. When a device on the leading leg Q3 (Q4) turns on, diodes D1, D4, D5, D8 (D2, D3, D6, D7) are commutated off. The reverse-recovery current associated with this flows in the leakage inductance of the transformer. When the outgoing diodes in each bridge snap off, the trapped energy results in an increased voltage across the bridges. Clamp diodes D10 and D9 conduct as soon as this increased bridge voltage exceeds the output voltage, transferring the recovery energy to clamp capacitor C_{cl}, and eventually to the output. The clamp circuit recovers the reverse-recovery energy of the output rectifiers at the expense of increased conduction loss due to the two series lower voltage rectifier bridges. The superior switching characteristics of the lower voltage rectifiers and the presence of a stiff clamping voltage source permit tight control of rectifier voltage overshoots and makes this an optimal tradeoff.

The secondary voltage of the coaxial-wound transformers is a square wave with a peak of $V_i/2$ due to the turns ratio of the transformer. If the converter is operated with an average duty ratio of less than 50%, the output voltage is less than half the input voltage. In this scenario, the clamp diodes D9, D10 bypass the filter inductors L_{f1}, L_{f2} during the active state, leading to peak charging of the output capacitors. In this mode the output current di/dt, which is limited only by the small transformer leakage inductance, is unacceptably large. Thus, the converter cannot be operated with an effective duty ratio less than 50%. However, this does not pose an undue limitation because in the present application, the converter is designed to operate at a nominal effective duty ratio of 80%. At startup, charging of the output bus is accomplished at no load by using a half-bridge mode where only the slave devices Q3, Q4 are switched. L_{co} limits the output current di/dt in this mode and the output bus can be charged to half the input bus voltage, allowing normal operation to commence thereafter. As the dual transformer clamp circuit arrangement is a loss control mechanism for reverse-recovery energy and does not affect the operation at rated output voltage it can be replaced by an idealized bridge and a 1:1 transformer for control analysis.

The commutation inductor L_{co} provides assistance at startup as well as providing commutation energy to the master leg Q1, Q2 at very light loads. As the closed-loop analysis presented in this paper primarily focuses on operation at significant load levels, the contribution of the commutation inductor can be ignored in the analysis. Thus, the analysis of circuit operation from the point of view of power transfer, dynamic model, and controller development is performed using the simplified model shown in Fig. 3.

III. HIGH-FREQUENCY MODAL ANALYSIS

As there are significant time-scale differences between switching dynamics, output filter dynamics, and the averaged dc behavior, the following convention is used for clear identification of variables. Signals at the fast switching cycle time scale ($\sim$ μs) are designated in lower case italics, i_{LF}, v_{CF}, etc. Averaged signals analyzed at timescales at the order of the output LC filter corner ($\sim$ms) are described in lowercase, e.g., i_{LF}, v_{CF}. Small signal behavior of these signals is

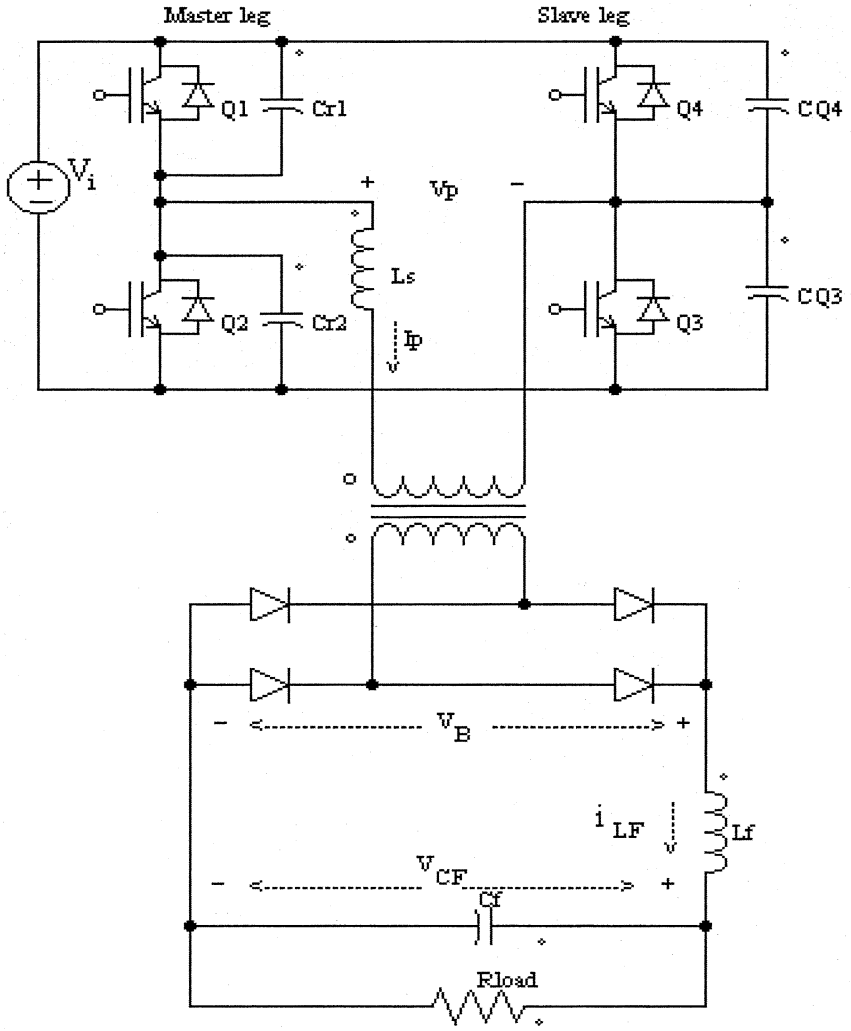

Fig. 3. Simplified isolated loss-limited dc–dc converter topology.

represented by $\tilde{v}_{CF}$, $\tilde{i}_{LF}$. Averaged steady-state dc quantities are represented by capital letters with capital subscripts like I_{LF}, V_{CF}. Peak quantities are represented by $\hat{v}_{CF}$, $\hat{i}_{LF}$.

The converter operation can be divided into various modes, each of which is analyzed in this section. Typical idealized time-domain waveforms under various modes of operation are illustrated in Fig. 7. Consider the converter in Fig. 3 to be initially in the zero state, with both slave leg devices Q3, Q4 open, the master device Q1 closed, and the primary current at zero.

Mode 1 $(0 < t < t_{Ls})$: At time 0, the slave device Q3 is closed, applying V_i across the primary winding of the transformer. The primary current (i_p) increases until it becomes equal to the filter inductor current i_{LF}. During this period, v_B is clamped to zero by the freewheeling secondary rectifiers. The equations governing primary voltage v_P, primary current i_P and bridge output voltage v_B are

$$i_P = \frac{V_i}{L_s}t \quad v_B = 0 \quad v_P = V_i. \tag{1}$$

This mode ends at t_{Ls} where

$$t_{Ls} = \frac{i_{LF}}{V_i}L_s. \tag{2}$$

With nominal values from Table I, the time interval t_{Ls} is seen to be negligibly small ($\sim$100 ns).

Mode 2 $(t_{Ls} < t < t_{Ls} + t_{\rm ON})$: During this interval, the converter is in its power stroke, and the primary current is identical to the filter inductor current

$$i_P = i_{LF} \quad v_B = V_i \quad v_P = V_i. \tag{3}$$

The filter inductor current ramps up by the following equation:

$$\frac{di_{LF}}{dt} = \frac{(V_i - v_{CF})}{L_f}. \tag{4}$$

Mode 2 ends at $t = t_{\rm ON} + t_{Ls}$, when the filter current reaches its peak value $\hat{i}_{LF}$, and the master leg device Q1 is turned off.

Mode 3 $(t_{Ls} + t_{\rm ON} < t < t_{Ls} + t_{\rm ON} + t_R)$: When Q1 is turned off, capacitor C_{r1} and C_{r2} are charged and discharged to V_i and 0, respectively, by filter current i_{LF}. The governing equations are

$$\begin{aligned} i_P &= i_{LF} \\ v_B &= v_P \\ v_P &= V_i - \frac{\hat{i}_{LF}}{C_{r1} + C_{r2}}t. \end{aligned} \tag{5}$$

This mode ends at $t = t_{Ls}+t_{\rm ON}+t_R$ when the primary voltage goes to zero and the antiparallel diode in Q2 starts conducting, at which time device Q2 is turned on. The period t_R is given by

$$t_R = \frac{V_i}{\hat{i}_{LF}}(C_{r1}+C_{r1}). \tag{6}$$

Mode 4 $(t_{Ls}+t_{\rm ON}+t_R < t < t_{Ls}+t_{\rm ON}+t_R+t_Z)$: This is the zero state interval when Q2 and Q3 are on. The load current freewheels in the secondary diodes, while the leakage current freewheels in the primary. The governing equations are

$$\begin{aligned} i_P &= i_{LF} \\ v_B &= 0 \\ v_P &= 0 \end{aligned} \tag{7}$$

$$\frac{di_{LF}}{dt} = \frac{-v_{CF}}{L_f}t. \tag{8}$$

This mode ends at $t = t_{Ls}+t_{\rm ON}+t_R+t_Z$ where t_Z is either determined by the controller action or fixed.

Mode 5 $(t_{Ls}+t_{\rm ON}+t_R+t_Z < t < t_{Ls}+t_{\rm ON}+t_R+t_Z+t_{SC1})$: The slave device Q3 is turned off with di/dt of k_Q. While current is still present in the device Q3, the primary current and voltage are given by

$$\begin{aligned} i_P &= i_{LF} - k_Q t + \frac{k_Q}{\omega}\sin(\omega\cdot t) \\ v_B &= 0 \\ v_P &= -k_Q L_s\{1-\cos(\omega\cdot t)\} \end{aligned} \tag{9}$$

where $\omega = 1/\sqrt{L_s(C_{Q3}+C_{Q4})}$. The primary voltage v_P reaches its largest negative value of $2k_QL_s = 400$ V. This mode ends at $t_{SC1} = i_{LF}/k_Q$ when the device current goes to zero, which for rated conditions is 250 ns. The final primary voltage at the end of this mode (v_{Po}) may be determined to be about 145 V.

Mode 6 $(t_{Ls}+t_{\rm ON}+t_R+t_Z+t_{SC1} < t < t_{Ls}+t_{\rm ON}+t_R+t_Z+t_{SC1}+t_{SC2})$: With no current in the slave devices, the device capacitance C_{Q3} discharges while C_{Q2} charges to V_i by resonating with L_s

$$\begin{aligned} i_P &= \frac{v_{P_0}}{Z_o}\sin(\omega\cdot t) \\ v_B &= 0 \\ v_P &= v_{P_0}\cos(\omega\cdot t) \end{aligned} \tag{10}$$

where $Z_0 = \sqrt{L_S/(C_{Q3}+C_{Q4})}$. This mode terminates when the primary voltage reaches zero at $t_{SC2} = \pi/(2\omega)$, which for given system parameters is ~78 ns.

Mode 7 $(t_{Ls}+t_{\rm ON}+t_R+t_Z+t_{sn} < t < t_{Ls}+t_{\rm ON}+t_R+t_Z+t_{sn}+t_D)$: Both slave devices are off, while the master device Q2 is on. The equations governing this condition are

$$i_P = 0 \quad v_B = 0 \quad v_P = 0. \tag{11}$$

Mode 7 is a zero state, representing the completion of one half cycle. This mode ends when slave device Q4 is turned on and a complementary negative half cycle is initiated, with identical modes. The slave leg dead time, t_D (between turn off of Q3 and turn on of Q4) is 2 μs, which is the total allowable time for Modes 5, 6, and 7. Thus, t_D is less than 2 μs.

Transformer primary voltage waveform obtained from the prototype converter is shown in Fig. 4. A detailed viewpoint of the primary voltage and current during switching obtained experimentally is shown in Figs. 5 and 6. Typical waveforms obtained using a piecewise modal analysis are shown in Fig. 7. Excellent correlation is observed between the theoretical waveforms and the experimental results from the prototype.

Examining the waveform of v_P and i_P under Modes 5 and 6, it may be observed that the primary voltage shows a narrow and small blip during this period. As the width of this blip is 300

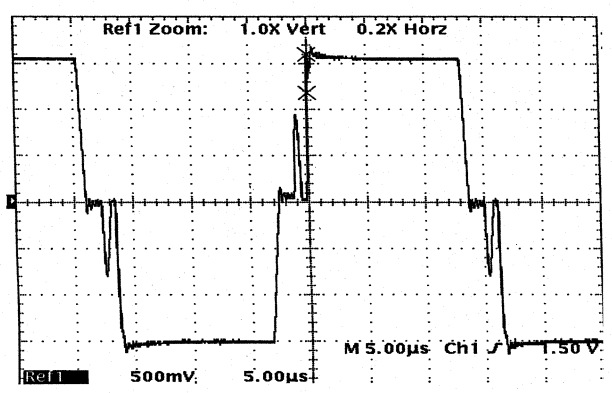

Fig. 4. Transformer primary winding voltage waveform from the experimental prototype converter (250 V/div, 5 μs/div).

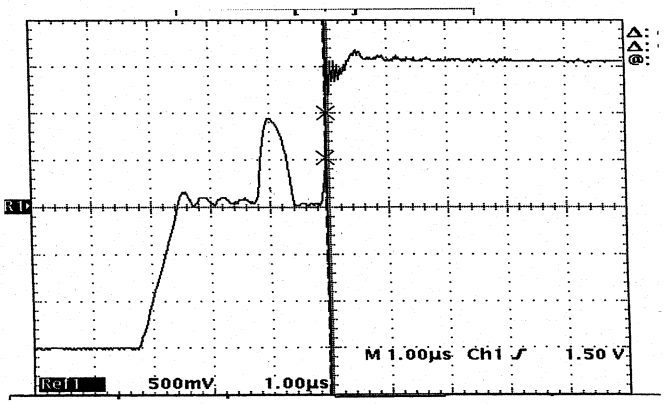

Fig. 5. Transformer primary winding voltage waveform from the experimental prototype converter (250 V/div, 1 μs/div).

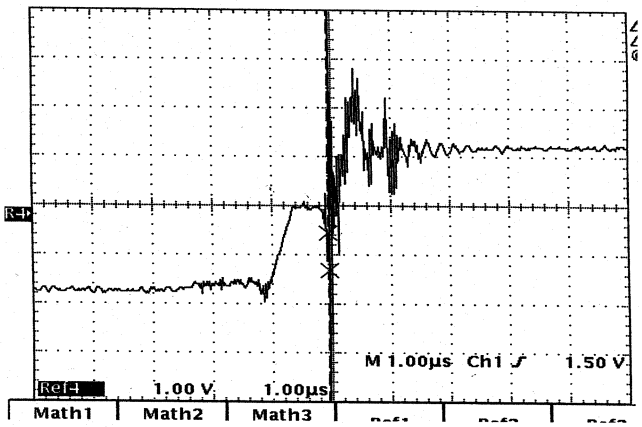

Fig. 6. Transformer primary current waveform from the experimental prototype converter (100 A/div, 1 μs/div).

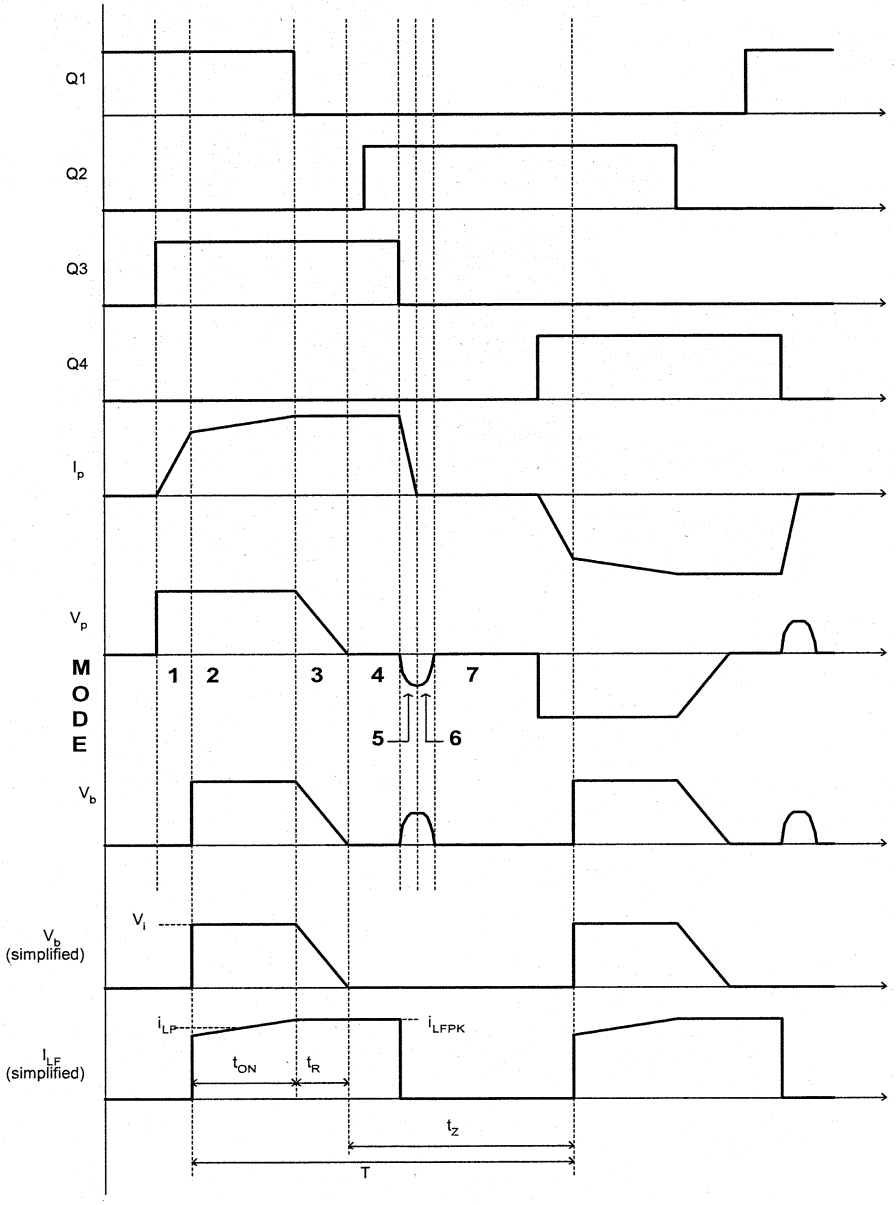

Fig. 7. Typical operating waveforms under various operating modes.

ns and the voltage never exceeds about 400 V, the volt-seconds contribution due to these modes is very small, and may be ignored. Similarly, Modes 1 and 7 can also be lumped into Modes 2 and 4, respectively. By eliminating these modes, nonidealities in the slave leg switching are ignored.

Also, the bridge voltage v_B is essentially equal to the rectified value of the primary voltage v_P. The bridge voltage and the filter inductor current waveform under these simplifying assumptions are illustrated in the last two waveforms of Fig. 7. The system equivalent circuit can now be reduced to a source v_B, driving the output filter as illustrated in Fig. 8.

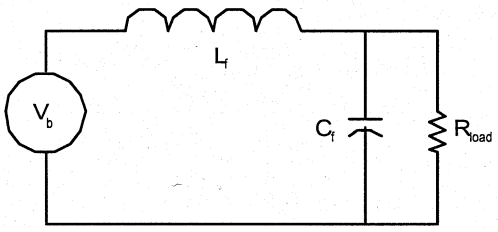

Fig. 8. Simplified equivalent circuit useful for dynamic and static analysis.

IV. Dynamic Analysis

The dynamic behavior of the system can be characterized by state equations of the output filter alone, while incorporating the averaged high-frequency dynamics due to resonant transitions [6]

$$\frac{di_{LF}}{dt} = \frac{v_B - v_{CF}}{L_f} = \boldsymbol{f}(\cdot) \tag{12}$$

$$\frac{dv_{CF}}{dt} = \frac{i_{LF} - \frac{v_{CF}}{R_{\text{load}}}}{C_f} = \boldsymbol{g}(\cdot). \tag{13}$$

In peak current-control mode, the controller generates a peak current command $\hat{i}$ that is compared with the inductor current to determine switching instants. A compensating ramp m_c is subtracted from $\hat{i}$ for the stability of the current-mode controller [7]. From this control action, we obtain

$$\hat{i} - m_c t_{\rm ON} = \hat{i}_{LF}. \tag{14}$$

From Mode 2 equations and boundary conditions,

$$\hat{i}_{LF} - i_{LF} = \frac{[V_i - v_{CF}]}{L_f}\frac{t_{\rm ON}}{2}. \tag{15}$$

From Mode 3 equations and boundary conditions,

$$\hat{i}_{LF} = \frac{[C_{r1} + C_{r2}]V_i}{t_R}. \tag{16}$$

Also, the following equations can be written for each cycle:

$$t_Z + t_R + t_{\rm ON} - T = 0 \tag{17}$$

$$V_i\left[t_{\rm ON} + \frac{t_R}{2}\right] = v_B T. \tag{18}$$

Equations (14)–(18) can be solved first with a fixed time period T for the time variables t_Z, t_R, $t_{\rm ON}$, and intermediate variables v_B, $\hat{i}_{LF}$. These can be expressed as functions of state variables i_{LF}, v_{CF}, input $\hat{i}$, and parameters V_i, C_{r1}, C_{r2}, L_f, m_c as follows:

$$v_B, \hat{i}_{LF}, t_R, t_{\rm ON}, t_Z = \phi\left(i_{LF}, v_{CF}, \hat{i}, V_i, C_{r1}, C_{r2}, L_f, m_c, T\right). \tag{19}$$

This control mode corresponds to fixed-frequency variable-off-time operation.

Alternatively, the equations can be solved with a fixed time period t_Z, and another set of functions can be derived as follows:

$$v_B, \hat{i}_{LF}, t_R, t_{\rm ON}, T = \phi\left(i_{LF}, v_{CF}, \hat{i}, V_i, C_{r1}, C_{r2}, L_f, m_c, t_Z\right). \tag{20}$$

This control mode corresponds to variable-frequency fixed-off-time operation.

V. Static Analysis

The static equations can be obtained by setting the left-hand side of (12) and (13) to zero. This yields two additional algebraic equations

$$0 = V_B - V_{CF} \quad 0 = I_{LF} - \frac{V_{CF}}{R_{\rm load}} \tag{21}$$

subject to the constraints imposed by the algebraic (14)–(18), which, at steady state become

$$\begin{aligned} \hat{I} - m_c t_{\rm ON} &= \hat{I}_{LF} \\ \hat{I}_{LF} - I_{LF} &= \frac{[V_i - V_{CF}]}{L_f}\frac{t_{\rm ON}}{2} \\ \hat{I}_{LF} &= \frac{[C_{r1} + C_{r2}]V_i}{t_R} \\ V_i\left[t_{\rm ON} + \frac{t_R}{2}\right] &= V_B T \\ t_Z + t_R + t_{\rm ON} - T &= 0. \end{aligned} \tag{22}$$

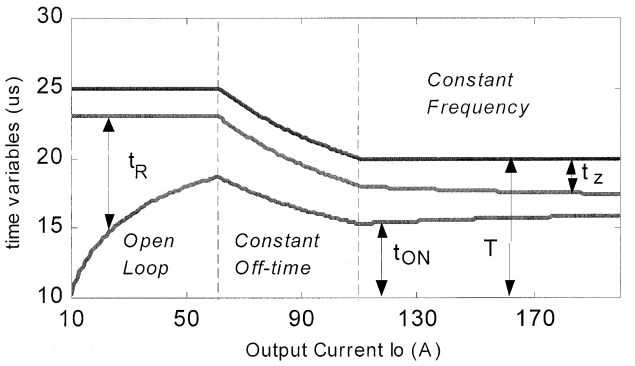

Fig. 9. Variation of interval sections of the switching period.

Knowing that the rated value of V_{CF} is 750, these seven equations can be solved for dc quantities V_B, I_{LF}, $\hat{I}_{LF}$, $\hat{I}$, and time variables t_Z, t_R, $t_{\rm ON}$ with fixed known T to obtain steady-state values for the constant-frequency mode. Similarly, if t_Z is assumed to be fixed and known, the other time variables t_R, $t_{\rm ON}$, T can be obtained for the constant off-time mode. These solutions obtained for both modes are checked against the following limits:

$$t_Z \geq 2\ \mu{\rm s}: \text{ minimum dead time} \tag{23}$$

$$T \leq 25\ \mu{\rm s}: \text{ minimum frequency} \tag{24}$$

$$T \geq 20\ \mu{\rm s}: \text{ maximum frequency.} \tag{25}$$

The lower limit in t_Z ensures adequate time for lossless commutation; the upper limit on T ensures that the transformer peak flux is below the saturation level and the lower limit on T ensures that the power device switching losses are below the design value. At heavy-load conditions, only the solution obtained for the constant-frequency mode satisfies (23)–(25) and the solution for the constant-off-time mode is discarded as it violates (24). This holds true until the load is reduced to about 60%, when the constant-frequency solution violates (25) and, hence, is discarded. However, at this load, the constant-off-time mode solution satisfies (23)–(25). This solution can be used for loads reduced down to about 30%, when (23) is violated.

The converter controller is encoded into a high-speed state machine, which seamlessly transitions from fixed-frequency control at heavy loads to constant off time for lighter loads. When the load current is reduced further, the converter operates in a constant-off-time constant-frequency open-loop mode. The static solutions for this open-loop case can be obtained by solving (21) and (22), assuming both T, t_Z fixed but with V_{CF} unknown. Fig. 9 shows the sectioning of the time period into the various components $t_{\rm ON}$, t_Z and t_R for different values of load currents and the three distinct operating modes can be identified.

Fig. 10 shows the extension of the operating region of the converter achieved due to the multimodal control method when compared with a fixed-frequency current-mode controller at 25 kHz. A fixed-frequency current-mode controller would have to operate at 20 kHz in order to realize this operating region. However, operating at such lower frequencies over the entire range would result in larger magnetic component losses at

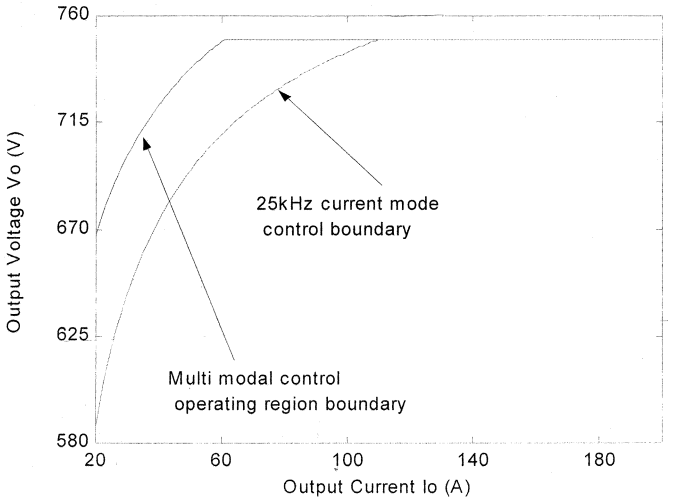

Fig. 10. Variation of output voltage obtainable as function of load level.

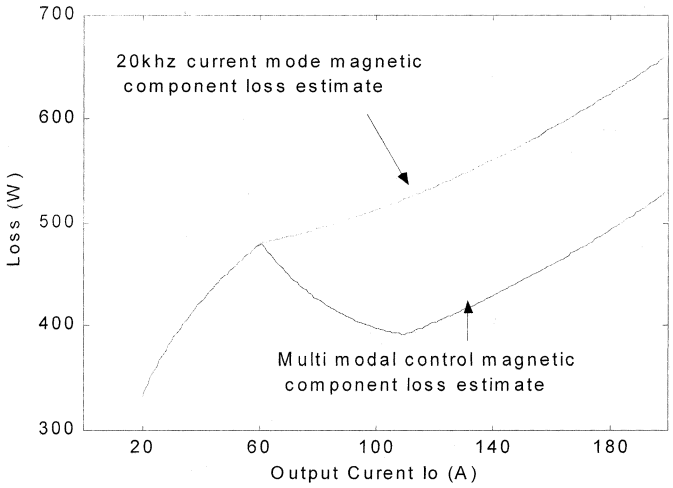

Fig. 11. Variation of magnetic component losses as function of load level.

heavy loads. The transformers in the dc–dc converter were manufactured using litz wire for primary windings, square copper tubing for secondary windings, and ferrite E-E sets for core material. The copper losses can be calculated directly for the litz winding from the manufacturers data sheet [8], while a very good estimate for the secondary winding can be obtained using skin-depth approximations [9]. The core loss can be determined using the ferrite material parameters for "P" type material [10]. Fig. 11 illustrates the variation of total core and copper losses with the multimode control scheme operating between 20–25 kHz in comparison with fixed-frequency current-mode control operating at 20 kHz and the benefits realized due to multimodal control. The efficiency of the prototype power converter under various modes of operation was measured to be over 96% confirming the expectations. Details of the power circuit design and steady-state operating conditions have been presented in [1]. A computer-simulation-based comparative evaluation of the proposed converter with other approaches for realizing such isolated high-power system indicates that the proposed approach provides superior performance [4] from a thermal point of view.

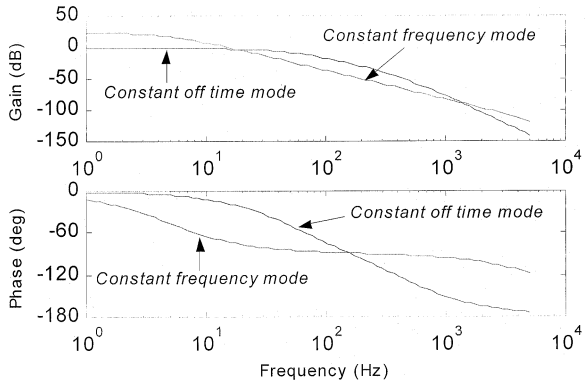

Fig. 12. Gain and phase of $\tilde{V}_{CF}/\tilde{i}_{PK}$ at constant off time mode: $V_o = 750$ V, $I_o = 70$ A, $F = 22.9$ kHz; constant frequency mode: $V_o = 750$ V, $I_o = 150$ A, $F = 25$ kHz.

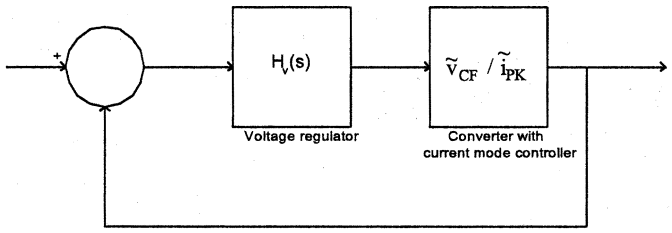

Fig. 13. Block diagram of the converter voltage regulator.

VI. Loop Gain and Compensator Design

Using the steady-state solution obtained from (21) and (22) and computing the Jacobian of the system described in (12)–(18), the state-space description of the small-signal behavior [11] of the system can be obtained for both control modes as follows:

$$\begin{pmatrix} \frac{d\tilde{i}_{LF}}{dt} \\ \frac{d\tilde{v}_{CF}}{dt} \end{pmatrix} = \begin{pmatrix} \frac{\partial \boldsymbol{f}}{\partial i_{LF}} & \frac{\partial \boldsymbol{f}}{\partial v_{CF}} \\ \frac{\partial \boldsymbol{g}}{\partial i_{LF}} & \frac{\partial \boldsymbol{g}}{\partial v_{CF}} \end{pmatrix} \begin{pmatrix} \tilde{i}_{LF} \\ \tilde{v}_{CF} \end{pmatrix} + \begin{pmatrix} \frac{\partial \boldsymbol{f}}{\partial i_{PK}} \\ \frac{\partial \boldsymbol{g}}{\partial i_{PK}} \end{pmatrix} \begin{pmatrix} \tilde{\hat{i}} \end{pmatrix}. \tag{26}$$

The control to output transfer functions can be evaluated at the steady-state operating points under the various modes of control. These are shown in Fig. 12 for two steady-state operating points corresponding to the two different control modes.

The block diagram of the outer loop voltage regulator is illustrated in Fig. 13. As the converter was designed to reject single-phase loading up to 72 Hz, it was desirable to extend the loop gain crossover up to a few hundred hertz. The voltage regulator also was required to have infinite gain at dc and reject the switching-frequency harmonics. These goals were achieved by using a proportional plus integral (PI) regulator with a high-frequency roll-off whose transfer function is given by

$$H_V(s) = K_p \frac{1 + \frac{s}{\omega_z}}{s\left(1 + \frac{s}{\omega_p}\right)} \tag{27}$$

where $\omega_z = 2 \cdot \pi \cdot 72$, $\omega_p = 2 \cdot \pi \cdot 2700$.

The gain K_p was chosen to extend the unity gain bandwidth while maintaining a stable phase margin of about 60°. The combined loop gains including the regulator for the two operating points illustrated in Fig. 12 are shown in Fig. 14. Several units

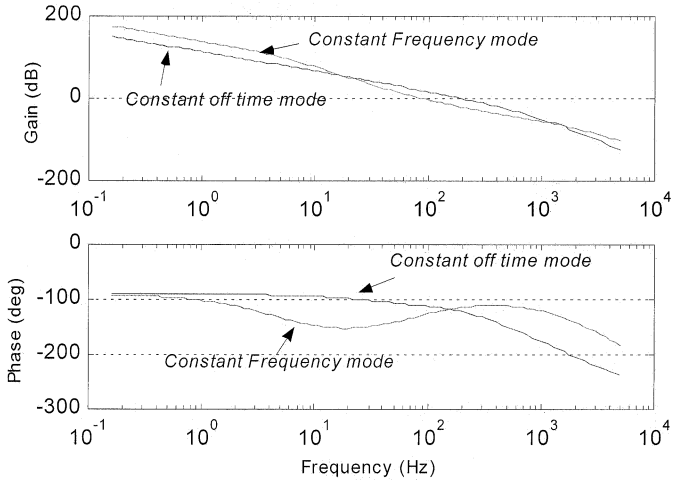

Fig. 14. Frequency response of voltage regulator loop gain.

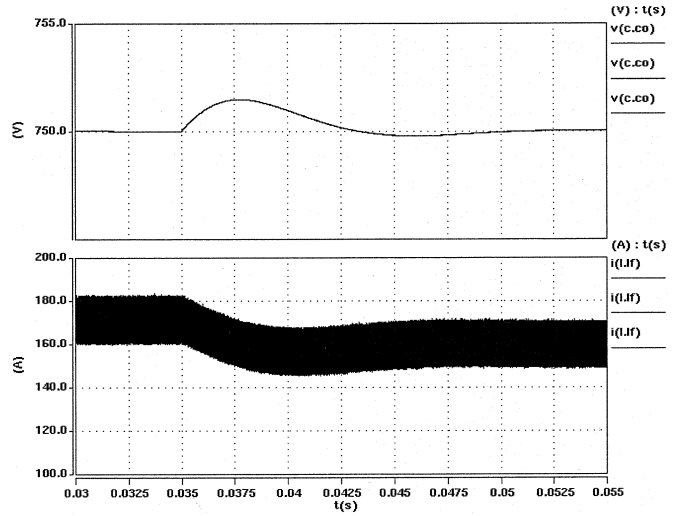

Fig. 15. SABER waveforms illustrating the variation of output voltage and inductor current to a step change in load.

of the converter power circuit incorporating the controller developed herein have been produced and incorporated for feeding power to multilevel cascaded H-bridge inverters. Extensive tests at various power levels have been conducted and have confirmed stable and acceptable operation.

Furthermore, a detailed simulation of the converter was also performed using SABER computer software. The model included insulated gate bipolar transistor (IGBT) device models for switching devices and a complete model for the transformer. The waveforms of the response of the voltage regulator for a step change in load are shown in Fig. 15, for the constant-frequency-control mode, near rated operating point. The traces indicate stable operation of the controller with a settling time of the output voltage to be about 15 ms.

VII. Open-Loop Operation

Peak current control regulates the dc component of the primary current to zero on a cycle-by-cycle basis, keeping the transformer out of saturation. At light loads and low input voltages, the commanded peak current is too high to yield any

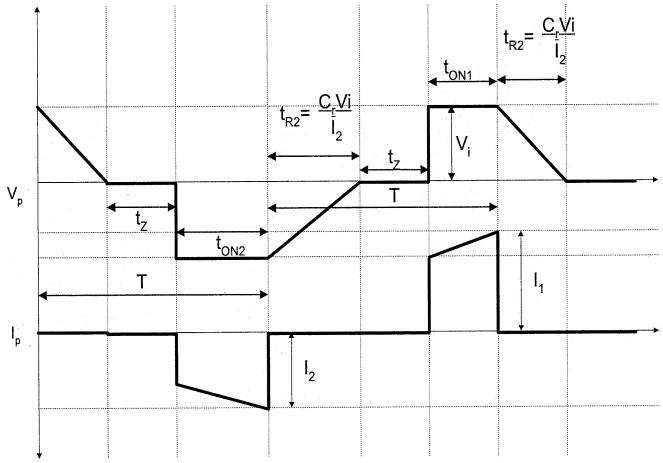

Fig. 16. Idealized open-loop operation.

intersection points with the measured primary current, unless the frequency is reduced. The converter frequency cannot be reduced further as it will violate (23) and lead to high core losses in the transformer. The converter frequency hence fixed at 20 kHz and it is operated in the open-loop mode without peak current control, and the output voltage is reduced as seen in Fig. 10. During open-loop converter operation, small variations in device and parasitic voltage drops can integrate up to lead to large flux excursions in the transformer, which are reflected as large imbalances in the magnetizing current. If there is an unbalance present in the transformer magnetizing current the applied voltage and current waveforms for the converter will be asymmetric as shown in Fig. 16. The unbalance in magnetizing current manifests itself as a difference in the turn-off current for the positive and negative cycles, leading to differing resonant times t_{R1} and t_{R2}. Fixed-frequency controllers, in the open-loop mode, operate with a constant on time $t_{\rm ON}$ for the switch, while the new scheme operates by timing successive switch turn-off instances which leads to differing on times $t_{\rm ON1}$ and $t_{\rm ON2}$. The net average voltage $(V_{\rm avg})$ applied over a switching cycle can be shown to be

$$V_{\rm avg} = -\frac{3V_i^2 C_r}{4T}\left(\frac{I_1 - I_2}{I_m^2}\right). \tag{28}$$

Recognizing that the flux imbalance $\Delta\phi$ is $L_m(I_1 - I_2)$, it can be shown that it decays at an exponential rate given by

$$\Delta\phi = \Delta\phi_o \boldsymbol{e}^{-3V_i^2 C_r/4TL_m I_m^2 t}. \tag{29}$$

A plot of the decay of flux imbalance as a function of time under classical constant on-time control mode and the new open-loop control mode is shown in Fig. 17. The rapid decay of flux imbalance may be readily observed from the figure along with the improved response of the new scheme.

VIII. Conclusions

A new loss-limited dc–dc converter topology employing one resonant soft-switching pole and one phase-shifted hard-switching pole has been introduced recently for high-power isolated dc–dc power conversion [1]. Comparative

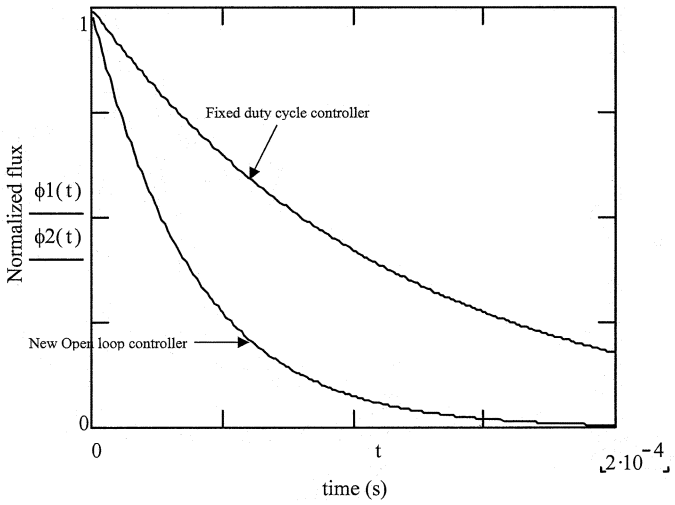

Fig. 17. Decay of flux imbalance with traditional and proposed methods.

analysis of this topology with alternate dc–dc converter topologies has demonstrated the viability of the new topology [4]. A new multimodal control scheme that extends operating region while maintaining reduced magnetic component losses has been developed and implemented for the loss-limited full-bridge dc–dc converter. The paper has presented a detailed modal analysis describing the operation of the converter. The analytical results from the modal analysis have been approximated using numerical justifications to develop a simplified dynamic model. The simplified dynamic model is used to develop multimodal control techniques and small-signal control transfer functions which are used to design a voltage regulator that is stable under all modes of operation. The operation of the controller and the converter operation have been verified in production units. Converter simulation waveforms have been used to illustrate the dynamic response of the system under step changes in load. Negative feedback mechanisms that lead to transformer flux balancing under open-loop operation have been analyzed and exploited for improved dynamic performance.

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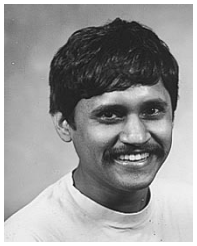

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