SPATIAL INHOMOGENEOUS BARRIER HEIGHTS AT GRAPHENE/ SEMICONDUCTOR SCHOTTKY JUNCTIONS

by

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ABSTRACT

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Under the Supervision of Professor Lian Li

Graphene, a semimetal with linear energy dispersion, forms Schottky junction when interfaced with a semiconductor. This dissertation presents temperature dependent current-voltage and scanning tunneling microscopy/spectroscopy (STM/S) measurements performed on graphene Schottky junctions formed with both three and two dimensional semiconductors.

To fabricate Schottky junctions, we transfer chemical vapor deposited monolayer graphene onto Si- and C-face SiC, Si, GaAs and MoS_2 semiconducting substrates using polymer assisted chemical method. We observe three main type of intrinsic spatial inhomogeneities, graphene ripples, ridges and semiconductor steps in STM imaging that can exist at graphene/semiconductor junctions. Tunneling spectroscopy measurements reveal fluctuations in graphene Dirac point position, which is directly related to the Schottky barrier height. We find a direct correlation of Dirac point variation with the topographic undulations of graphene ripples at the graphene/SiC junction. However, no such correlation is established at graphene/Si and Graphene/GaAs junctions and Dirac point variations are attributed to surface states and trapped charges at the interface. In addition to graphene ripples and ridges, we also observe atomic scale moiré patterns at graphene/MoS_2 junction due to van der Waals interaction at the interface. Periodic topographic

modulations due to moiré pattern do not lead to local variation in graphene Dirac point, indicating that moiré pattern does not contribute to fluctuations in electronic properties of the heterojunction.

We perform temperature dependent current-voltage measurements to investigate the impact of topographic inhomogeneities on electrical properties of the Schottky junctions. We observe temperature dependence in junction parameters, such as Schottky barrier height and ideality factor, for all types of Schottky junctions in forward bias measurements. Standard thermionic emission theory which assumes a perfect smooth interface fails to explain such behavior, hence, we apply a modified emission theory with Gaussian distribution of Schottky barrier heights. The modified theory, applicable to inhomogeneous interfaces, explains the temperature dependent behavior of our Schottky junctions and gives a temperature independent mean barrier height. We attribute the inhomogeneous barrier height to the presence of graphene ripples and ridges in case of SiC and MoS_2 while surface states and trapped charges at the interface is dominating in Si and GaAs.

Additionally, we observe bias dependent current and barrier height in reverse bias regime also for all Schottky junctions. To explain such behavior, we consider two types of reverse bias conduction mechanisms; Poole-Frenkel and Schottky emission. We find that Poole-Frenkel emission explains the characteristics of graphene/SiC junctions very well. However, both the mechanism fails to interpret the behavior of graphene/Si and graphene/GaAs Schottky junctions. These findings provide insight into the fundamental physics at the interface of graphene/semiconductor junctions.

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LIST OF ABBREVIATIONS

2D	Two-dimensional
3D	Three-dimensional
AFM	Atomic force microscopy
BOE	Buffer oxide etching/etchant
BZ	Brillouin zone
C-V	Capacitance-voltage
CVD	Chemical vapor deposition
dI/dV	Differential tunneling conductance
DI	Deionized
DOS	Density of states
EG	Epitaxial graphene
FE	Field emission
FWHM	Full width at half maximum
HOPG	Highly oriented pyrolytic graphite
I-V	Current-voltage
I-V-T	Current-voltage-temperature
M-S	Metal-semiconductor
PF	Poole-Frenkel
PMMA	Polymethyl methacrylate
PR	Photoresist
SBH	Schottky barrier height
STM	Scanning tunneling microscopy
STS	Scanning tunneling spectroscopy

TB	Tight binding
TE	Thermionic emission
TFE	Thermionic field emission
UHV	Ultra-high vacuum
UV	Ultraviolet
vdW	Van der Waals

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Chapter 1
Introduction

Most of the modern semiconductor industry is based on silicon that has a small band gap (1.12 eV), lower cost and relatively large working temperature range (-65 to150^{o}C) [1-3]. On the other hand SiC, GaAs and other semiconductors are useful in more specific applications such as high power or photovoltaic devices [4, 5]. However, silicon and other semiconductor devices are reaching to their limits in fabrication and performance due to a continuous demand of smaller size electronic components [6]. Therefore, new materials with improved electronic properties at smaller scale are required for the development of next generation electronic devices. In the search of such new materials, two dimensional (2D) materials offer a possible solution due to their planar structures with a thickness of less than a nanometer.

Graphene, a monolayer of carbon atoms, is among the few promising 2D materials because of its high electron mobility [10^5 cm^2/Vs], excellent thermal conductivity [5300 W/mK], large Young's modulus [~2.5 Tpa], superior intrinsic carrier velocity [10^6 cm/s] and chemically inert nature [7-10]. Despite having all these qualities, graphene cannot be used all alone in the industry because of its 2D nature that still requires a substrate to support it. It is speculated that the graphene heterojunctions with supporting substrate might play an important role in future hybrid electronic systems. Of particular interest is graphene/semiconductor Schottky junctions which have been demonstrated in solar cells, photodetectors, gas sensors, and barristor [11-18]. Despite its use in various applications, only few studies have been performed to understand the physics of the graphene/semiconductor interface [19-22]. In most of the studies, thermionic emission (TE) theory is used to extract the Schottky barrier height and ideality factor of graphene/semiconductor Schottky junctions, however, TE theory failed to explain the observed temperature dependence of

barrier height and ideality factor. For conventional metal/semiconductor Schottky junctions, such behavior is attributed to interface inhomogeneities coming from defects/atomic steps in semiconductor and thickness modulation/grain boundaries in metal [23].

In graphene/SiC Schottky junctions, fluctuations in graphene's Dirac point position originated from inhomogeneous interface has been observed [24]. The presence of graphene ripples and ridges has been speculated as the sources of such inhomogeneous interface. However, a direct correlation in temperature dependent electrical properties and spatial inhomogeneous interface has not been known yet. Answer of such question is crucial for the graphene based electronic industry. In this dissertation our focus is on the investigation of possible sources of interface inhomogeneities in graphene/ semiconductor Schottky junctions. Furthermore, a direct correlation in spatial inhomogeneous interface and electrical transport properties is also established for such Schottky junctions. This dissertation consists of nine chapter including introduction.

Chapter 2 reviews the physics of conventional metal-semiconductor Schottky junctions. The formation of ideal Schottky junction is discussed in section 2.1, followed by non-ideal contributions in section 2.2. Transport mechanisms in forward and reverse biased Schottky junctions are discussed in section 2.3. The experimental methods of barrier height measurements and models to explain barrier inhomogeneity are discussed in section 2.4 and 2.5 respectively.

Chapter 3 provides a brief introduction of electrical properties of graphene in the section 3.1. Detailed description of graphene synthesis using chemical vapor deposition and its transfer process onto an arbitrary substrate is presented in the section 3.2.

Chapter 4 lays out the photolithography methods used to fabricate graphene Schottky diode. Furthermore, it explains the working principle of the two main characterization techniques used in

this dissertation; temperature dependent current-voltage (I-V) measurements and scanning tunneling microscopy/spectroscopy (STM/S).

Chapter 5 presents STM/S and temperature dependent I-V measurements of graphene Schottky junctions with chemically inert Si- and C-face SiC substrates. Here, temperature dependence of junction parameters is found directly correlated to topographic corrugations in absence of interface states.

Chapter 6 explains STM/S and temperature dependent I-V measurements of graphene/Si and graphene/GaAs Schottky junctions. Similar to graphene/SiC case, a temperature dependence of junction parameters is observed. However, no direct correlation is found in topographic corrugations and junction parameters that is further attributed to presence of interface states.

2D layered semiconductors such MoS_2 are suggested as an alternate substrate to overcome the previously discussed issue of spatial inhomogeneities. The temperature dependent I-V characteristics and STM/S measurements of graphene/MoS_2 Schottky junctions are presented in chapter 7. Similar to conventional semiconductor case, a temperature dependence of junction parameters is observed in graphene/MoS_2 junction too. Such behavior is clearly opposite to the speculation of atomically flat interface between graphene and MoS_2 and attributed to graphene ripples and ridges.

Chapter 8 explains the temperature and electric field dependence of the reverse bias current (and barrier height) in graphene/semiconductor Schottky junctions. Poole-Frenkel conduction mechanism is found dominating in graphene/SiC junctions which explains the field dependence of barrier height. However, such behavior could not be explained neither by Poole-Frenkel nor by Schottky emission mechanism in graphene/GaAs and graphene/Si junctions.

Chapter 9 concludes the dissertation and provides future prospects.

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Chapter 2
Schottky Junctions Basics

2.1 Introduction

A rectifying metal-semiconductor junction is known as a Schottky junction after German Physicist W. H. Schottky who first proposed a model of the barrier formation [1]. In the beginning of the 20^{th} century, Schottky contacts were fabricated by employing a sharpened metallic wire in contact with an exposed semiconductor surface which proved to be useful in early radio wave detectors. However, due to their unreliable characteristics, such contacts were replaced by rectifiers obtained by deposition of a thin metal film on a clean semiconductor surface. Since then Schottky rectifiers have played an essential role in many electronic and optoelectronic devices.

In this chapter, the formation of ideal Schottky junctions and a description of the electrostatics present in such junctions is discussed in section 2.1.1 and 2.1.2, respectively. Non-ideal contributions to Schottky junctions are presented in section 2.1.3. The carrier transport mechanism in the forward bias regime is given in section 2.2, followed by a discussion of the reverse bias conduction mechanism in section 2.3. Different methods to measure the Schottky barrier height are given in section 2.4. In section 2.5, sources of barrier height inhomogeneity and models to explain those are discussed.

2.1.1 Formation of ideal Schottky junction

A Schottky junction is formed when a metal comes into contact with a semiconductor. The difference in their respective work functions forms an energy barrier at the interface, called Schottky barrier [1]. The Schottky barrier height (SBH) of an ideal metal/n-type semiconductor (M-S) junction can be expressed using the Schottky-Mott model [2, 3]

$$\boldsymbol{\phi_B = \Phi_M - \chi} \quad [2.1]$$

where ϕ_B is the Schottky barrier height, Φ_M is metal work function and χ is electron affinity of the semiconductor. It is important to mention that the contribution from interface states and barrier lowering due to an image force is not considered in an ideal junction [2, 3].

The schematic energy band diagram of an isolated metal and n-type semiconductor is shown in Fig. 2.1 (a). The vacuum level E_0 is shown as a reference level. The work function (Φ) of a material is the minimum energy required to remove one electron from a solid to a point in the vacuum and it is equal to the energy difference between the vacuum level (E_0) and the Fermi energy (E_F) of the material. For metals, Φ_M is an invariant quantity because $E_C \approx E_F$, where E_C is conduction band energy. However, the semiconductor work function $\left(\Phi_S = (E_0 - E_F)\right)$ is a function of E_F that depends on doping, therefore, another constant quantity χ is used in Equation [2.1]. This parameter can be expressed as the difference in vacuum and conduction band energies i.e. $\chi = E_0 - E_C$. Before making contact, the Fermi level of the semiconductor is higher than that of the metal. However, once both are brought into contact, electrons flow from the semiconductor into the lower energy states of the metal to establish an equilibrium Fermi level as shown in Fig. 2.1 (b). Here, ϕ_B is the potential barrier seen by the electrons travelling from the metal to the semiconductor. The magnitude of ϕ_B can be obtained from Equation [2.1]. A similar energy barrier is seen by the semiconductor conduction band electrons who move into the metal. This barrier is called the built-in potential (V_{bi}) and given as

$$V_{bi} = \phi_B - \Phi_S = \phi_B - (E_C - E_F) = \phi_B - kT\, ln\frac{N_C}{N_D} \quad [2.2]$$

where N_C and N_D are the effective density of states of the conduction band and the donor concentrations of an n-type semiconductor, respectively.

When a positive voltage is applied to the semiconductor with respect to the metal, the metal to semiconductor barrier ϕ_B remains constant but the semiconductor to metal barrier V_{bi} increases which prohibits electron flow from the semiconductor to the metal [4]. Under this condition the device is said to be reverse biased. Conversely, in the forward bias regime (negative voltage to the semiconductor with respect to positive metal) V_{bi} is reduced while ϕ_B again remains constant. The lowering of the barrier allows electrons to flow more easily from the semiconductor into the metal. The energy band diagrams for both reverse and forward bias conditions are shown in Fig. 2.2 (a) and (b).

It is important to mention that a Schottky junction between a metal and an n-type semiconductor forms only if $\Phi_S < \Phi_M$. When $\Phi_S > \Phi_M$, the majority charge carriers can move freely from the metal into the semiconductor without being opposed by a barrier. This type of M-S contact is called an Ohmic contact. The energy band representation of a M-S (n-type) Ohmic contact is shown in Fig. 2.3 (a) and (b). Oppositely for a metal-p-type semiconductor junction one can have Ohmic contact for $\Phi_S < \Phi_M$ and Schottky contact for $\Phi_S > \Phi_M$. The barrier height of an ideal metal-p-type semiconductor Schottky junction can be expressed by [4]

$$(\phi_B)_{p-type} = \frac{E_g}{q} - (\Phi_M - \chi) = \frac{E_g}{q} - (\phi_B)_{n-type} \qquad [2.3]$$

All possible combinations of metal-semiconductor junctions are given in Table 2.1:

Work function relation	n-type semiconductor	p-type semiconductor
$\phi_S < \phi_M$	Schottky	Ohmic
$\phi_S > \phi_M$	Ohmic	Schottky

2.1.2 Electrostatics of a Schottky junction

One needs to solve Poisson's equation for a better understanding of a Schottky junction. The solution of Poisson's equation gives information about the spatial variation of the electric potential and field, the depletion layer width, and the capacitance of a Schottky junction. In Schottky junctions, charge depletes from the M-S interface into the bulk of semiconductor to form a depletion region where the Poisson's equation is given by [4]

$$\frac{d^2V(x)}{dx^2} = -\frac{\rho}{\epsilon_S} \qquad [2.4]$$

where ϵ_S is the dielectric constant of the semiconductor. We approximate the charge density as a step function and the charge density distribution in depletion region (of width W) can be given as

$$\rho(x) = \begin{cases} qN_D \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 0 \le x \le W \\ 0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots x > W \end{cases} \qquad [2.5]$$

The above equation serves as boundary conditions for Equation [2.4]. No consideration is needed for a metal because of a zero electric field and constant potential inside a metal. The spatial distribution of the electric field on the semiconductor side can be obtained from Equation [2.4] as $E = -dV/dx$,

$$\frac{dE(x)}{dx} = \frac{\rho}{\epsilon_S} = \frac{qN_D}{\epsilon_S} \qquad 0 \le x \le W \qquad [2.6]$$

at $x = W, E = 0$, therefore, the solution of Poisson's equation gives the following expression for the electric field

$$E(x) = \frac{qN_D}{\epsilon_S}(x - W) \qquad 0 \le x \le W \qquad [2.7]$$

and the maximum electric field E_{max} can be obtained by putting $x = 0$ in Equation [2.7]

$$E_{max} = \frac{qN_D W}{\epsilon_S} \qquad [2.8]$$

Since $E = -dV/dx$, the distribution of electrostatic potential in depletion region is

$$\frac{dV}{dx} = -E = \frac{qN_D}{\epsilon_S}(W - x), \qquad 0 \le x \le W \qquad [2.9]$$

$$V(x) = -\frac{qN_D}{2\epsilon_S}(W - x)^2, \qquad 0 \le x \le W \qquad [2.10]$$

Furthermore, by applying the boundary conditions for the potential [$V(x = 0) = -V_{bi}$ and $V(x = W) = 0$], the depletion layer width can be given as

$$W = \sqrt{\frac{2\epsilon_S V_{bi}}{qN_D}} \qquad [2.11]$$

It is clear from Equation [2.11] that the depletion layer width is directly proportional to the square root of the built-in potential and is inversely proportional to the semiconductor dopant density. Furthermore, when a bias voltage is applied to the Schottky junction then V_{bi} will be replaced by $(V_{bi} - V_a)$ resulting in a decrease in W for a forward bias voltage ($V_a > 0$) and increase with a reverse bias voltage ($V_a < 0$). Lastly, the electric field can also be expressed in terms of the built in potential by substituting W from Equation [2.11] to [2.8]

$$E_{max} = \sqrt{\frac{2qN_D V_{bi}}{\epsilon_S}} \qquad [2.12]$$

The depletion layer capacitance can also be obtained by calculating the space charge density Q_S [4]

$$Q_S = qN_D W = \sqrt{2qN_D\epsilon_S(V_{bi} - V_a)} \qquad [2.13]$$

Now, differentiation of the above equation with respect to the applied voltage gives the depletion layer capacitance per unit area

$$C_d = \frac{dQ_S}{dV_a} = \sqrt{\frac{qN_D\epsilon_S}{2(V_{bi} - V_a)}} \qquad [2.14]$$

Equation [2.14] shows that the depletion layer capacitance is inversely proportional to square root of the applied bias voltage.

2.2 Non-ideal contributions to Schottky junctions

In the previous section, we solved the electrostatics of an ideal Schottky junction to obtain key parameters that define such a device using the Schottky-Mott model. This model neglects the contribution from surface states, defects, and image force lowering and how it effects the performance of Schottky device. However, in reality surface states are an inherent property of a semiconductor and need to be considered for a proper understanding. Furthermore, other factors such as thermionic field emission and direct tunneling through the barrier can also alter the actual SBH from the value obtained by using the Schottky-Mott model [4, 5]. In fact, for a high surface state density semiconductor, the barrier height does not depend on the metal work function contrary to the Schottky-Mott model [4-6]. Therefore, it is necessary to include the contribution of above mentioned factors for a better understanding of real Schottky junctions, discussed in the following subsections.

2.2.1 Image force lowering (Schottky effect)

Image force induced lowering of the SBH is called the Schottky effect [11]. An electron at a distance x away from metal will induce a positive charge inside the metal at distance of $-x$. This positive charge is referred to as the image charge and the attractive force associated between these charges is called an image force. Such force can be written as

$$\boldsymbol{F = \frac{-q^2}{4\pi\epsilon_S(2x)^2} = -qE} \qquad [2.15]$$

The formation of image charge and electric field lines at M-S junction is shown in Fig. 2.4 (a). The potential can then by obtained as

$$\boldsymbol{-V(x) = +\int_x^\infty E dx' = +\int_x^\infty \frac{q}{4\pi\epsilon_S.4\,(x')^2}\,dx' = \frac{-q}{16\pi\epsilon_S x}} \qquad [2.16]$$

Where x' is the integration variable. The plot of the potential energy (PE) of the electron, $-qV(x)$ is shown in Fig.2.4 (b) under the assumption of an absence of any other electric field. However, when an external electric field is applied, the potential energy is modified and can be written as

$$\boldsymbol{PE(x) = \frac{q^2}{16\pi\epsilon_S x} + qEx} \quad [2.17]$$

The potential energy of the electron, including the effect of an external electric field, is also shown in Fig. 2.4 (b). The peak potential barrier is now lowered by $\Delta\phi$ and the location of the lowering x_m can be given by the condition

$$\boldsymbol{\frac{d(PE(x))}{dx} = 0} \quad [2.18]$$

that gives

$$\boldsymbol{x_m = \sqrt{\frac{q}{16\pi\epsilon_S E}}} \quad [2.19]$$

and

$$\boldsymbol{\Delta\phi = \sqrt{\frac{qE}{4\pi\epsilon_S}}} \quad [2.20]$$

Thus, the effective SBH can by expressed as

$$\boldsymbol{(\phi_B)_{eff} = \phi_B - \Delta\phi} \quad [2.21]$$

In the above equation, ϕ_B is representing the zero bias SBH. However, in the previous sections ϕ_B was the general representation of the SBH, therefore let us relabel this zero bias SBH as ϕ_{B0}. Note that in forward bias, the effective barrier height is slightly larger than ϕ_{B0}. On the other hand, under reverse bias, the effective barrier height is slightly smaller than ϕ_{B0}. Image force lowering constitutes a very small portion, 1-50 meV, of the total Schottky barrier height which also depends on the dielectric constant and the doping concentration of semiconductor [4].

2.2.2 The tunneling effect

The tunneling effect is a dominant transport process in highly doped semiconductors where the width of depletion layer decreases with increasing dopant concentration [7]. Since the barrier is triangular and smaller at the top, the charge carriers might have sufficient energy to tunnel through this barrier. This process is called thermionic field emission (TFE). However, tunneling can also occur for carriers near the Fermi level in degenerate semiconductors which is known as field emission (FE). Although, the current conduction mechanism is different for TFE and FE but both result in an effective decrease in the SBH [8, 9]. Schematic representation of TFE and FE is shown in Fig.2.5. For a TFE process, the current can be given as [9]

$$\boldsymbol{I = I_S exp\left(\frac{qV}{E_0}\right)} \qquad [2.22]$$

with

$$\boldsymbol{E_0 = E_{00}\, coth\left(\frac{E_{00}}{kT}\right)} \qquad [2.23]$$

and

$$\boldsymbol{E_{00} = \frac{\hbar}{2}\sqrt{\frac{N_D}{m^* \epsilon_S}}} \qquad [2.24]$$

where E_{00} is characteristic tunneling energy. The effective tunneling barrier lowering due to TFE can be given by [9]

$$\boldsymbol{\Delta\phi_{tunn} = (1.5E_{00})^{2/3} V^{1/3}} \qquad [2.25]$$

2.2.3 Bardeen's model

It is experimentally observed that the previously discussed Schottky-Mott model does not work for most metal-semiconductor contacts [4, 10]. Deviation from the Schottky-Mott model was explained by Bardeen [8] who proposed that if sufficient number of surface states existed at the M-S interface, the SBH would be independent of the metal work function. The surface states,

known as Shockley-Tamm states, are electronic states localized at the surface of the semiconductor crystal and are due to the termination of the crystal lattice [11, 12]. Fig.2.6 shows the energy band diagram of M-S junction considering the case when surface states are distributed within the bandgap and inside the conduction and valence bands. Here, Φ_0 is the charge neutrality level relative to the valence band. When the Fermi level E_F coincides with Φ_0, the surface states below E_F are filled and the ones above are empty so that the net charge of all surface states is zero, i.e. the surface is neutral. However, if E_F is below (above) Φ_0, the net surface charge (Q_{SS}) is positive (negative) and Q_{SS} can be given by [4]

$$\boldsymbol{Q_{SS} = -qD_S\left(E_g - q\Phi_0 - q\phi_{B0} - q\Delta\phi\right)} \quad [2.26]$$

where D_S is density of surface states per unit area per unit energy and $\Delta\phi$ is the Schottky barrier lowering. The remaining term in parenthesis, is the energy difference between the Fermi level at the surface and the zero bias SBH. Now, if D_S is very large, a minor displacement in the Fermi level from the neutrality level causes a large change in Q_{SS}. Furthermore, for the case when E_F drops slightly below the Φ_0, this excess Q_{SS} counterbalance the charge transferred from metal and locks the Fermi level to the charge neutrality level. A similar mechanism occurs when E_F moves above Φ_0. The locking of Fermi level to the charge neutrality level is referred to as Fermi level pinning which makes the SBH almost independent of the metal work function. Using the Bardeen model, the SBH can be given as

$$\boldsymbol{q\phi_{B0} = E_g - q\Phi_0} \quad [2.27]$$

where $\Phi_0 = E_F - E_V$. On the other hand, when D_S is zero, Equation [2.26] turns into the Schottky-Mott case for an ideal Schottky junction.

2.3 Carrier transport processes

Although the electrostatic of a M-S junction is very similar to a p-n junction, the carrier transport mechanism is totally different [4]. In M-S junctions, the dominant current component comes from the majority carriers which is in contrast to a p-n junction where both the majority and the minority carriers participate in current conduction. Four main types of transport mechanisms of M-S junctions in the forward bias region (inverse processes occur under reverse bias) have already shown in Fig.2.5. These four mechanisms are (a) thermionic emission (TE), (b) quantum mechanical tunneling of charge carriers through the potential barrier, (c) electron-hole recombination in the depletion region, similar to p-n junctions, and (d) hole injection from the metal to the semiconductor. The detailed discussion about dominant transport mechanisms in forward and reverse bias regimes is given in the next two subsections.

2.3.1 Forward bias transport mechanism

2.3.1.1 Thermionic emission theory

Usually emission of electrons from a hot metal surface into free space is called thermionic emission and the equation that relates emitted current to the temperature and work function of metal is called the Richardson equation [13, 14]

$$\boldsymbol{I = AA^{*}T^{2}exp\left(-\frac{\Phi_M}{kT}\right)} \qquad [2.28]$$

where I is the emission current and $A^{*}$is the Richardson constant. A similar thermionic equation can be easily obtained for a M-S junction under the assumptions of (a) much higher Schottky barrier height than kT, (b) a well-established thermal equilibrium at the emission plane, and (c) no effect on thermal equilibrium due to net current flow. Furthermore, it also illustrates two current density components, one for the metal to semiconductor $J_{M\rightarrow S}$, and the other for the semiconductor

to metal $J_{S\to M}$. Here, the current density $J_{S\to M}$ is a function of the concentration of electrons which have sufficient energies to overcome the barrier and move in the x-direction. The current density from the semiconductor to the metal can thus represented as [4]

$$\boldsymbol{J_{S\to M} = \int_{E_F+q\phi_b}^{\infty} q v_x dn} \qquad [2.29]$$

where $E_F + q\phi_b$ is the minimum energy required for thermionic emission into the metal, and v_x is the carrier velocity in the direction of transport. The incremental electron concentration is given by [4]

$$\boldsymbol{dn = g_c(E) f_F(E) dE} \qquad [2.30]$$

where dn is the number of electrons in the energy range of E to $E + dE$, $g_c(E)$ is the density of states in the conduction band, and $f_F(E)$ is the Fermi-Dirac distribution function. Under the assumption of the Maxwell-Boltzmann approximation,

$$\boldsymbol{dn = \frac{4\pi(2m_n^*)^{3/2}}{h^3}\sqrt{E - E_C}\, exp\left[\frac{-(E-E_F)}{kT}\right] dE} \qquad [2.31]$$

If all of the electron energies above E_C is assumed to be only kinetic then

$$\boldsymbol{\sqrt{E - E_C} = v\sqrt{m^*/2}} \qquad [2.32]$$

substitution of Equation [2.32] in to Equation [2.31] gives

$$\boldsymbol{dn = 2\left(\frac{m^*}{h}\right)^3 exp\left(\frac{-qV_n}{kT}\right) exp\left(\frac{-m^*v^2}{2kT}\right)(4\pi v^2 dv)} \qquad [2.33]$$

The above equation gives the distribution of electron density (number of electrons/unit volume) that have speeds between v and $v + dv$ in all directions. If the speed is resolved into its components along the axes with the x-axis parallel to the transport direction, we have

$$\boldsymbol{v^2 = v_x^2 + v_y^2 + v_z^2} \qquad [2.34]$$

With the transformation $4\pi v^2 dv = dv_x dv_y dv_z$, one can obtain

$J_{S\to M}$

$$= 2e\left(\frac{m^*}{h}\right)^3 exp\left(-\frac{qV_n}{kT}\right)\int_{v_{ox}}^{\infty} v_x\, exp\left(-\frac{m^*v_x^2}{2kT}\right)dv_x \int_{-\infty}^{\infty} exp\left(-\frac{m^*v_y^2}{2kT}\right)dv_y \int_{-\infty}^{\infty} exp\left(-\frac{m^*v_z^2}{2kT}\right)dv_z$$

$$= \left(\frac{\boldsymbol{4\pi q m^* k^2}}{\boldsymbol{h^3}}\right)\boldsymbol{T^2 exp}\left(-\frac{\boldsymbol{qV_n}}{\boldsymbol{kT}}\right)\boldsymbol{exp}\left(-\frac{\boldsymbol{m^* v_{0x}^2}}{\boldsymbol{2kT}}\right) \quad [2.35]$$

The velocity v_{0x} is the minimum velocity required in the x direction to surmount the barrier and is given by

$$\boldsymbol{\frac{1}{2}m^* v_{0x}^2 = q(V_{bi} - V)} \quad [2.36]$$

where V_{bi} is the built in potential at zero bias. Substituting Equation [2.36] into Equation [2.35] to get

$$J_{S\to M} = \left(\frac{4\pi q m^* k^2}{h^3}\right)T^2 exp\left(-\frac{q(V_{bi}+V_n)}{kT}\right)exp\left(\frac{qV}{kT}\right)$$

$$= \boldsymbol{A^* T^2 exp}\left(-\frac{\boldsymbol{q\phi_{B0}}}{\boldsymbol{kT}}\right)\boldsymbol{exp}\left(\frac{\boldsymbol{qV}}{\boldsymbol{kT}}\right) \quad [2.37]$$

Where ϕ_{B0} is the barrier height and is equal to $[V_n(\sim E_C - E_F) + V_{bi}]$ where

$$\boldsymbol{A^* = \frac{4\pi q m^* k^2}{h^3}} \quad [2.38]$$

$A^*$is the effective Richardson constant of the semiconductor. Since the barrier height for the electrons moving from the metal into the semiconductor remains the same, the current flowing into the semiconductor is thus unaffected by the applied voltage. It must therefore be equal to the current flowing from the semiconductor into the metal when thermal equilibrium is established (i.e. when $V = 0$). The corresponding current density is obtained from Equation [2.37] by setting $V = 0$,

$$\boldsymbol{J_{M\to S} = -A^* T^2 exp}\left(-\frac{\boldsymbol{q\phi_{B0}}}{\boldsymbol{kT}}\right) \quad [2.39]$$

The total current density is given by the sum of Equation [2.37] and [2.39]

$$\boldsymbol{J = \left[A^{*}T^{2} exp\left(-\frac{q\phi_{B0}}{kT}\right)\right]\left[exp\left(\frac{qV}{kT}\right) - 1\right]} \quad [2.40]$$

$$\boldsymbol{= J_S\left[exp\left(\frac{qV}{kT}\right) - 1\right]} \quad [2.41]$$

where J_S is reverse saturation current. Equation [2.41] is the well-known Schottky junction equation that shows an exponential dependence of the current density on applied bias voltage and temperature [4]. The characteristic parameters (barrier height and ideality factor) of a Schottky junction can be obtained from the above equation which is discussed in the next sections.

2.3.1.2 Diffusion theory

The diffusion theory works for lightly doped semiconductors which have a depletion width larger than the carrier diffusion length [15]. In this theory, both (drift and diffusion) components are considered to contribute for total current density in the depletion region. The current in the depletion width is a function of the local electric field (E) and concentration gradient which can be given by [4,15]

$$\boldsymbol{J = qn(x)\mu_n E_x + qD_n \frac{dn(x)}{dx}} \quad [2.42]$$

where, $\mu_n = (q/kT)D_n$ and $E_x = -\,dV(x)/dx$. Under steady state conditions, current density in depletion region is constant and independent of x, therefore, the above equation can be integrated over the entire depletion region after multiplying by $exp(-qV(x)/kT)$ as an integrating factor. The integration gives

$$\boldsymbol{J\int_0^W exp(-qV(x)/kT)\,dx = qD_n n(x) exp(-qV(x)/kT)|_0^W} \quad [2.43]$$

boundary conditions at $x = 0$ and $x = W$ are

$$\boldsymbol{qV(0) = -q\phi_{B0}} \text{ and } \boldsymbol{qV(W) = -q(V_{bi} + V_a)} \quad [2.44]$$

where V_a is the applied voltage. Similarly electron densities at $x = 0$ and $x = W$ are given by

$$\boldsymbol{n(0) = N_C exp\left(-\frac{q\phi_{B0}}{kT}\right)\ and\ n(W) = N_C exp\left(-\frac{qV_n}{kT}\right)} \quad [2.45]$$

Substituting Equation [2.44] and [2.45] in to Equation [2.43] and we get

$$\boldsymbol{J = \left(\frac{q^2 D_n N_C}{kT}\right)\sqrt{\frac{2q(V_{bi}+V_a)N_D}{\epsilon_S}}\, exp\left(-\frac{q\phi_{B0}}{kT}\right)\left[exp\left(\frac{qV_a}{kT}\right) - 1\right]} \quad [2.46]$$

or

$$\boldsymbol{J = J_S\left[exp\left(\frac{qV_a}{kT}\right) - 1\right]} \quad [2.47]$$

where J_S is the saturation current density obtained from the diffusion model. Both TE and diffusion models have similar exponential dependence of $J_S (or\ I_S)$ on the barrier height and temperature. Furthermore, it is also noted that the saturation current derived from the diffusion model shows a stronger dependence on the applied bias rather than that from the TE model where it is more sensitive to temperature [4].

There is one more possibility of conduction, the tunneling mechanism where charge carriers pass (tunnel) through the Schottky barrier instead of overcoming it. The tunneling mechanism is dominating in degenerate semiconductors where the thin depletion layer allows charge carriers to tunnel easily. The magnitude of the tunneling current is an exponential function of the barrier height and the doping density, which can be given by [9]

$$\boldsymbol{J_T \sim exp(-q\phi_{B0}/E_{00})} \quad [2.48]$$

where $E_{00} = (q\hbar/2)\sqrt{N_D/m^*\epsilon_S}$. This equation indicates that the tunneling current will increase exponentially with the square root of dopant density and decreases exponentially with increasing barrier height.

2.3.2 Reverse bias transport mechanism

According to standard TE emission theory, the reverse leakage current (I_r) of a Schottky junction is constant with an applied bias $V > 3kT/q$. However, significant enhancement in I_r is reported

at large electric fields (i.e. applied bias voltage V_R) that further lead to a bias dependent barrier height i.e. the SBH decreases with increasing V_R for a moderately doped semiconductor (doping concentration~10^{15}-10^{16} cm^{-2}). This bias dependent barrier height has been attributed to the electron tunneling directly through the M-S interface [4, 15]. There are several tunneling mechanisms to explain this behavior where the two most common, Poole-Frenkel and Schottky emission, are discussed in the following subsections.

2.3.2.1 Schottky emission/ field enhanced thermionic emission

Detailed discussion about the Schottky effect is already given in section (2.2.1). This mechanism is based on Schottky barrier lowering which occurs due to strong electric fields [15, 16]. Under reverse bias operation (negative voltage on metal), electrons escaping from the metal surface create positive image charges inside the metal. The positive image charges create a coulombic attractive force that pulls the escaping electrons back into the metal and reduces the effective barrier height as given in Equation [2.20]

$$\Delta\boldsymbol{\phi} = \sqrt{\frac{\boldsymbol{qE_{max}}}{\boldsymbol{4\pi\epsilon_S}}} \qquad [2.49]$$

It is clear from the above equation that the barrier reduction depends on the applied voltage which further leads to a field dependence for the reverse bias current. The effect of the electric field on the reverse bias current can be obtained by replacing ϕ_{B0} by $\phi_{B0} - \Delta\phi$ in Equation [2.41]

$$\boldsymbol{I = AA^{*}T^{2}exp\left[-\frac{q(\phi_{B0}-\sqrt{qE_{max}/4\pi\epsilon_S}}{kT}\right]} \qquad [2.50]$$

If reverse bias conduction mechanism is dominated by Schottky emission, then the plot of $\ln(I_S/T^2)$ versus $E^{1/2}$ should be linear where barrier height can be obtained from the intercept at $E = 0$.

2.3.2.2 Poole-Frenkel emission

The mechanism of Poole-Frenkel emission (P-F) is similar to the Schottky emission where the thermal excitation of electrons occurs in presence of strong electric fields which lowers the energy barrier. However, in case of the Schottky effect, the lowering of the energy barrier is due to the interaction between image forces and the applied electric field. On the other hand, for P-F conduction, the coulombic interaction is associated with an ionized trap and the applied field [16, 17]. The schematic representation of the P-F conduction mechanism is shown in Fig.2.7. Here, the black line shows the evenly spread potential wells (due to trap states) in absence of any applied electric field. The application of electric field tilts the potential well background from its equilibrium position (black to red line) which reduces the barrier to allow the escape of charge carriers from one trap state to the next trap state of a lower potential. The potential energy of a trapped electron is given as follows

$$\boldsymbol{\phi(x) = -\frac{q^2}{4\pi\epsilon_S x}} \qquad [2.51]$$

where x is the distance from the trap center. The potential energy in P-F emission is four times higher than that of Schottky emission, therefore P-F barrier lowering would have twice the effect compared with to the Schottky effect. The current due to P-F emission is given by [17]

$$\boldsymbol{I_S = \sigma_0 E\, exp\left[\frac{-q\left(\phi_T - \sqrt{qE/\pi\epsilon_S}\right)}{kT}\right]} \qquad [2.52]$$

where $\sigma_0 = N_C q\mu$ stands for low field conductivity with N_C being the density of states of the conduction band charge carriers and μ is the electronic mobility and $q\phi_T$ is the trap energy level. For P-F emission, the plot of $\ln(I/E)$ versus $E^{1/2}$ would be linear where the trap barrier height can be extracted from the intercept at E=0. The slope provides the dielectric constant of the semiconducting material. Furthermore, it is clear from Equation [2.50] and [2.52] that the slope

(emission coefficient) of P-F emission is twice that of Schottky emission. Therefore, a general relationship can be given as [18]

$$\boldsymbol{S = \frac{q}{nkT}\sqrt{\frac{q}{\pi\epsilon_S}}} \quad [2.53]$$

with n=1 for P-F and n=2 for Schottky emission.

2.4 Measurement of the Schottky barrier height

There are various measurements techniques that have been used to estimate the barrier height of various M-S Schottky junctions. The most commonly used methods are current-voltage (I-V), current-temperature (activation energy), photoelectric, and capacitance-voltage (C-V) measurements. The brief introduction of these methods is given in the following sections.

2.4.1 Current-Voltage (I-V) measurement

In M-S junctions, the total current is expected to increase in the forward bias direction as derived and discussed in section (2.3.1.1), where the total current passing through a M-S interface is given by

$$\boldsymbol{I(V,T) = I_S(T)exp\left(\frac{qV}{\eta kT}\right)} \quad [2.54]$$

where I_S the reverse saturation current, expressed as $I_S = AA^*T^2 \exp(-q\phi_{B0}/\eta kT)$ which can be determined by the y-intercept for the linear region of $\ln(I)$ versus V plot. Once the value of I_S is known, the Schottky barrier height can be determined as follows [4]

$$\boldsymbol{\phi_{B0} = \frac{\eta kT}{q} ln\left(\frac{AA^*T^2}{I_S}\right)} \quad [2.55]$$

The parameter η is called the ideality factor and is written as an inverse slope of $\ln(I)$ versus V,

$$\boldsymbol{\eta = \frac{q}{kT}\frac{dV}{d(ln\, I)}} \quad [2.56]$$

Here, η is a measure of the deviation from the ideal thermionic emission process that has $\eta = 1$ for an ideal case. However, the experimental value of η is found to be greater than 1, which can be attributed to additional current processes that are discussed in section 2.5.

Although, I-V measurement provides a practical and standard method to measure the effective barrier height at the M-S interface after reaching thermal equilibrium, but it does not give the true Schottky barrier height due to not knowing the electrically active M-S contact area.

2.4.2 Current-Temperature (I-V-T)/activation energy measurement

The basic assumption of this method is that the value of the Schottky barrier height does not depend on temperature. This method requires the measurement of I_S from I-V characteristics at different temperatures. The expression of I_S can be rewritten as [4]

$$\boldsymbol{ln}\left(\frac{\boldsymbol{I_S}}{\boldsymbol{T^2}}\right) = \boldsymbol{ln}(\boldsymbol{AA^*}) - \frac{\boldsymbol{q\phi_{B0}}}{\boldsymbol{kT}} \qquad [2.57]$$

In the above equation, the contact area term is only in the first term of the right hand side. Therefore, ϕ_{B0} can be deduced from the slope of the Richardson plot, $\ln(I_S/T^2)$ versus$1/T$. The main advantage of an activation energy measurement method is that the estimation of the electrically active area can be avoided. However, the expected linear plot of the activation energy becomes non-linear due to a lateral inhomogeneous junction which leads to inaccurate ϕ_{B0}.

2.4.3 Capacitance-Voltage (C-V) measurement

The barrier height of a Schottky junction can also be determined by capacitance-voltage (C-V) measurements. In these measurements, a small ac signal is superimposed upon a dc voltage (V_R) that forms a capacitance between the metal and the semiconductor surface. The magnitude of the capacitance at M-S interface strongly depends on the built-in potential(V_{bi}), dielectric constant, and the doping level of the semiconductor. A typical relationship between C and V is given by [4]

$$\frac{1}{C^2} = \frac{2(V_{bi}+V_R)}{q\epsilon_S N_D} \quad [2.58]$$

when $1/C^2$ is plotted as a function of V_R a linear dependence should be observed. The value of V_{bi} can be obtained from the y-intercept at $V_R = 0$ while N_D can be obtained from the slope $(2/q\epsilon_S N_D)$. After knowing the value of V_{bi}, ϕ_{B0} can be determined as follows

$$\phi_{B0} = V_{bi} + \frac{E_C - E_F}{q} = V_{bi} + \frac{kT}{q} ln\left(\frac{N_C}{N_D}\right) \quad [2.59]$$

Theoretically, I-V and C-V measurements must yield the same ϕ_{B0} value for a homogeneous M-S interface. However, for an inhomogeneous interface, the barrier height value obtained from the C-V method is found to be larger than ϕ_{B0} obtained using I-V measurements [4]. In an I-V measurement, the electrons usually pick the least resistive paths dominated by small effective SBHs, while a C-V measurement probes an average value of the SBH [19]. The difference in the barrier height values obtained by these two measurement methods is explained in next section.

2.5 Barrier height inhomogeneity

One reliable way to obtain key parameters, η and ϕ_{B0}, of a M-S Schottky junction is to apply thermionic emission theory on a set of temperature dependent I-V measurements. However, the reported temperature dependence of η and ϕ_{B0} with $\eta > 1$ gives a clear indication of a deviation from ideal TE theory. The value of η larger than 1 is attributed to various factors such as presence of interface/trap states in the native oxide layer on the M-S interface, barrier lowering due to image forces, and contributions from generation/recombination currents [19]. The above mentioned factors and ideal TE theory are all based on assumption of a spatially homogeneous, atomically flat M-S interface that has only one barrier height present. But in reality, the barrier height may not be the same over the entire area of contact due to the variation in the metal film thickness, atomic steps, dislocations, and grain boundaries which have been confirmed via electrical and

optical characterization methods [20,21]. Furthermore, the effect of barrier height inhomogeneities on I-V-T characteristics and junction parameters has also been reported [20,21]. In earlier approaches, the barrier height inhomogeneity was investigated by considering the Schottky junction made of non-interacting parallel patches of different barrier heights. This patch model had little success and only agreed well when the depletion width is smaller than the spatial variation of the barrier height [22, 23]. However, the non-interacting models failed to explain the reason of ideality factor larger than one as well as the temperature dependence of barrier height [19]. Therefore, the interaction between different barrier height patches needed to be considered and this was done using the following two models.

2.5.1 Gaussian distribution of barrier heights

Werner and Guttler proposed an analytic model to describe I-V-T characteristics and the temperature dependence of the barrier height (and ideality factor) of a Schottky junction [19]. In their model, a continuous barrier distribution at the M-S interface on the length scale that is small compared to the width of the depletion region is considered. A Gaussian distribution of the barrier heights is assumed

$$\boldsymbol{\phi_{B0} = \phi_{bm}(T = 0) - \frac{q\sigma_S^2}{2kT}} \qquad [2.60]$$

characterized by a zero bias standard deviation σ_S and zero bias mean barrier height ϕ_{bm}. The plot of ϕ_{B0} versus $q/2kT$ yields a graph with linear portions each of which corresponds to a patch with different Gaussian distribution characteristics. Furthermore, the variation of η with temperature, according to this model, is given as

$$\boldsymbol{\left(\frac{1}{\eta_{ap}} - 1\right) = \rho_2 - \frac{q\rho_3}{2kT}} \qquad [2.61]$$

where the coefficients ρ_2 and ρ_3 represents the voltage deformation of ϕ_{bm} and $\sigma_{S,}$ respectively. In addition, the Gaussian distribution of barrier heights takes care of the non-linearity of the Richardson plot which gives a modified Richardson equation and is as follows [19]

$$\boldsymbol{ln\left(\frac{I_S}{T^2}\right) - \left(\frac{q^2\sigma_S^2}{2k^2T^2}\right) = ln(AA^*) - \frac{q\phi_{bm}}{kT}} \quad [2.62]$$

The modified Richardson plot according to Equation [2.62] must be a straight line whose slope directly gives the mean barrier height ϕ_{B0} and the intercept yields the value of A^*.

2.5.2 Flat band barrier height

In the previous section, the temperature dependence of the barrier height and the ideality factor is attributed to spatial barrier fluctuations at the M-S interfaces. The influence of inhomogeneities can be eliminated by considering the flat band barrier height. The flat band barrier height ϕ_{bf} is a more fundamental quantity than the ϕ_{B0} since it is measured at zero electric field i.e. when the semiconductor bands are flat. It is worth noting that ϕ_{bf} is independent of the current transport mechanism. Therefore, it can also be used for the case where tunneling current dominates the transport mechanism. ϕ_{bf} can be expressed in terms of ϕ_{B0} and η as given below [24]

$$\boldsymbol{\phi_{bf} = \eta\phi_{B0} - \xi(\eta - 1)} \quad [2.63]$$

where $\xi = (kT/q)\ln(N_C/N_d)$ is the energy difference between the Fermi level and the bottom of the conduction band. Other symbols are as follows $N_C = 2M_C(2\pi m^* kT/h^2)^{3/2}$, is the effective density of states in the conduction band, N_d is the donor concentration, and M_C is conduction band minima for the semiconductor [24]. The non-linear trend observed in the Richardson plot can also be eliminated by substituting ϕ_{bf} for ϕ_{B0} in Equation [2.41]

$$\boldsymbol{I_{f0} = AA^*T^2 exp\left(-\frac{q\phi_{bf}}{\eta kT}\right)} \quad [2.64]$$

where I_{f0} is flat band saturation current density, which can be expressed as

$$\boldsymbol{I_{f0} = I_0\, exp\left[\left(\frac{\eta-1}{\eta}\right) ln\left(\frac{N_C}{N_d}\right)\right]} \quad [2.65]$$

The above Equation [2.65] can be used to obtain a modified Richardson plot of $\ln\left(I_{f0}/T^2\right)$ versus $1000/\eta T$. In addition, Equation [2.63] shows a linear dependence between ϕ_{B0} and η which gives a way to calculate the barrier height of a homogeneous M-S interface just by putting $\eta = 1$ in Equation [2.63] and by this means it accounts for the effect of the barrier height inhomogeneity [25].

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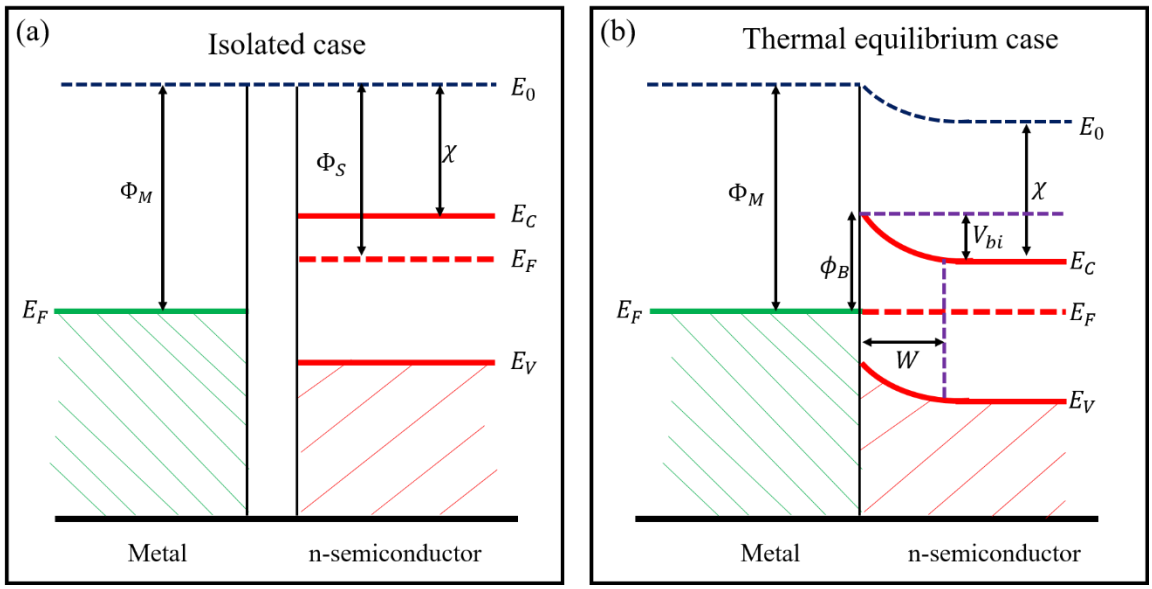

Figure 2.1: (a) Energy-band diagram of a M-S (n-type) junction before contact and (b) ideal energy-hand diagram of a metal-n-semiconductor junction in equilibrium condition.

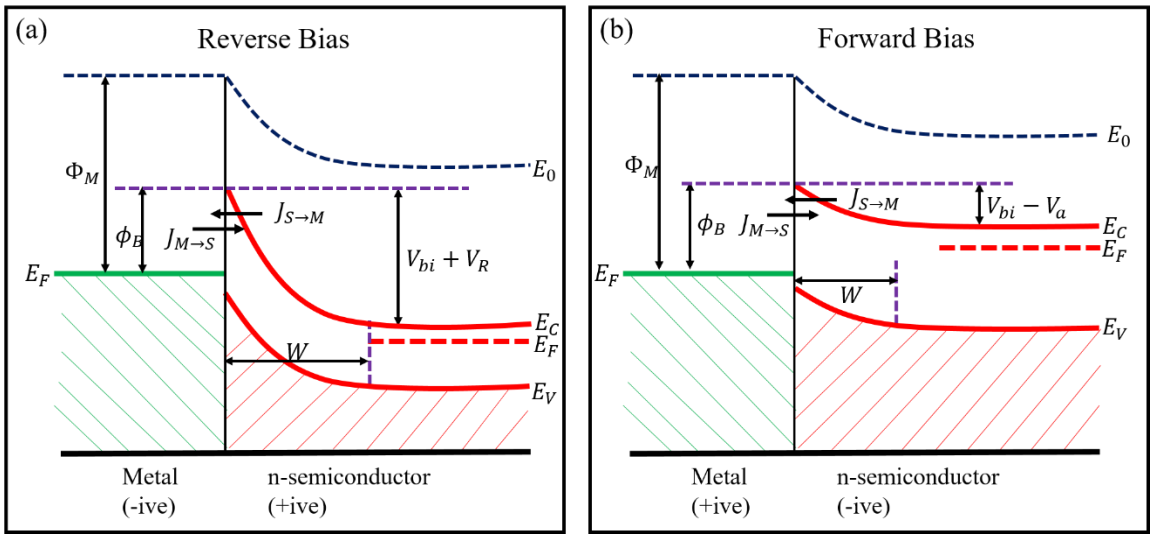

Figure 2.2: Energy-band diagram of a M-S (n-type) junction under (a) reverse bias, and (b) forward bias conditions.

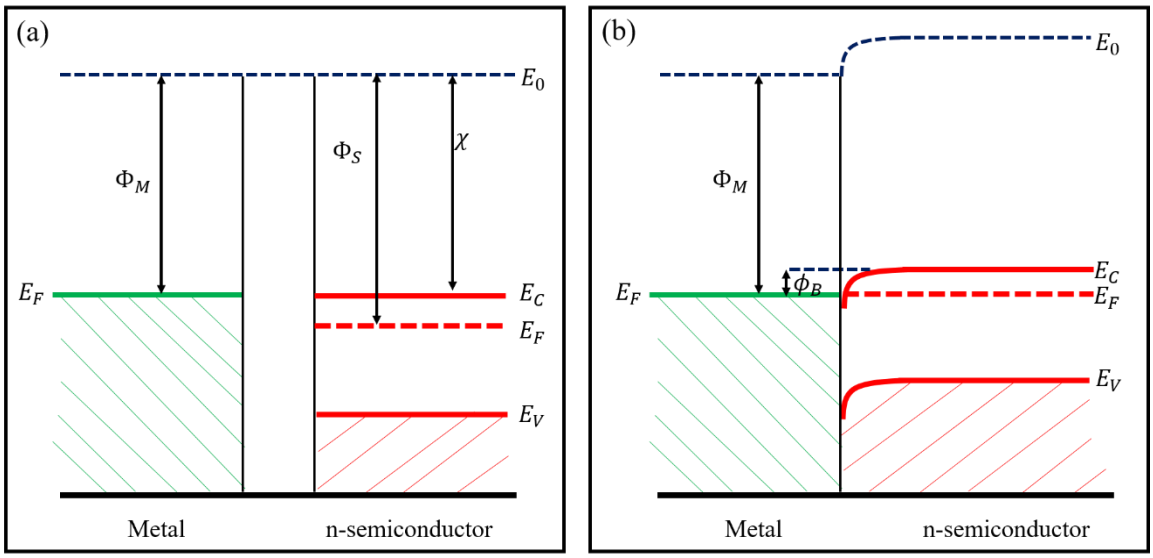

Figure 2.3: (a) Energy-band diagram of a M-S (n-type) semiconductor junction before contact, and (b) energy band diagram of M-S (n-type) Ohmic contact with $\Phi_M < \Phi_S$.

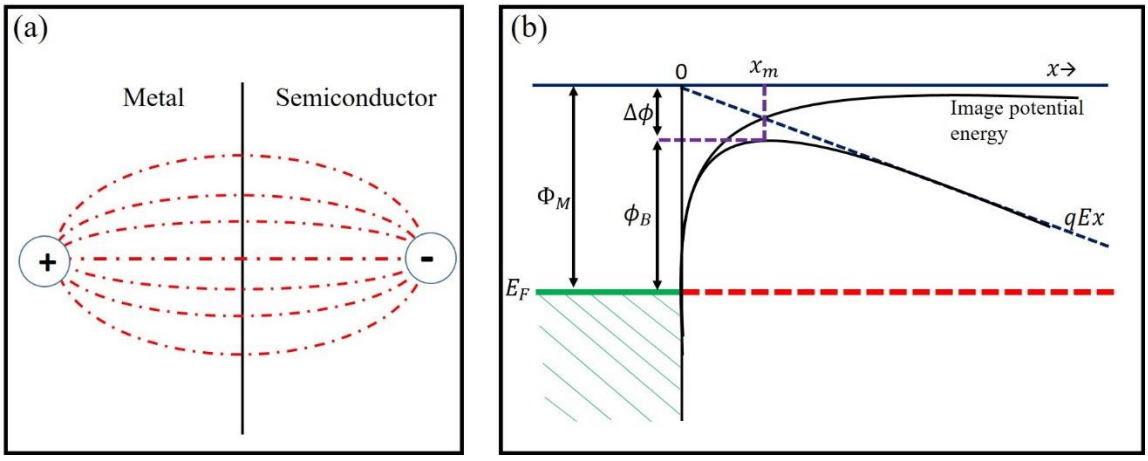

Figure 2.4: (a) Formation of image charge and electric field lines at M-S junction interface, and (b) Schottky barrier height lowering due to image force in presence of applied electric field.

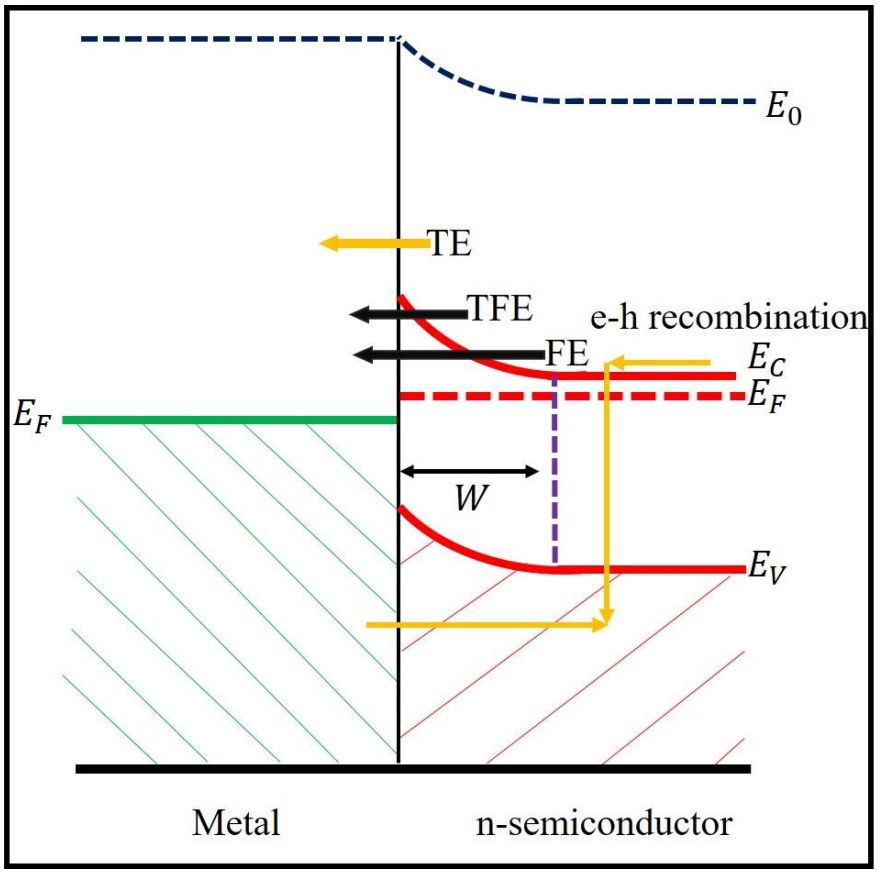

Figure 2.5: Charge transport mechanism at M-S interface under forward bias condition.

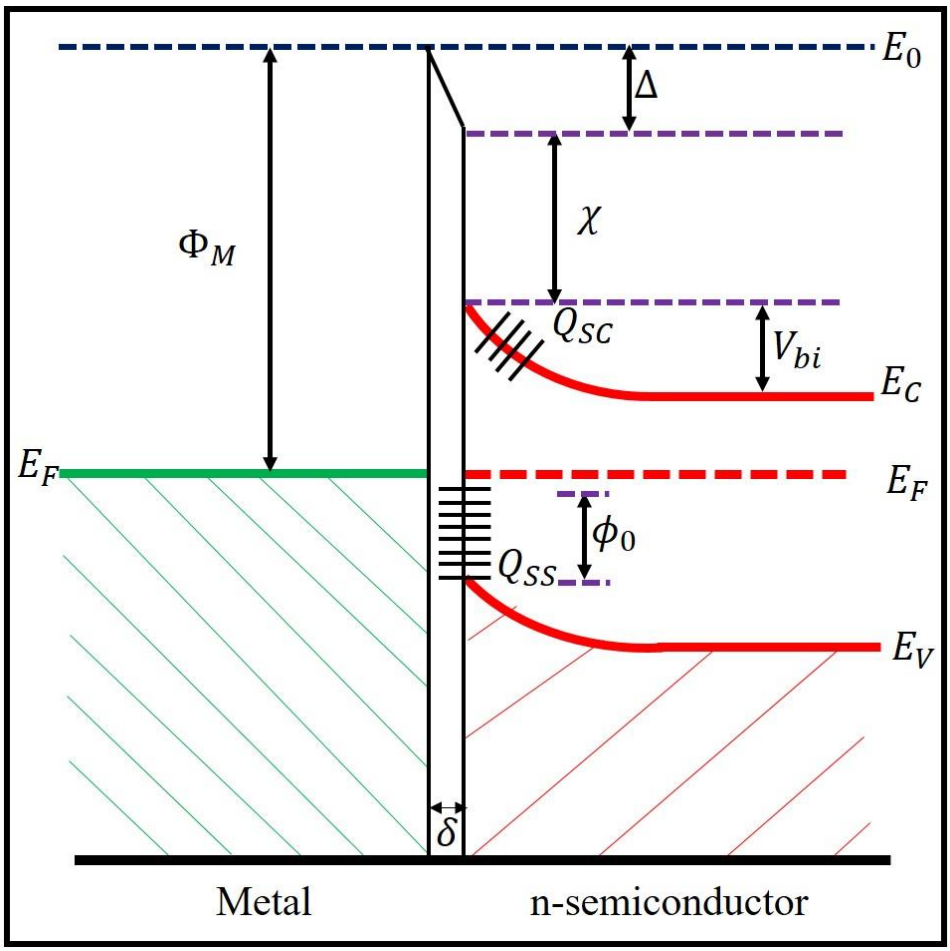

Figure 2.6: Energy-band diagram of a M-S junction with an interfacial layer and surface states.

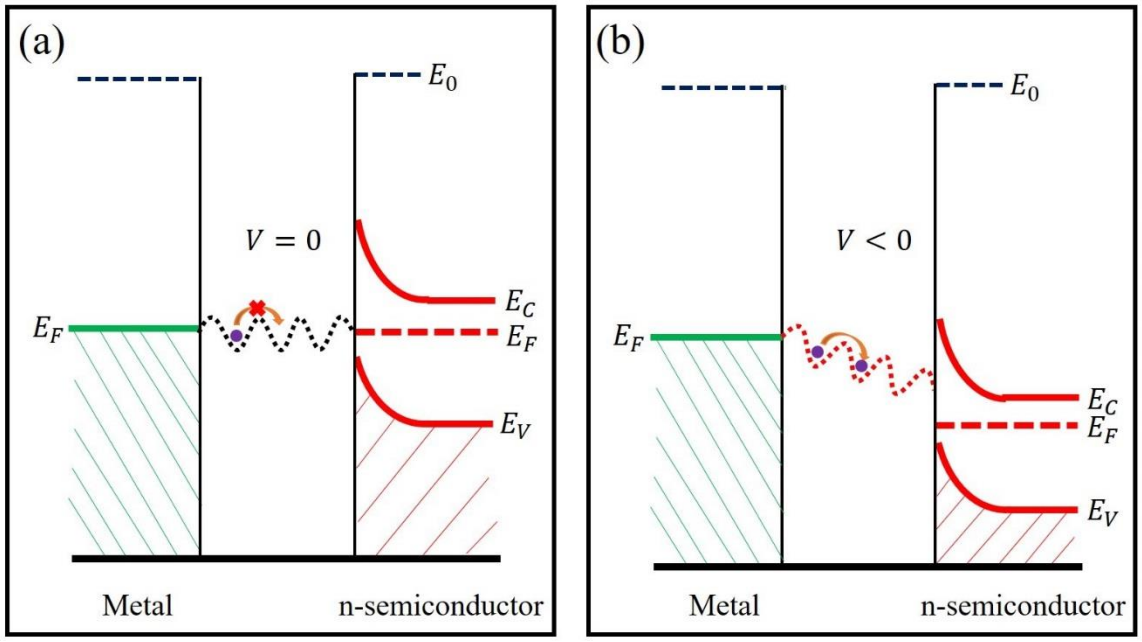

Figure 2.7: Poole- Frenkel transport mechanism at M-S interface (a) in absence of applied electric field, and (b) in presence of applied electric field.

Chapter 3
Introduction of Graphene

Drs. Novoselov and Geim won the Nobel-prize in 2010 for their ground breaking discovery of graphene [1]. Since then graphene has been the subject of intensive research because of its unique electronic, optical, thermal and mechanical properties. In this chapter, a brief introduction of basic electronic properties and semi-metallic band structure of graphene is given in section 3.1. The details of graphene growth with a brief overview of transferring graphene from the growth substrate to an arbitrary substrate is also discussed in section 3.2.

3.1 Graphene band structure

Many unique properties of graphene, a monolayer of sp^2 bonded carbon atoms, are directly linked to its 2D crystalline nature and the resulting band structure [1-3]. In the ground state, each carbon atom has six electrons which occupy the atomic orbitals $1s^2$, $2s^2$ and $2p^2$. In the $1s^2$ orbital, the two electrons are strongly bonded to the nucleus, however the 2s, $2p_x$, $2p_y$ and $2p_z$ orbitals share four loosely bonded electrons (one in each) which can mix up their wave- functions in a process called hybridization. The states after hybridization are shown in Fig.3.1 (a). Here the three σ states are evenly spaced in the x-y plane at an angle of 120° with respect to each other to form covalent bonds with their neighbors and give rise to the hexagonal lattice structure of graphene. The remaining unpaired $2p_z$ orbitals, the π state, is aligned to the z-direction. Electrons in π state are weakly bonded and can hop easily between neighboring atoms. When one carbon atom interacts with its neighbor carbon atom, overlapping of their sp^2 orbitals gives three σ bonding and three σ* antibonding covalent bands that are extremely rigid and provide strength for graphene. While the hybridization of remaining $2p_z$ orbitals gives π bonding and π* antibonding bands [shown in

Fig.3.1 (b)] that contribute to the electrical conductivity [4]. This discussion is important to determine the energy dispersion relation for graphene.

The honeycomb lattice of graphene can be seen as a triangular lattice with a basis of two atoms per unit cell. The unit cell of graphene is shown in Fig.3.2 (a) where the two interpenetrating triangular lattices are shown by A and B type atoms. Here, each carbon atom at site A has three nearest neighboring atoms at site B and vice versa, separated by a C-C bond of length 1.42 Å. The real space lattice vectors ($\overrightarrow{a_1}$ and $\overrightarrow{a_2}$) can be written in Cartesian coordinates as

$$\overrightarrow{a_1} = \frac{a}{2}(\sqrt{3}, 1),\ \overrightarrow{a_2} = \frac{a}{2}(\sqrt{3}, -1) \qquad [3.1]$$

The reciprocal space lattice along with the Brillouin zone (BZ) is shown in Fig.3.2 (b). The reciprocal lattice vectors can be written in Cartesian coordinates as

$$\overrightarrow{b_1} = \frac{2\pi}{3a}(\sqrt{3}, 3), \qquad \overrightarrow{b_2} = \frac{2\pi}{3a}(\sqrt{3}, -3) \qquad [3.2]$$

Here, $\overrightarrow{a_i}.\ \overrightarrow{b_j} = 2\pi\delta_{ij}$, is the standard definition of the reciprocal space. The first BZ represents four types of high symmetry points Γ, M, K and K' corresponding to the center, edge and the corners of the BZ, respectively. Specifically, the corners of BZ (K and K') are of significant importance because the interesting physics of graphene occurs at these points which are called Dirac points.

The energy dispersion relation or band structure for graphene can be obtained by considering the interaction of carbon atoms to nearest carbon atoms i.e. the tight binding approximation (TB). As shown in Fig.3.2 (a) each carbon atom at site A has three nearest neighbors at site B

$$\eta_1 = a\left(\frac{1}{\sqrt{3}}, 0\right), \eta_2 = \frac{a}{2}\left(\frac{-1}{\sqrt{3}}, -1\right), \eta_3 = \frac{a}{2}\left(\frac{-1}{\sqrt{3}}, 1\right) \qquad [3.3]$$

In the honeycomb lattice of graphene, sublattice A and B are independent to each other, therefore, the wavefunction is generated as a linear superposition of the eigenfunction of both. As only $2p_z$

orbitals of two neighboring carbon atoms contribute to conductivity, the TB wavefunction of graphene can be written as [5]

$$\boldsymbol{\Psi_{\vec{k}}(\vec{r}) = \frac{1}{\sqrt{N}} \sum_{\vec{R}} e^{i\,\vec{k}.\vec{R}} \left[\alpha_A \phi_A(\vec{r} - \vec{R}) + \alpha_B \phi_B(\vec{r} - \vec{R})\right]} \quad [3.4]$$

Where $\Psi_{\vec{k}}(r)$ are the unit cell wavefunctions in the momentum basis, $\phi_{(A,B)}$ are the wave functions associated with $2p_z$ orbitals of each sub-lattice, $\alpha_{(A,B)}$ are the complex functions of the wave vectors $\vec{k}$ that represent the probability amplitude of an electron being at site A or site B. The electronic band structure of solids can be obtained by solving the Schrodinger equation,

$$\boldsymbol{H\Psi_{\vec{k}}(\vec{r}) = E_k(\vec{r})\Psi_{\vec{k}}(\vec{r})} \quad [3.5]$$

Multiplying above equation from the left by the states ϕ_A and ϕ_B followed by integration over space results into two equations as follows

$$\boldsymbol{\langle \Phi_A | H |\, \Psi_k \rangle = E\, \langle \Phi_A | \Psi_k \rangle} \quad [3.6\ (a)]$$

$$\boldsymbol{\langle \Phi_B | H |\, \Psi_k \rangle = E\, \langle \Phi_B | \Psi_k \rangle} \quad [3.6\ (b)]$$

Inserting $\Psi_{\vec{k}}(r)$ from Equation [3.4] to Equation [3.6 (a)] to get

$$\sum_{\vec{R}} e^{i\,\vec{k}.\vec{R}} \left[\alpha_A \langle \phi_A(\vec{r}) |\, H | \phi_A(\vec{r} - \vec{R}) \rangle + \alpha_B \langle \phi_B(\vec{r}) |\, H | \phi_B(\vec{r} - \vec{R}) \rangle\right]$$

$$\boldsymbol{= E \sum_{\vec{R}} e^{i\,\vec{k}.\vec{R}} \left[\alpha_A \langle \phi_A(\vec{r}) | \phi_A(\vec{r} - \vec{R}) \rangle + \alpha_B \langle \phi_B(\vec{r}) | \phi_B(\vec{r} - \vec{R}) \rangle\right]} \quad [3.7]$$

Considering only the nearest neighbors, the only matrix elements that survive in Equation [3.7] would be for on-site $\vec{R} = 0$ and nearest neighbor $\vec{R} = \eta_i (i = 1,2,3)$. The coordinates of the nearest neighbor are already given in Equation [3.3]. In addition, the direct overlapping of the $2p_z$ orbitals centered on different atoms is also neglected i.e. $\langle \phi_A(\vec{r}) | \phi_B(\vec{r} - \vec{R}) \rangle = 0$. Taking only the on-site term on the right side, Equation [3.7] turns in to

$$\boldsymbol{\alpha_A\langle\phi_A(\vec{r})|H|\phi_A(\vec{r}-\vec{R})\rangle + \alpha_B\sum_i e^{i\vec{k}.\vec{\eta_i}}\langle\phi_A(\vec{r})|\,H|\phi_B(\vec{r}-\vec{\eta_i})\rangle =}$$

$$\boldsymbol{E\alpha_A\langle\phi_A(\vec{r})|\phi_A(\vec{r})\rangle} \qquad [3.8]$$

Recall that wave function normalization is defined as $\langle\phi_{A,B}\,(\vec{r})|\,\phi_{A,B}(\vec{r})\rangle = 1$ and considering the on-site energy of π orbitals $\langle\phi_{A,B}\,(\vec{r})|H|\phi_{A,B}(\vec{r})\rangle = \epsilon_0$ with Equation [3.3] transform Equation [3.8] in to

$$\boldsymbol{\alpha_A\epsilon_0 - \alpha_B t\left[e^{-i\,k_x\,a} + e^{i\,k_x\frac{a}{2}}\left[2\,\cos\left(k_y\frac{\sqrt{3}}{2}a\right)\right]\right] = E\alpha_A} \qquad [3.9]$$

where, $t = -\langle\Phi_A(\vec{r})|H|\Phi_B(\vec{r}-\vec{\eta_l})\rangle$ is the nearest neighbor hopping term. A Similar equation can be obtained from Equation [3.5] as follows

$$\boldsymbol{\alpha_B\epsilon_0 - \alpha_A t\left[e^{i\,k_x\,a} + e^{-i\,k_x\frac{a}{2}}\left[2\,\cos\left(k_y\frac{\sqrt{3}}{2}a\right)\right]\right] = E\alpha_B} \qquad [3.10]$$

Equation [3.9] and [3.10] can be expressed in matrix form for simplicity

$$\begin{pmatrix}\boldsymbol{\epsilon_0 - E} & \boldsymbol{-tf(k)}\\ \boldsymbol{-tf^*(k)} & \boldsymbol{\epsilon_0 - E}\end{pmatrix}\begin{pmatrix}\boldsymbol{\alpha_A}\\ \boldsymbol{\alpha_B}\end{pmatrix} = \boldsymbol{0} \qquad [3.11]$$

with $f(k) = e^{i\,k_x\,a} + e^{-i\,k_x\frac{a}{2}}\left[2\,\cos\left(k_y\frac{\sqrt{3}}{2}a\right)\right]$. The solution of Equation [3.11] gives

$$\boldsymbol{(\epsilon_0 - E)^2 - t^2\left[3 + 4\cos\frac{k_x\,3a}{2}\,\cos\frac{k_y\sqrt{3}a}{2} + 2\cos k_y\sqrt{3}a\right] = 0} \qquad [3.12]$$

Solving Equation [3.12] to get the value of E while setting the reference energy as $\epsilon_0 \to 0$

$$\boldsymbol{E_{\pm}(\vec{k}) = \pm t\sqrt{3 + 4\cos\frac{k_x\,3a}{2}\,\cos\frac{k_y\sqrt{3}a}{2} + 2\cos k_y\sqrt{3}a}} \qquad [3.13]$$

Fig.3.3 shows the theoretically calculated band structure of the graphene π-bands according to Equation [3.13]. This plot gives us several important features for graphene. First, the valence and conduction bands (π and π* bands, respectively) touch each other at the K and K' symmetry points which make graphene a zero-gap semiconductor. Therefore, the intrinsic Fermi energy (E_F) of graphene is also defined to be at the Dirac points (band intersecting points, K and K'). However,

when graphene is doped the E_F moves into the upper (lower) cone which makes graphene n-type (p-type) doped. Second, the linear dispersion relationship suggests that the charge carriers in graphene are Dirac fermions, relativistic particles with zero rest mass and velocity equivalent to that of light.

Expansion of the energy dispersion around the Dirac points for k=K+ δK, where δK <<1, gives the electronic states near the Fermi level. Before moving on to this step, coordinates of K and K' points are required and defined as follows

$$\boldsymbol{K} = \frac{\boldsymbol{2\pi}}{\boldsymbol{3}}\left(\frac{\boldsymbol{1}}{\boldsymbol{a}}, \frac{\boldsymbol{1}}{\boldsymbol{\sqrt{3}a}}\right), \boldsymbol{K'} = \frac{\boldsymbol{2\pi}}{\boldsymbol{3}}\left(\frac{\boldsymbol{1}}{\boldsymbol{a}}, -\frac{\boldsymbol{1}}{\boldsymbol{\sqrt{3}a}}\right) \quad [3.14]$$

Considering only the K point coordinates, we get

$$\boldsymbol{k_x} = \frac{\boldsymbol{2\pi}}{\boldsymbol{3a}} + \boldsymbol{\delta K_x},\ \boldsymbol{k_y} = \frac{\boldsymbol{2\pi}}{\boldsymbol{\sqrt{3}a}} + \boldsymbol{\delta K_y} \quad [3.15]$$

substitution of k_x and k_y values from Equation [3.15] to *f(k)* and using a Taylor expansion (e^x= 1+x+…..) to expand the exponential and cosine terms around k_x and k_y gives

$$\boldsymbol{f(k)} \approx \frac{\sqrt{3}}{2}\boldsymbol{a}\left(\boldsymbol{\delta K_x - i\delta K_y}\right) \quad [3.16]$$

With the help of the above expression, Equation [3.11] can be rewritten as

$$\frac{\sqrt{3}}{2}\boldsymbol{a\ t}\begin{pmatrix} \boldsymbol{\epsilon_0 - E} & \boldsymbol{\delta K_x - i\delta K_y} \\ \boldsymbol{-(\delta K_x + i\delta K_y)} & \boldsymbol{\epsilon_0 - E} \end{pmatrix}\begin{pmatrix} \boldsymbol{\alpha_A} \\ \boldsymbol{\alpha_B} \end{pmatrix} = \boldsymbol{0} \quad [3.17]$$

Solution of Equation [3.17] with $\epsilon_0 \rightarrow 0$ is

$$\boldsymbol{E_{\pm}(\delta K)} = \pm\frac{\sqrt{3}}{2}\boldsymbol{at|\delta K|} = \pm\hbar\boldsymbol{v_f}\boldsymbol{|\delta K|} \quad [3.18]$$

where $V_f = \frac{\sqrt{3}}{2\hbar}at$ is Fermi velocity of the Dirac particles near the K and K' points. The value of V_f can be calculated by using nearest neighboring hopping interaction energy t that is ~ 2.80 eV and the lattice constant a. The second order terms become negligible for small values of δK and can be ignored for energies less than ± 1 eV from the Fermi-level [6]. After inserting all of the

parameters into, V_f it turns out to be constant ~ 10^8 cm/s [7]. Same result can also be obtained from the general expression of the energy $E = [(pc)^2 + (mc^2)]^{1/2}$ which gives the $E = pc$ relationship for light in the limit of $m = 0$ (as charge carriers in graphene behave like massless Dirac fermions for any low energy electronic excitations).

The density of states (DOS), number of available states per unit volume and energy, is also affected by the linear band structure of graphene. At the Dirac points, the DOS actually becomes zero and therefore there are no free charge carriers at these points. In general, the density of electronic states, $n(E)$, is defined by [2, 8]

$$\boldsymbol{n(E) = \frac{1}{(2\pi)^2} \int_{-\pi}^{\pi} d\theta \int_0^{\infty} \delta(E - E_k).\, kdk} \qquad [3.19]$$

We can then use the low-energy linear dispersion relation to express the above integral in terms of energy,

$$\boldsymbol{n(E) = \frac{1}{(2\pi)^2} 2\pi \int_0^{\infty} \frac{E}{(\hbar v_f)^2}.\, \delta(E - E_k)\, dE} \qquad [3.20]$$

From here, the total density of electronic states can be obtained by multiplying by the degeneracy of four, resulting from the two energy bands and spin states,

$$\boldsymbol{n(E) = \frac{g|E|}{2\pi(\hbar v_f)^2}} \qquad [3.21]$$

where g is the degeneracy. From the above equation, it is clear that the DOS vanishes linearly at the Dirac points where energy is zero. This is a direct result of the linearity of the energy dispersion in the vicinity of the Dirac points. This particular situation is in contrast to typical two dimensional metals (parabolic band structure) where the DOS is $n\,(E) = \; gm^*/2\pi\hbar^2$.

In summary, the linear dispersion of π and π* bands at the K- point along with the fact that they also touch leads to the conclusion that transport within graphene happens mainly by electrons hopping from one sub-lattice to the other. The linear band dispersion makes the electrons behave

like zero rest mass particles that travel with an effective speed of light $V_f = \frac{c}{300} = \frac{10^8 cm}{sec}$. Moreover, together with the vanishing density of states this leads to an extremely high room temperature mobility of charge carriers of $200000\ cm^2/Vs$ that exceeds the best value for mobility ($\sim 1400\ cm^2/Vs$) in silicon [9]. The mean free path of the charge carriers in graphene has been measured to be in the sub micrometer range which makes ballistic transport possible [10]. In addition, the near-relativistic behavior of the charge carriers in graphene leads to a number of interesting phenomenon such as the quantum Hall effect at room temperature [11] and Klein tunneling [12]. All these unique properties of graphene make it a promising candidate for replacing silicon in future field effect transistor based devices.

3.2 Graphene synthesis

The first method to isolate monolayer graphene from highly oriented pyrolytic graphite (HOPG) crystals was developed by Novoselov *et al*. in 2004 [1, 4]. In this method, layers of graphene are separated from the HOPG crystal using Scotch tape and are deposited onto SiO_2/Si substrate. The Scotch tape method has proved to be an easy way to obtain high quality graphene. However, the disadvantage of this process is the lack of control over the number of layers that makes it an inefficient process not suitable for large scale productions.

Another method for graphene production is epitaxial growth on silicon carbide (SiC) [13-15]. In this method, wafer sized graphene can be produced by heating the SiC to high temperatures (1400-1600°C) where the Si sublimates and the remaining C atoms form epitaxial graphene. One advantage of epitaxial growth is to avoid the lengthy process of exfoliating graphene from graphite and re-deposition of small flakes onto a substrate. Therefore, this method is a simple and reproducible process for graphene synthesis. However, a disadvantage of this process is that the

first layer of graphene acts as a buffer layer i.e. has no electronic properties of graphene [16]. In addition, this process also requires high temperatures, ultrahigh vacuum, as well as high cost which limits its use in applications.

The most recent technique used to grow large size graphene is chemical vapor deposition (CVD) [17-19] which is used in this dissertation. The detailed description of CVD grown graphene is given in next section.

3.2.1 Chemical vapor deposition growth

CVD is a process for depositing highly ordered, solid, thin-film materials from gaseous chemical precursors. In the simplest way, CVD requires flowing a precursor gas or gases into a chamber containing heated objects to be coated [20]. The chemical reactions occur on and near the hot surfaces, resulting in the deposition of a thin film on the surface. In addition, the by-products along with unreacted precursor gases are exhausted out of the chamber by the continuous gas supply. In this way, a wide range of materials can be deposited in the form of uniform films.

Particularly for graphene, the growth is carried out in a tube furnace by thermal decomposition of hydrocarbon gases on the surface of transition metal substrates (such as Cu, Ni, Pt, and Ru) [17-19, 21, 22]. The transition metal works as catalyst to promote the decomposition of the precursor gas which enhances the growth. Among all the transition metals, most reports for graphene growth have been on Ni and Cu mostly due to their cheaper cost. However, the growth mechanism is different for Ni and Cu and which will be discussed after describing the fundamental processes of nucleation and growth of graphene on polycrystalline metal substrates.

The growth of graphene via CVD method takes place in two modes (a) segregation, and (b) surface catalysis [23]. Both the modes have similar growth steps: transport of the reactants through the boundary layer to the catalytic substrate, adsorption of reactants at the substrate,

atomic/molecular diffusion, nucleation, and domain growth. All of the steps are strong functions of temperature (T), pressure (P) and the available amount of precursor gases. For a given T and P, the concentration of adsorbates will reach an equilibrium which is determined by the sticking coefficient for the precursor molecules. However, thermal fluctuations or substrate defects form local regions of supersaturation where stable graphene nuclei can form. The nuclei continue to grow rapidly until the remaining supersaturated carbon species are incorporated into the graphene domains and such domains merge into each other to form a continuous sheet of graphene.

In segregation mode, the C atoms diffuse into the bulk of the metal (e.g. Nickel) at higher temperatures (~ 900 °C), therefore the total amount of carbon available to the catalytic system is not self-limiting. As the solid solubility is a temperature dependent function, the C atoms come out from metal lattice during cooling. The number of graphene layers depends on the amount of diffused carbon and the rate of cooling. At fast cooling rate, the diffusion completely stops because the C atoms are frozen in the lattice at non-equilibrium concentrations. Conversely, for very slow cooling rates the C atoms completely come out from the bulk towards the surface and form clusters after encountering other carbon atoms.

Secondly, surface catalysis mode requires a metal (Copper) catalyst that has very low solid solubility (< 0.001 C %) for carbon even at higher temperatures (~ 1000°C). Due to the low solid solubility, Cu can be annealed very close to its melting point (~ 1050 °C) to maximize the surface diffusion and catalytic activity. The surface diffusion of C atoms forms random nuclei of graphene on the Cu substrate. The coalescence of different graphene nuclei forms a continuous sheet of graphene. The most remarkable part of graphene growth on Cu is its self-limiting behavior i.e. catalyst reactivity decreases as a function of graphene coverage. Once monolayer graphene covers

the Cu surface completely, the reaction stops [shown in Fig. 3.4]. Overall, CVD grown graphene has excellent electrical properties with large scale coverage.

In this work, a piece of 25-μm-thick Cu foil (purity ~ 99.99 %) of size ~ 1 cm × 1 cm was cleaned with acetone and methanol to remove any organic impurities before being loading into a hot wall furnace with 2''diameter quartz tube [schematic is shown in Fig. 3.5 (a)]. The tube was evacuated to ~ 100 mTorr at room temperature using a mechanical pump. At room temperature the quartz tube was flushed three times with research grade Ar/H_2 gas mixture (500/10 sccm) for 20 minutes each to remove oxygen and water vapors. The flow of Ar and H_2 was controlled by mass flow controllers and kept constant throughout the growth process. After purging the tube, furnace temperature was increased to 900°C with a ramp rate of 10 °C/min and kept constant for 20 minutes to anneal the Cu foil. This annealing process is required for the complete removal of the native oxide from the Cu surface as well as the formation of larger Cu grains. Then at the same temperature, 7 sccm of ethylene [with unaltered flow of Ar/H_2] was passed through the tube at a total pressure of~6 Torr to start graphene nucleation [temperature profile is shown in Fig. 3.5 (b)]. Full coverage of graphene on the Cu foil was achieved in 10 minutes followed by ceasing the flow of C_2H_4. Finally, the tube was allowed to cool naturally to room temperature in the Ar/H_2 environment.

3.2.2 Graphene transfer process

After CVD growth of graphene on Cu foil, it was transferred onto different semiconducting substrates such as SiC, Si, GaAs, and MoS_2 by using a polymer assisted method [24]. A thick layer (~ 300 nm) of polymethyl methacrylate (PMMA) was spin coated onto one side of the Cu foils at 3000 rpm for 45 seconds. This PMMA/graphene/Cu stack was baked on hot plate at 135°C for 10 minutes. In the next step, the Cu was etched in iron chloride [$FeCl_3$] solution. After complete

etching of the Cu within a few hours, the PMMA/graphene stack was washed in deionized (DI) water several times to remove traces of the Cu etchant solution. Such stack was kept in RCA solution (1:1:10 $HCl/H_2O_2/H_2O$) for 15 minutes at room temperature to remove any remaining Cu residues and subsequently rinsed with DI water a few more times. In the next step, the floating PMMA/graphene film was scooped out directly onto the desired substrate and flattened by spin coating (1000 rpm for 90 seconds). After drying the PMMA/ graphene/ substrate stack at 135°C for 10 minutes, the stack was then placed in hot acetone to remove the PMMA. In the last step, the graphene/substrate was washed with a mixture of ethyl alcohol and DI water to remove the traces of acetone. The schematic of the PMMA assisted transfer process is shown in Fig. 3.6. A vacuum annealing (P ~ 5 Torr) was further performed at 300 °C in an Ar/H_2 environment for 3 hours to obtain a clean graphene surface.

Figure 3.7(a) shows an optical microscope image of graphene transferred onto a SiO_2/Si substrate. In this image, the pink and yellow contrast represent the graphene and SiO_2, respectively. The light pink color becomes darker with the increasing number of graphene layers. The graphene growth is further confirmed by Raman spectroscopy which is a fast, non-destructive technique ideal for distinguishing monolayer graphene from multilayer graphene and graphite. Raman spectra were taken with a Horiba Raman system using a 532 nm excitation laser with a 2400-line diffraction grating. Figure 3.7(b) shows a typical spectrum of CVD grown graphene transferred onto a SiO_2/Si substrate. Transferred graphene exhibits two characteristic peaks; 2D peak at 2670 cm^{-1} and G peak at 1579.89 cm^{-1}. An absence of defect-induced D-peak in Raman spectra suggests growth of good quality graphene.

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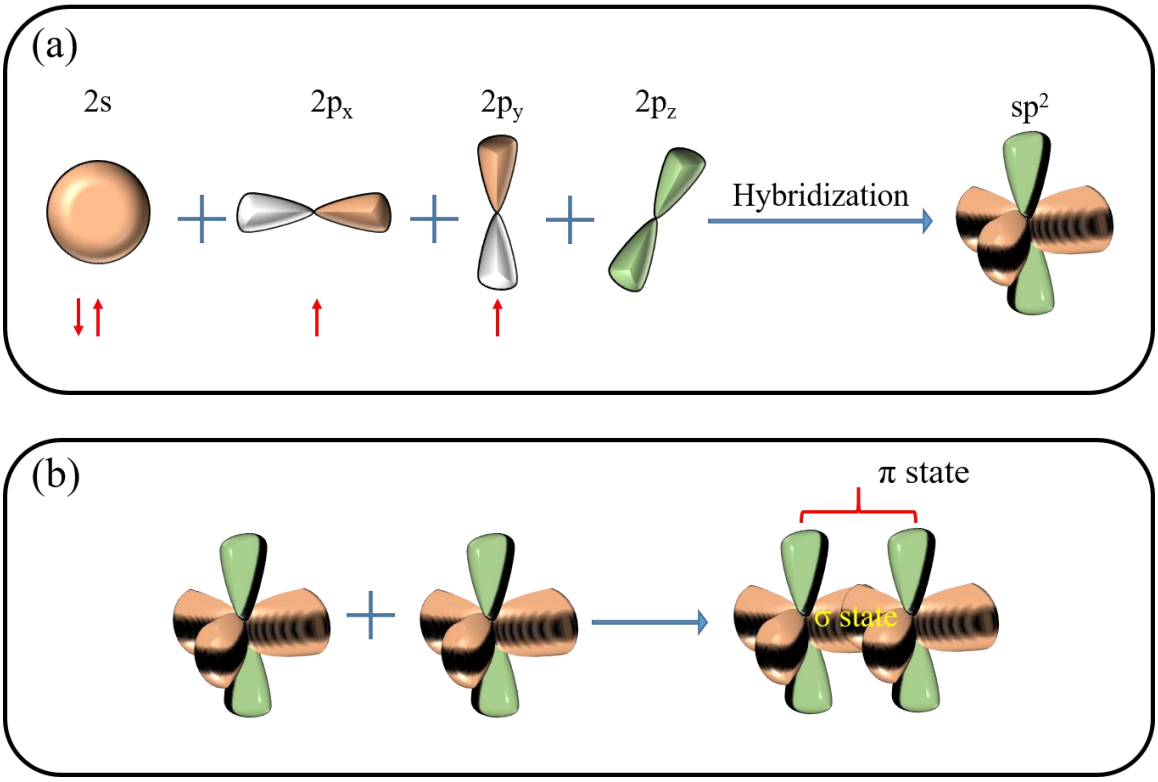

Figure 3.1: (a) Sp^2 hybridization scheme in carbon atoms, and (b) formation of π and σ states in graphene.

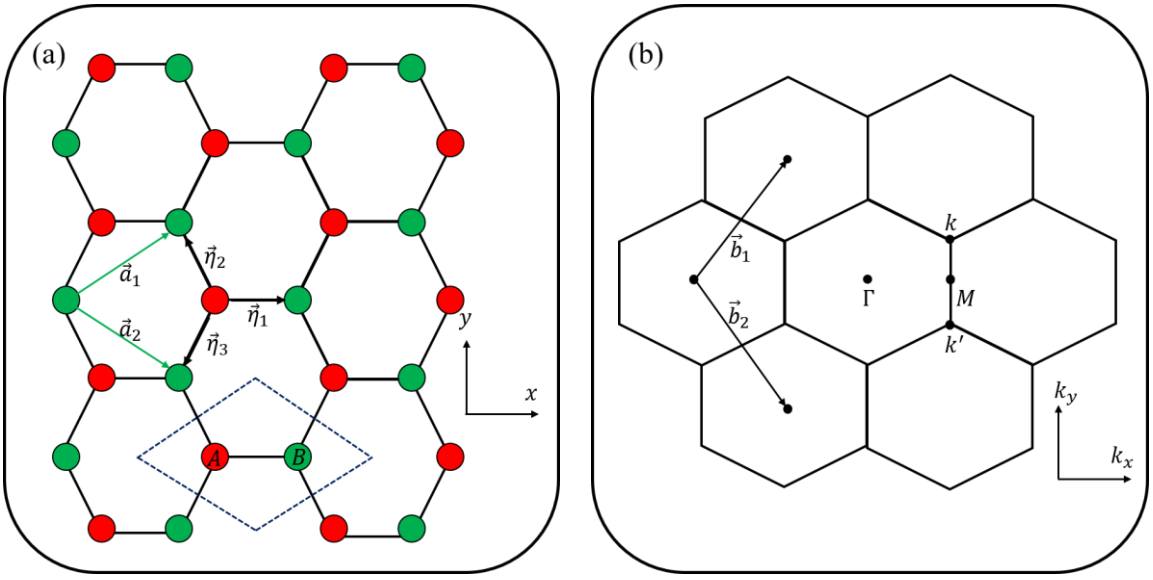

Figure 3.2: (a) The graphene hexagonal lattice is made of two inter-penetrating triangular lattices with unit vectors $\overrightarrow{a_1}$ and $\overrightarrow{a_2}$. The primitive unit cell is shown by dashed diamond shape, and (b) the first Brillouin zone with reciprocal space lattice vector $\overrightarrow{b_1}$ and $\overrightarrow{b_2}$.

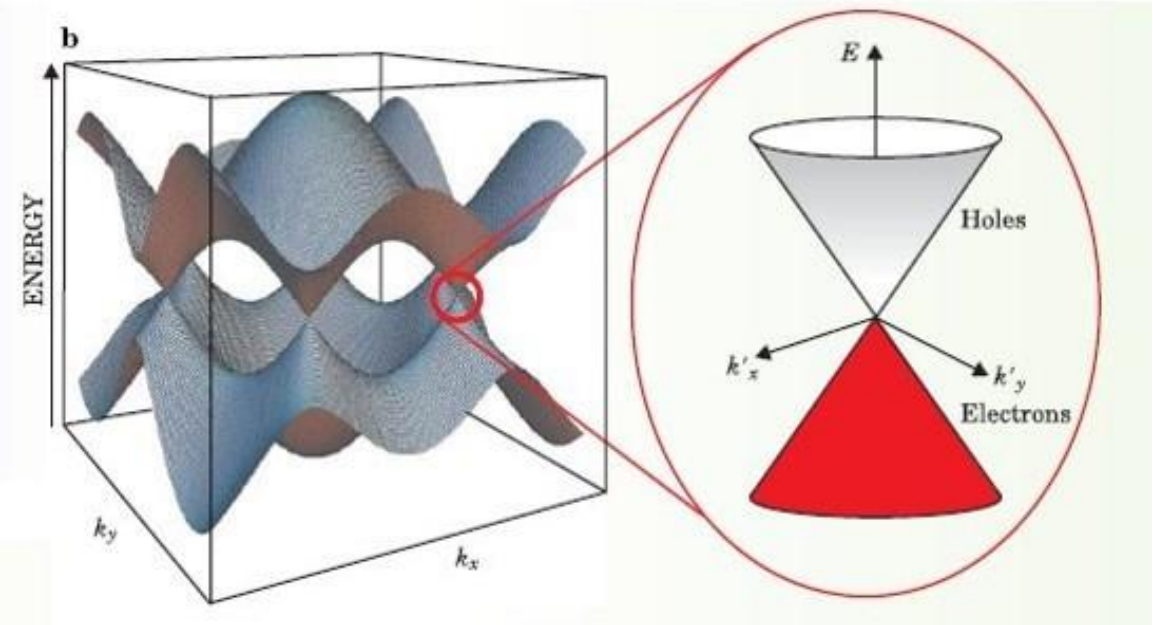

Figure 3.3: Graphene band structure from the solution of nearest neighbor tight binding model where encircled area exhibiting linear dispersion close to the Dirac points, K and K′ (image adapted from wikipedia.com).

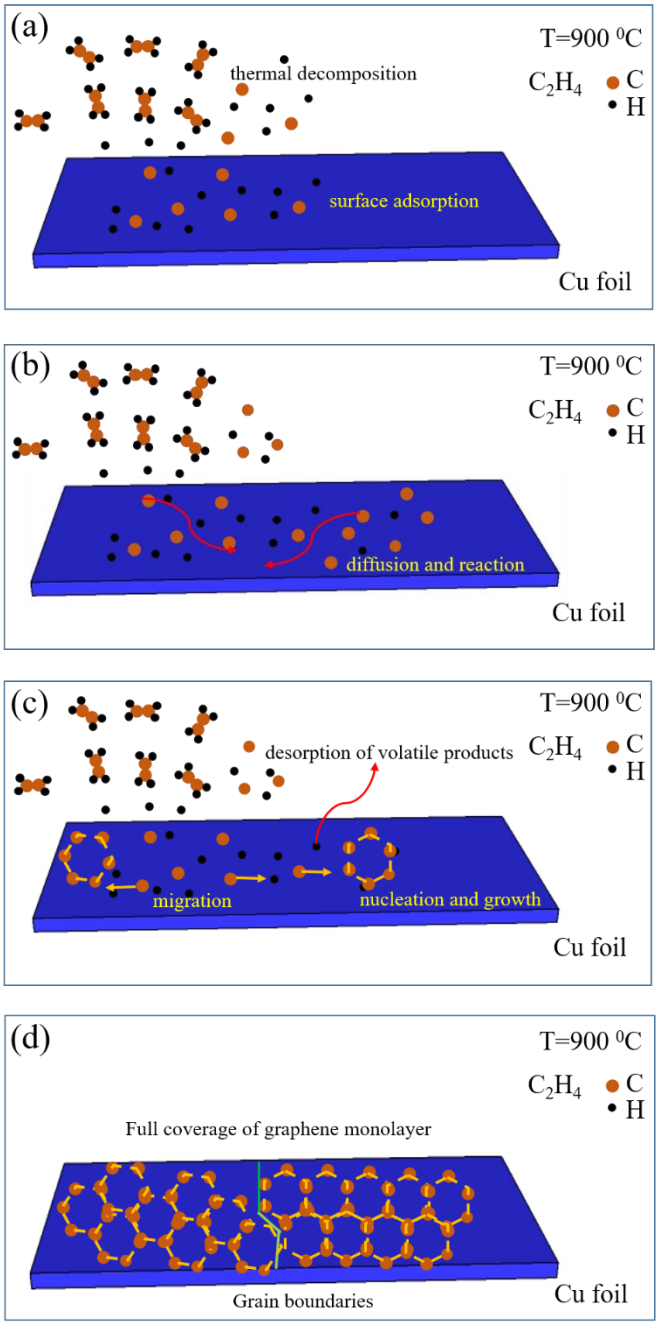

Figure 3.4: Graphene growth on Cu substrate in surface catalysis mode, (a) thermal decomposition, surface adsorption, (b) diffusion and reaction with substrate, (c) desorption of volatile by products, and (d) nucleation and growth of monolayer graphene.

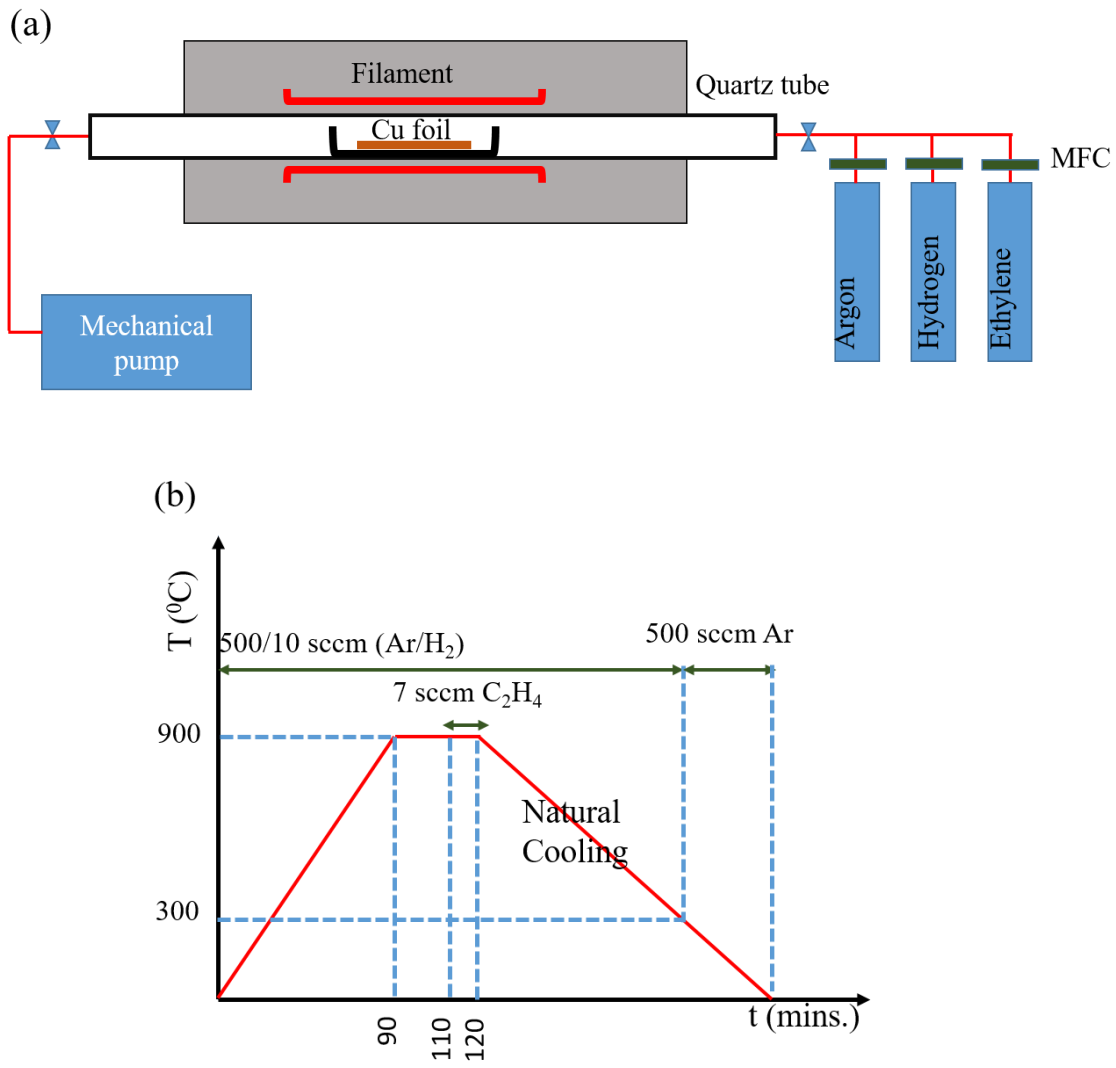

Figure 3.5: Schematic of (a) experimental setup and (b) temperature profile used in monolayer graphene growth on Cu substrate.

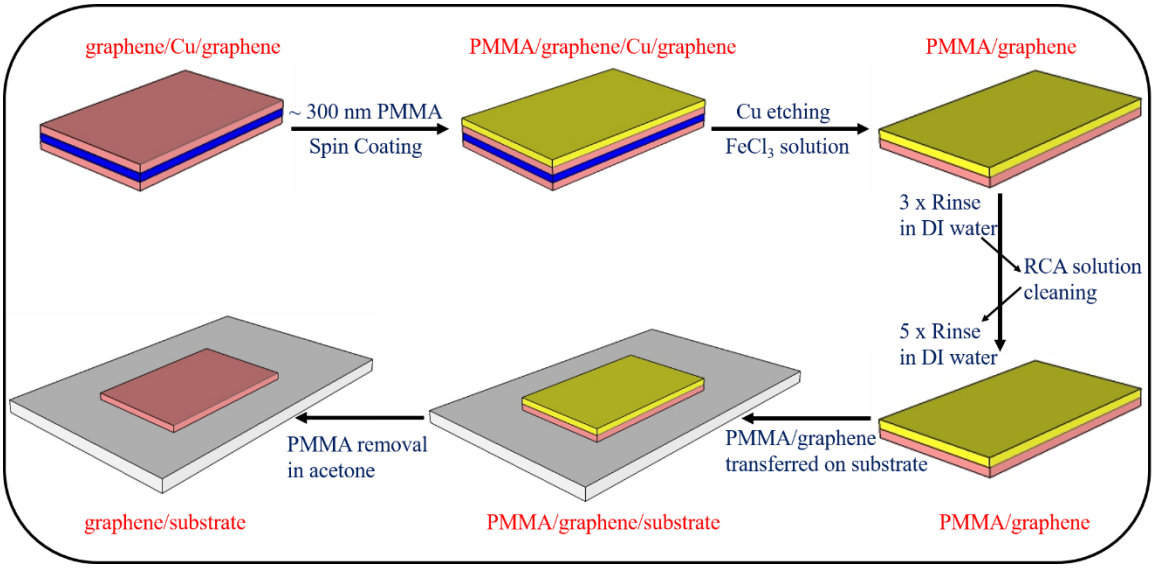

Figure 3.6: Schematic representation of PMMA assisted graphene transfer method.

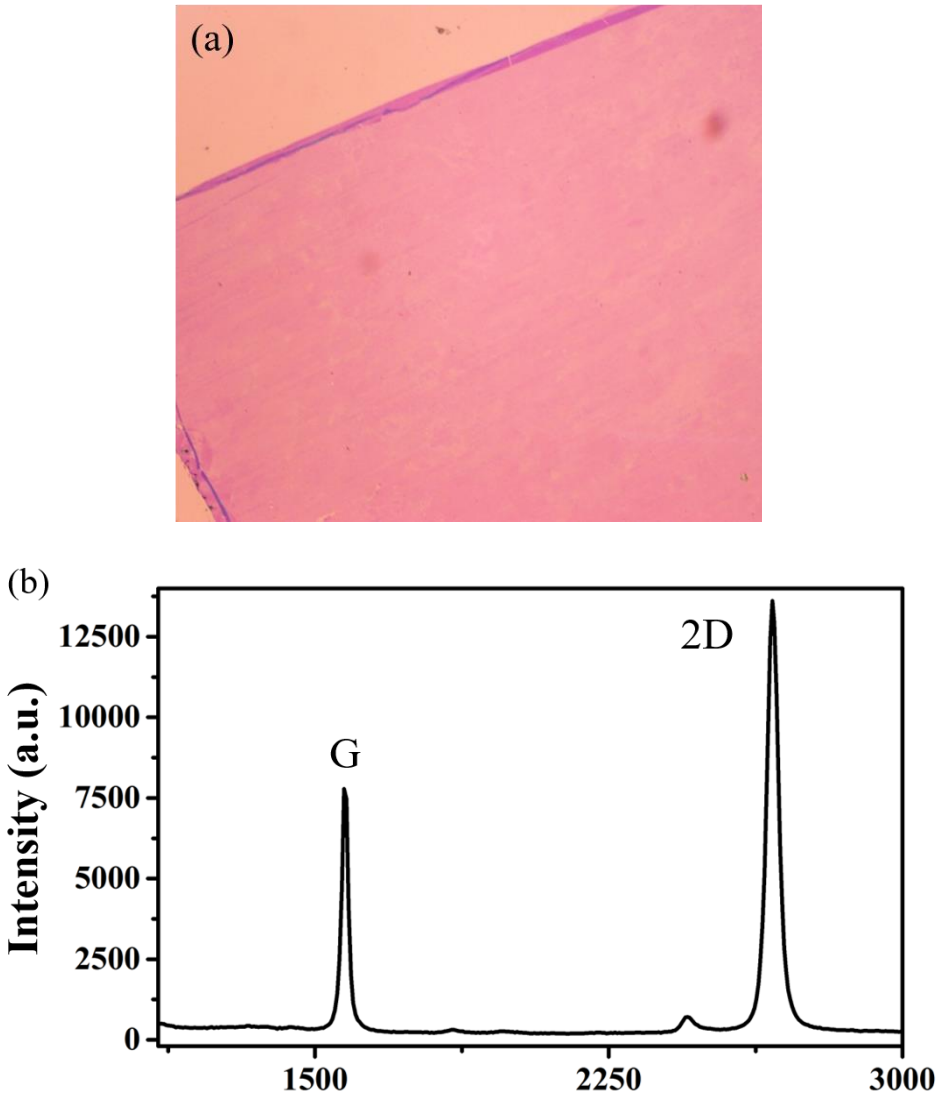

Figure 3.7: (a) Optical microscope image at 5x magnification, and (b) Raman spectra of CVD grown graphene transferred onto SiO_2/Si substrate.

Chapter 4
Device fabrication and characterization methods

In this dissertation, we fabricated graphene Schottky diodes with conventional (SiC, Si, GaAs) and van der Waals (MoS_2) semiconductors using photolithography. In this chapter, section 4.1 describes cleaning procedures for the semiconductor substrates. Section 4.2 explains photolithography processes used in device fabrication. Section 4.3 gives the overview of the different characterization methods.

4.1 Substrate preparation

In order to remove particles, organic and metallic contaminations, substrate cleaning is an essential part of the semiconductor device processing. Therefore, all semiconducting substrates are cleaned before any photolithography steps. The cleaning method varies based on the substrate i.e. hydrogen etching for silicon carbide (SiC) and wet chemical cleaning of Si and GaAs.

4.1.1 SiC cleaning

As received, solvent cleaned SiC substrates show a large number of deep, irregularly directed mechanical scratches over the entire surface as shown in Fig.4.1 (a). These scratches are caused by mechanical polishing and are bad for device performance, therefore it is necessary to remove such scratches. Hydrogen etching has been widely used to flatten the surface of a SiC wafer [1, 2]. In our hydrogen etching experiments, solvent cleaned SiC substrates are placed on a molybdenum (Mo) strip heater ($2\times0.5\times0.005$ in^3) inside a homemade double wall etching chamber. First, the chamber is purged with Ar (with a flow rate of 40 sccm, 5N purity) gas for 10 minutes to remove oxygen. Then H_2 (flow rate of 20 sccm, 5N purity) gas is added without altering the Ar flow. In

the second step, high current (~ 170 A) is passed through the Mo strip heater to heat the SiC substrate to about 1600°C for 15 minutes and then subsequently allowed to cool down in an Ar environment. During this whole process, cold water is flown in between the two walls of the chamber for efficient heat dissipation in order to aid in cooling. The reaction of SiC with H_2 gas at high temperature results in gaseous hydrocarbons and elemental silicon byproducts as given below

$$2SiC + 5H_2(\uparrow) \rightarrow 2SiH_4(\uparrow) + 2C_2H_2(\uparrow) \quad [4.1]$$

High temperature H_2 etching produces regular arrays of wide (few hundred nanometers) atomically flat terraces separated by steps of unit cell height as can be seen in Fig.4.1 (b). In addition, hydrogen etching process provides a chemically inert surface by saturating the surface dangling bonds [3, 4].

4.1.2 Silicon cleaning

As received Si substrates have a very thin native oxide layer that affects the electrical properties of devices. We used a buffered oxide etching (BOE) method to remove the native oxide [5]. In the first step, acetone (two times in an ultra-sonicator for 10 minutes each) is used to remove organic impurities from the Si substrates. Later on, the Si substrates are kept in methanol which works as a solvent for acetone. These solvent cleaned substrates are rinsed in deionized water (DI) and then dried with nitrogen gas. In the next step, the solvent cleaned substrates are kept at 70°C in an RCA solution (1:1:5 HCl: H_2O_2:H_2O) for 10 minutes to remove metallic impurities, followed by a rinsing with DI water and a drying with nitrogen gas. In the last step, the Si substrates are kept in a BOE solution (7:1 volume ratio of 40 % NH_4F in water to 49 % HF in water) for 15 mins to remove the native silicon dioxide from the Si wafers. This BOE cleaning process yields an H-terminated smooth Si substrate [5].

4.1.3 Gallium arsenide cleaning

GaAs substrates are also processed through a standard degreasing method using an ultra-sonication in acetone, methanol and DI water. Next to remove the interfacial oxide of gallium and arsenic, the samples are immersed in NH_4OH/H_2O (1:2) solution for 3 minutes and rinsed with DI water followed by drying the surface with N_2 gas. After this step the surface becomes covered by elemental arsenic and a small amount of gallium sub-oxide which can be removed by dipping the samples in HCl: H_2O=1:1 solution for 1 minute. These HCl/H_2O treated samples are then soaked in $(NH_4)_2S$ (40%) for 10 minutes at room temperature to obtain a sulfur passivated GaAs surface [6].

4.2 Device fabrication

4.2.1 Photolithography

Photolithography is a method used to transfer a pattern by selective exposure to a radiation source from a photomask to a photosensitive material deposited on a substrate [7]. The photolithography process involves several steps which are substrate preparation, photoresist (PR) coating, pre-baking, ultra-violet (UV) exposure, developing and post-baking. The procedure of substrate preparation has already been discussed in previous section. In this work, all substrates (SiC, Si, and GaAs) are spin coated (3000 revolutions per minute for 45 seconds) with Shipley -1813 positive PR. The Spin coating process results in a uniform, thin layer of PR that is baked at 105°C for 60 seconds on a hot plate. After baking, the PR coated substrates are exposed to UV light for 55 seconds through a transparent glass plate with patterned chromium areas on it, known as a photomask. The mask is placed between the radiation source and the wafer to selectively expose parts of the substrate to UV light. The UV exposed area of a positive PR becomes soluble in the

developer solution. As a result, the exposed PR parts are removed by keeping the substrate in MF-321 developer solution for 60 seconds. The remaining PR would become a protecting layer for the underlying substrate. Immediately after developing the pattern the samples are then loaded into an electron-beam evaporation system for dielectric deposition.

4.2.2 Electron-beam evaporation

Electron-beam (e-beam) evaporation is the most widely used vacuum evaporation technique for preparing high quality metal and dielectric thin films [8]. The evaporant material is kept in a water cooled crucible. The purity of the evaporant is ensured because only a small amount of material melts (or sublimes) while the rest of the material close to the crucible surface remains unmelted. In the most common configuration the electrons are thermionically emitted from a heated filament. The filament is kept away from the direct line of sight of the evaporant and substrate to avoid the possible contamination to film from the heated source. The filament is biased negatively with respect to a nearby grounded anode to accelerate the electrons. In addition, a transverse magnetic field is also applied to deflect the e-beam in a 270° circular arc to focus it on the crucible. This deflection is necessary because the electrons are emitted in a random manner and must be directed toward a very small area where the evaporation will occur. Once the e-beam strikes the target surface, the kinetic energy of electron is transferred into thermal energy. Although the energy transferred by a single electron is quite small, the large number of electrons striking the surface provides sufficient energy to vaporize the target material. This process produces energy of several million watts per square inch due to the high intensity of heat generated by the electron beam, therefore the evaporant holder must be water cooled to prevent it from being destroyed. The schematic of the e-beam evaporation system is shown in Fig.4.2.

In this work, SiO_2 (100 nm) is deposited on top of the semiconductors using a Telemark e-beam evaporator that can achieve the base pressure of 2.0E-6 Torr. After achieving base pressure, 1.2 sccm oxygen is back flown into the chamber to promote oxide deposition. Loose pieces of SiO_2 are placed in an alumina crucible and melted at temperature of ~2400°C. The emission current is set by simply increasing it from zero until the desired deposition rate is achieved (usually ~60 mA gives deposition rate of ~ 10 Å/sec on the crystal monitor) at constant accelerating voltage of 10 KV.

4.2.3 Lift-off process

Before e-beam evaporation, a patterned PR layer was spin coated on the substrates where the PR was selectively removed in the areas where material (dielectric or metal) is to be deposited [7]. However, the material deposits over the entire surface of the substrate during the e-beam evaporation process. Therefore, it is necessary to remove the material from the undesired places which can be done by the lift-off process. In the lift-off process, the PR layer serves as a sacrificial material that will be dissolved in a solvent bath causing the undesirable material to be removed. There are some issues that need to be addressed when performing a lift-off process. The biggest issue is that the material layer might remain on the unwanted regions of substrate. This could be due to a very thin layer of PR below the deposited film which cannot dissolve properly. It is also highly possible that the material reattached to the open surface at a random locations and which would make it very difficult to remove after drying. In addition, during material deposition the film can cover the sidewall of the PR which would not allow the lift-off solvent to dissolve the PR. Therefore, all the steps should be performed very carefully in order to fabricate good devices.

In this work, the substrates are kept in acetone at 70°C on a hot plate after dielectric deposition. The hot acetone dissolves the remaining S-1813 PR along with the undesirable material

on top of it and only leaves the material at the desired locations on the substrate. Fig.4.3 shows the procedure for the device fabrication which includes photolithography process, dielectric deposition, and lift-off.

4.2.4 Metallization

After the dielectric lift-off process, the same photolithography steps (spin coating, baking, UV-exposure, and pattern development) are performed for metallization. For the metallization process, a layer of metal is deposited on the substrate to provide electrical contact to the devices. Graphene makes Ohmic contact with gold (Au), therefore we first patterned Cr/Au electrodes on the semiconducting substrates and then transferred graphene on top. For all substrates, Cr/Au (10/150 nm) is deposited on top of SiO_2 (100 nm) via e-beam evaporation in a vacuum chamber with base pressure of 2.0E-6 Torr. Here, the SiO_2 provides insulation between the top metal electrode and the bottom semiconductor. Here, a thin layer of chromium is used as an adhesion promoter because gold does not make good contact with SiO_2 [9]. After metallization, the metal lift-off process is performed in hot acetone to remove metal from undesired locations. Next, an Ohmic contact is formed on the back of each semiconductor to complete the diode structure. Nickel of thickness of 100 nm is deposited on back of SiC via sputtering and annealed at 600°C in an argon environment to make a low resistance contact [10]. Conducting silver paste is used to make Ohmic contact on the back of Si. On the other hand, Ohmic contact on GaAs is formed by depositing a multilayer AuGe/Ni/Au (50/20/100 nm) using e-beam evaporation followed by a rapid thermal annealing at T~400°C in a forming gas environment [11]. After pre-patterning the diode structure, CVD grown graphene is transferred on to it using the PMMA assisted transfer method described in chapter 3.

4.3 Characterization techniques

4.3.1 Temperature dependent current-voltage measurements

Current-voltage (I-V) measurements are the most standard characterization technique to determine key parameters, ideality factor (η) and barrier height (ϕ_{B0}), of a Schottky diode. However, I-V measurements at one particular temperature (T) does not give any information about the carrier transport mechanism. Therefore, temperature dependent I-V measurements are required for a better understanding of the device transport mechanism.

In this work, two different set up are used to measure the T dependent electrical properties. The first I-V characterization set up consists of a Keithley 2400 source meter, a custom made four probe station mounted in a vacuum chamber with a SHI cryogenic compressor, a Lakeshore 300 temperature controller and a computer that controls and displays the real time measurements. The sample is mounted on top of a molybdenum plate using double sided insulating tape. A 25-micron thick gold wire is soldered to connect the sample with metal posts on the plate. The metal posts make pressure contact with the four probe station. All the components are interfaced in a LabVIEW program that allows controlled T dependent I-V measurements.

Another set up to perform such measurements was quantum design's MPMS-XL SQUID magnetometer with modified transport probe which allows to perform electrical measurements down to liquid helium temperature. To modify the probe, a circular 6-pin holder (2 pins are removed out of total 8 pins) is mounted at the bottom end of the probe. Next, the sample is mounted on top of a chip carrier (Au/SiO_2) by using double sided kapton tape. The chip carrier and sample are connected via a gold wire (25 μm). Finally, this chip carrier is attached to second 6-pin holder with the help of rubber cement and connections are made by indium soldering of gold wire. The second holder with the sample is attached to the first one and secured by using non-magnetic

screws through the two open holes [setup is shown in Fig.4.4]. For T dependent I-V measurements, an external device controller (EDC) is connected to QD's Multiview operating system along with a Keithley 2400 source meter through a GPIB interface.

The detailed description of Schottky junctions has already been discussed in section 2.3. In general, the Schottky diode parameters can be extracted by plotting its semi-logarithmic $[ln(I) - V]$ characteristics as shown for graphene/Si in Fig.4.5. Three different regions can be clearly seen in such plot: the initial nonlinear region "a" is due to non-exponential behavior of the diode when $V < 3kT/q$, middle linear region "b" and last saturating region "c" where series resistance (R_S) dominates the transport mechanism. The Schottky barrier height and the ideality factor both are obtained from the middle linear region. First, saturation current (I_S) is obtained from the Y-axis intercept using linear fitting to region "b" [12]

$$I_S = AA^*T^2 exp(-q\phi_{B0}/kT) \quad [4.2]$$

Thus,

$$\phi_{B0} = (kT/q)\, ln(AA^*T^2/I_S) \quad [4.3]$$

The ideality factor (η) can be obtained from the slope of the linear fit to region "b" as follows

$$\eta = (q/kT)(dV/d\,(ln\, I)) \quad [4.4]$$

However, R_S can be obtained from region "c" where the I-V characteristics of a Schottky diode obey the TE model given by [13]

$$I = I_S\, exp[q(V - IR_S)/\eta kT] \quad [4.5]$$

and the differentiation of the above equation with respect to I would give

$$dV/d(ln\, I) = R_S I + \eta kT/q \quad [4.6]$$

Thus, R_S can be obtained from the slope of $dV/d(ln\, I)$ versus I plot.

4.3.2 Scanning tunneling microscopy/spectroscopy

Sir Gerd Binning and Sir Heinrich Rohrer invented scanning tunneling microscopy (STM) in 1981 and won the Noble prize for it in 1986 [14]. Since then STM has become a powerful tool to image the surface of conducting samples with real space atomic resolution which also allows to study local electronic properties down to atomic limits. An ultra-high vacuum (UHV) STM can provide spatial resolution in the sub-angstrom range in vertical direction (along z-axis) with a lateral resolution of one angstrom (depends on tip radius and bias voltage) [15]. Because of these capabilities, STM is a very useful technique in various research areas such as nanoscience.

The physical phenomenon behind the STM is the quantum mechanical-tunneling effect that accounts for the possibility of electrons to overcome a potential barrier which would be prohibited in classical mechanics [15]. In experiments, a sharp metallic tip usually made of tungsten or a platinum-iridium alloy is brought to within several angstroms of a conducting surface. When a bias voltage is applied between tip and sample, electrons from the tip begin to tunnel through the vacuum gap into the sample or vice versa, depending upon the sign of the bias voltage. This flow of electron gives rise to a tunneling current that can be measured as a function of the (x, y) location and applied voltage with the help of piezoelectric transducers. These transducers provide motion in the three orthogonal directions. A saw tooth waveform rasters the tip in the x-direction, while a ramp voltage advances the raster signal in the y-direction. Another voltage applied to z-axis transducer maintains separation of a few angstroms between the tip and the sample. The tunneling current has an exponential dependence on the sample-tip separation which can be written as $I_t \propto e^{-kd}$ where d is the distance between the tip and the sample surface. This exponential dependence makes STM very sensitive to surface corrugations. The schematic

illustration of the operation of an STM is shown in Fig. 4.6 (a). The picture of low temperature STM used in this dissertation is shown in Fig. 4.6 (b).

The STM can be operated in two different modes, constant current and constant height mode [15]. In constant current mode, the tip is scanned over the surface while the feedback loop keeps the tunneling current constant by adjusting the height of the tip at each measurement point. Whenever, the system detects an increase (decrease) in tunneling current, it adjusts the voltage applied to the z-axis piezo transducer to decrease (increase) the distance between the tip and the sample. Therefore, the motion of the scanner corresponding to height change constitutes the data set that generates a topographic image of the sample surface. Constant current mode is most frequently used in STM imaging because it can measure an irregular surface with high precision. However, the finite response time of the feedback loop and piezoelectric transducer makes scanning slower in this mode.

On the other hand, in constant height mode the tip moves in a horizontal plane above the sample surface and the tunneling current varies depending on topography and the local surface electronic properties of the sample. The measurement of tunneling current modulation at each location gives the data set. The advantage of constant height mode is that it allows scanning with a faster speed, however, it provides useful information only for relatively smooth surfaces. The schematics of constant current and constant height mode are shown in Fig. 4.7 (a) and (b).

In addition to the topographical information, STM can be used to obtain information about electronic states and energy spectra from the local differential conductance (dI/dV). This mode is called scanning tunneling spectroscopy (STS). In STS experiments, the tunneling current is measured as a function of the bias voltage applied between the tip and the sample. For small bias voltages, the tunneling current can be written as

$$I \propto \int_0^{eV} \rho_S(E_F - eV + \epsilon)\rho_T(E_F + \epsilon)\, d\epsilon \quad [4.7]$$

where ρ_S and ρ_T are the density of states (DOS) of the sample and tip respectively. Under the assumption of a constant DOS for the tip, the dI/dV is directly proportional to the sample density of states

$$\frac{dI}{dV} \propto \rho_S(E_F - eV + \epsilon) \quad [4.8]$$

To obtain STS data, the STM tip is placed above a particular location of the sample in constant height mode (feedback loop is turned off). In this way, a bias voltage of desired range is swept in between the tip and sample. During the sweep, the change in tunneling current as a function of electron energy is recorded and referred to as a $I - V$ curve. However, the slope of $I - V$ curve (i.e. dI/dV) is more fundamental as it corresponds to the electron density of states at the local position of tip. Taking numerical differentiation of $I - V$ plot at each voltage is one way to produce a dI/dV plot but it produces very noisy data. Therefore, it would be much better to measure the derivative directly. Such a measurement is possible using a lock-in amplifier that filters the noise at frequencies away from a selected modulation frequency. The idea is to add a small AC voltage (dV) to the slowly varying DC bias voltage that is applied to the tip and the sample. When the feedback loop is removed, this small AC voltage modulation gives the current modulation dI at the same frequency. This current modulation is due to two factors; resistance and reactance of the circuit. The resistance component is the dI that carries the DOS information for the given energy and spatial location. On the other hand, the reactance component is 90° out of phase with the resistive component and can be removed by suitable selection of the lock-in phase.

In this dissertation, we used variable temperature and low temperature ultra-high vacuum Omicron STMs, at room temperature and at liquid nitrogen temperature (77K) with base pressure

of ~1 × 10^{-11} Torr, to study the morphology and electronic properties of graphene Schottky junctions.

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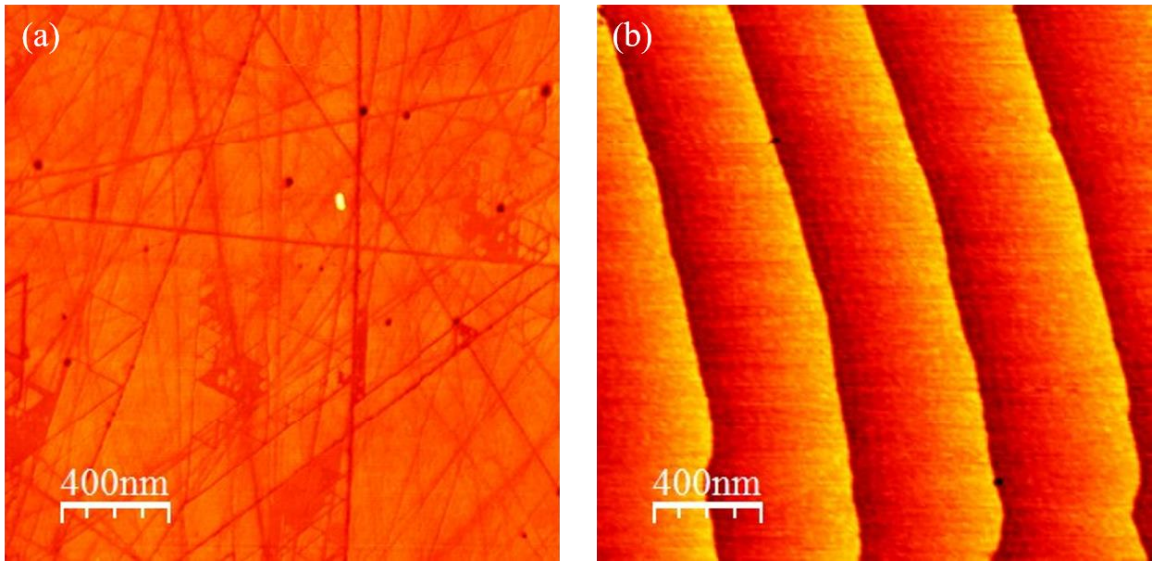

Figure 4.1: AFM images of the 6H-SiC (0001) substrate (a) before and (b) after the H_2 etching at ~1600^{o}C for 15 mins.

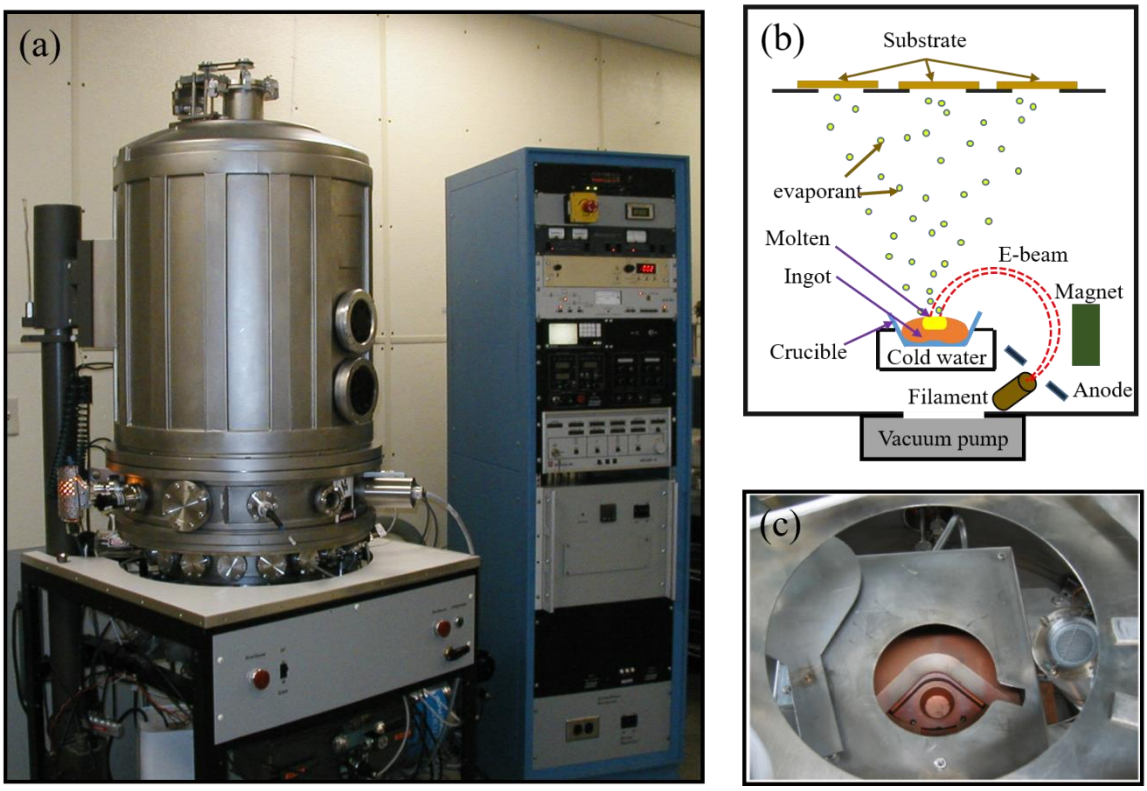

Figure 4.2: (a) Photograph of Telemark e-beam evaporation system. (b) Schematic diagram of e-beam evaporation system. (c) Picture of water cooled hearth.

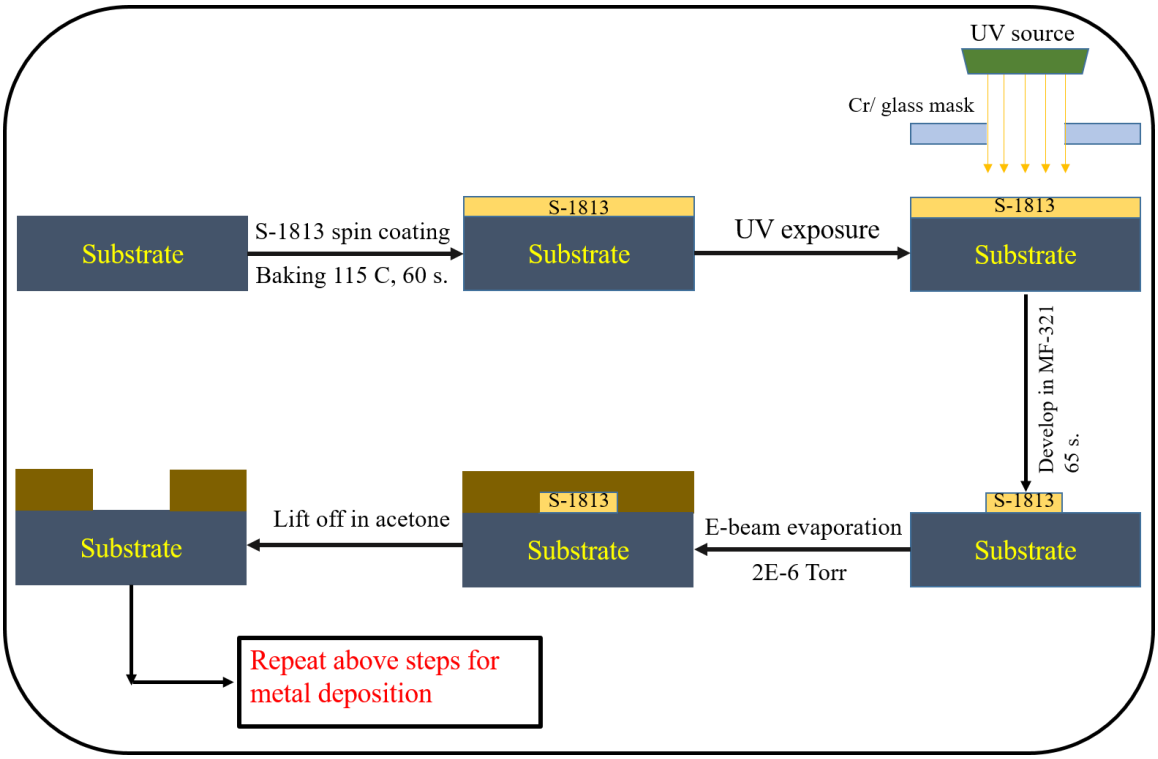

Figure 4.3: Schematic of device fabrication process using photolithography.

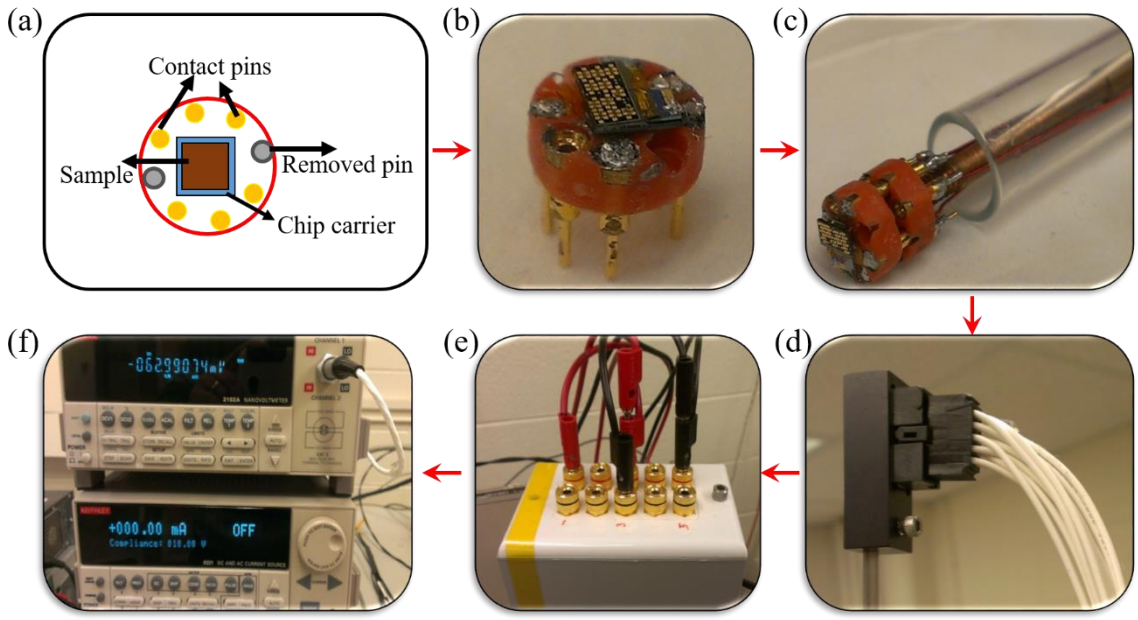

Figure 4.4: Modified sample holder for quantum design MPMS system. (a) Schematic of sample holder. (b) Picture of sample and chip carrier mounted on first holder. (c) First holder connected to second holder on one side of transport rod. (d) Electrical connections on the other side of transport rod. (e) Picture of electrical connection switch box, and (f) Keithley source meter.

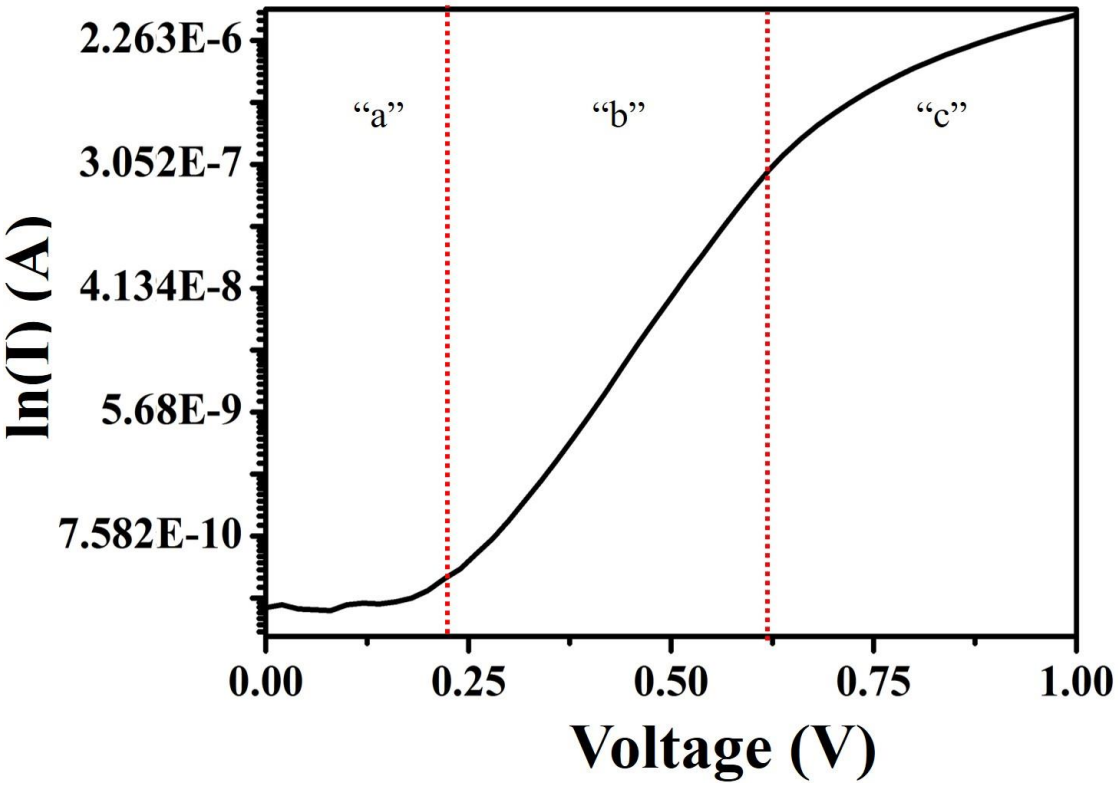

Figure 4.5: Room temperature $\ln(I)$ versus V plot for graphene/n-Si Schottky junction showing non-exponential region "a", linear region "b" and series resistance dominated region "c".

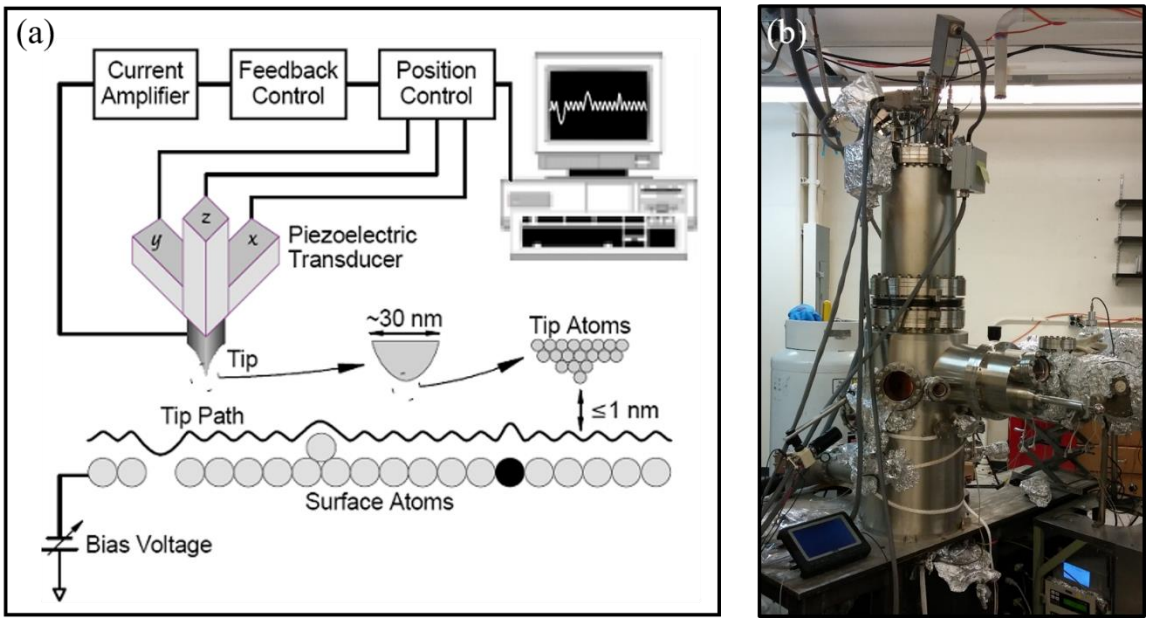

Figure 4.6: (a) Schematic view of scanning tunneling microscope (image adapted from wikipedia.com). (b) Picture of Omicron low temperature STM used in this dissertation.

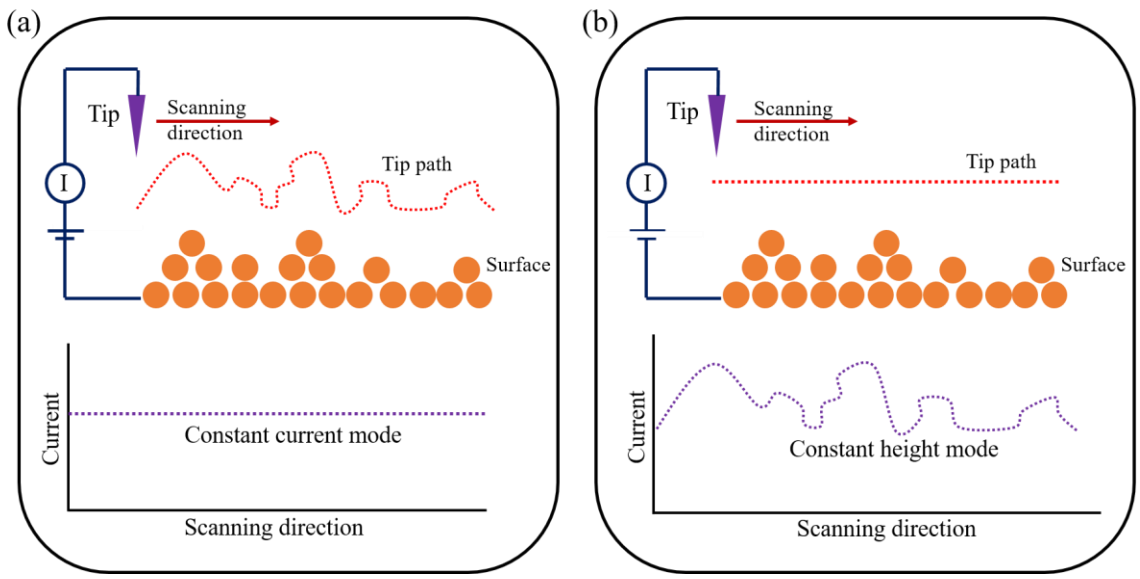

Figure 4.7: Schematic view of (a) constant current, and (b) constant height imaging mode in a scanning tunneling microscope.

Chapter 5
Intrinsic inhomogeneity in barrier height at monolayer graphene/SiC Schottky junction

5.1 Introduction

Metal-semiconductor Schottky junctions, characterized by SBH and ideality factor, are crucial to the operation of semiconductor devices. Non-ideal behaviors of Schottky junctions have been correlated to spatial inhomogeneity at the junction due to interface roughness, metal layer thickness variations, dislocations and grain boundaries in the metal layer, and the presence of atomic steps in the semiconductor [1-3].

Graphene, a semimetal with linear energy dispersion [4], also forms Schottky junctions when interfaced with semiconductors [5]. With a tunable work function by an electric field [6], graphene-semiconductor Schottky diodes [5], solar cells [7], photo detectors [8], and three terminal transistors with up to 10^6 on/off ratio [9, 10] have been reported. Of particular interest is the graphene/SiC Schottky junctions, where epitaxial graphene (EG) can be grown directly on wafer-sized substrates [11, 12]. In addition, hexagonal SiC is a polar material available with two surface terminations: Si-face (0001) and C-face (000-1). The opposite direction of polarization of the two substrates leads to p- and n-type doping in graphene on Si- and C-SiC, respectively [13].

Simple TE theory is typically invoked to calculate the SBH of graphene/ semiconductor Schottky junctions, which inherently assumes a perfect homogeneous junction interface. However, large variations in SBH, ranging from 0.08 eV to 1.15 eV, have been reported for the graphene/Si-SiC Schottky junctions [5, 14-18]. While these fluctuations can be related to the number of graphene layers, e.g., EG on SiC typically consists of one to three layers on a warped interface

layer [19], and exfoliated and CVD graphene studied are typically single layer [20]. The impact of spatial inhomogeneity has not been fully considered, particularly when graphene is normally susceptible to form ripples and ridges upon interfacing with another material [13, 21]. The lateral barrier inhomogeneities are speculated as the possible cause for different SBHs obtained from C-V and I-V measurements for few layer EG/Si-SiC junction [22]. Such variation in SBH has also been related to step length in EG/4H-SiC (0001) [23]. S. Rajput *et al.* also shown that the atomic-scale spatial fluctuations in SBHs directly follow the undulation of ripples in CVD graphene transferred onto both Si- and C-face SiC using STM/STS [13]. However, no transport study has directly related SBH variations to spatial inhomogeneities in graphene/SiC Schottky junctions.

In this chapter, we investigate the effect of intrinsic spatial inhomogeneities at monolayer graphene/SiC Schottky junctions using Raman spectroscopy, STM/STS, and T dependent I-V measurements. To minimize interfacial charge contributions to SBH variations, Schottky junctions are fabricated on chemically inert Si- and C-SiC substrates. The substrate preparation and device fabrication process has already been discussed in chapter 4 (section 4.1 and 4.2). By transferring monolayer CVD graphene onto these substrates, we also eliminate the possible SBH variations due to layer thickness.

We observe non-ideal behavior such as increase of zero bias SBH and decrease of η with increasing temperature in I-V characteristics. Such behavior is directly related to the three main types of spatial inhomogeneities as revealed by STM: atomic scale ripples, nanometer ridges, and deformation caused by SiC steps. Spatially resolved STS measurements over ripples show a Dirac energy at 270 meV with full width at half maximum (FWHM) of 70 meV. This broad distribution indicates modified thermionic emission-diffusion theory is necessary to better estimate the SBHs. Assuming a Gaussian distribution of the barrier height, we find mean barrier heights of 1.30 eV

and 1.16 eV for graphene/C-SiC and graphene/Si-SiC junctions with standard deviations of 0.18 and 0.16 eV, respectively.

5.2 Results

5.2.1 STM/STS on graphene/SiC junction

The transfer of graphene is confirmed by Raman spectroscopy and STM imaging. The 2D Raman band exhibits the same frequency (2655 ±2cm^{-1}) for graphene transferred on both faces of SiC, indicating similar stress [24]. The FWHM of the 2D peaks are 40 and 42 cm^{-1} for the Si- and C-face, respectively, consistent with single layer graphene [13]. Fig. 5.1(a) is an STM image of graphene transferred on the Si-SiC, and further annealed at ~300 ^{o}C in UHV for 30 min. Clearly evident are graphene ridges 2.5 nm in height, 7 nm in width, and hundreds of nm in length, likely originated from the CVD growth [20], and preserved during the transfer process. Additional smaller spatial fluctuations (i.e. ripples) are also observed, similar to earlier work [21, 25]. Fig. 5.1(b) is a close-up view of a ripple, showing that the honeycomb lattice is continuous throughout the corrugations. This indicates that ripples are the buckled-up region of the same graphene layer [26]. A line profile taken along the dashed line indicates a step height of 1.8 nm, corresponding to ~ 6 Si-C bilayer, on top of which an average ripple height of 0.34 nm is seen [Fig. 5.1(a) inset]. Graphene is also continuous over SiC steps [Fig. 5.1(a)]. Overall, ripples, ridges, and SiC steps are the three main types of intrinsic spatial inhomogeneities that can exist at the graphene/SiC junctions.

The electronic properties of graphene/Si-SiC are further investigated by STS. The inset in Fig. 5.1(b) is a dI/dV spectrum taken at the flat region, which exhibits two characteristic minima, one at zero bias (E_F) caused by phonon assisted inelastic tunneling [27], and the other at +0.22 eV

attributed to the Dirac point (E_D). The position of E_D with respect to E_F indicates p-type doping in graphene [13], which is further confirmed by Hall measurements. These results are consistent with the H-intercalated epitaxial graphene on SiC (0001) [28-30], confirming that the H_2/Ar processing indeed leads to H-terminated SiC. Hall measurements indicate a mobility of 27,500 cm^2/Vs, much higher than those on SiO_2 [31] and closer to that on BN substrates [32], likely a result of the atomically flat H-terminated SiC surfaces.

Fluctuations in Dirac energy between 205 to 315 meV are also found in spatially resolved dI/dV measurements. Spectra taken across a ripple at locations 1-13 marked in Fig. 5.1(c) are shown in Fig. 5.1(d). While all spectra exhibit the two characteristics minima E_F and E_D, fluctuations in the Dirac point are clearly seen (marked by vertical arrows), consistent with our earlier work [13]. By calculating the normal probability distribution, a mean value of 270 meV in Dirac energy with FWHM of 70 meV are obtained [inset Fig. 5.1(d)].

Atop the brightest region (spectrum 5-7), an additional peak at ~ 0.44 eV is also observed, possibly due to charged impurity trapped underneath graphene. The annealing of the H-terminated SiC substrates at 600 ^oC prior to graphene transfer likely causes partial desorption of hydrogen from the SiC surface, and the resulting Si dangling bonds may introduce additional states. However, the overall graphene morphology and electronic properties is not altered. Similar measurements were done for graphene/C-SiC without the annealing at 600^oC, where graphene is found to be n-type with a Dirac point at 0.42 eV below E_F and FWHM of 42 meV [13].

5.2.2 I-V measurements on graphene/SiC junction

Temperature dependent I-V measurements are carried out on the processed devices. At 310 K, both graphene/C-SiC and Si-SiC junctions show rectifying behaviors [Fig.5.2 (a)], suggesting the formation of Schottky diodes. A greater forward current for graphene/Si-SiC indicates a smaller

SBH. I-V spectra taken for graphene/C-SiC Schottky junction at 250-340 K are shown in Fig.5.2(b) (lower temperature measurements are not shown due to carrier freeze-out in SiC [5, 22]). Increase in forward bias current with increasing temperature [Fig.5.2(b) inset] suggests thermally excited transport across the junction. Similar temperature dependent behavior is also observed for graphene/Si-SiC junction.

The current across a metal/semiconductor Schottky junction can be written by TE theory as

$$I = I_S \left[exp\left(\frac{qV}{\eta kT}\right) - 1 \right] \quad [5.1]$$

where I_S is the saturation current density, T the temperature, k the Boltzmann constant and η the ideality factor. The zero-bias SBH ϕ_{B0} can be obtained from the extrapolation of I_S in the semi-log forward bias $ln(I) - V$

$$\phi_{B0} = \frac{\eta kT}{q} ln\left(\frac{AA^*T^2}{I_S}\right) \quad [5.2]$$

where A is the diode area, and $A^*$the Richardson constant. The ideality factor is a dimensionless parameter that accounts for the deviation from TE theory ($\eta = 1$ for ideal junction), and can be calculated from the slope of the linear region of the forward *I-V*

$$\eta = \frac{q}{kT}\frac{dV}{d(ln\, I)} \quad [5.3]$$

The $ln(I) - V$ characteristics at 310 K for graphene/C-SiC and graphene/Si-SiC junctions are shown in Fig. 5.3 (a). A linear region is observed in low bias region (from 0.1 to 0.4 V) where TE model is applied to obtain junction parameters. However, non-linearity in high voltage region 0.5-1.2 V is attributed to the contribution of other processes such series resistance. In this voltage range, series resistance is estimated to be 7 K-ohm at 300 K for both graphene/SiC junctions. Next, Richardson method is used to obtain temperature independent barrier height from the slope of

linear region of $ln(I_S/T^2)$ versus $1000/T$ plot. However, a non-linear [scattered data points as shown in Fig. 5.3 (b)] Richardson plot is observed for graphene/SiC suggesting temperature dependent barrier height. The temperature dependent zero bias SBH and ideality factor are calculated using Equation [5.2] and [5.3], with a diode area of 1.96 mm^2 and Richardson constant $A^* = 1.46\times10^6$A m^{-2} K^{-2} for n type 4H-SiC, and shown in Fig. 5.3(c). From 250 to 340 K, the barrier height increases from 0.57 to 0.79 eV, and the ideality factor decreases from 5.40 to 4.16 for the graphene/C-SiC Schottky junction. A similar trend is also seen for the graphene/Si-SiC junctions with a larger overall ideality factor, and smaller barrier height.

5.3 Discussion

The TE theory assumes a perfect homogeneous junction interface and a single SBH, however, our STM/STS results clearly indicate spatial inhomogeneity in graphene that cause fluctuations in E_D. Hence here instead of calculating SBHs based on the simple Richardson plot as was done in most recent studies [5, 15, 16], we apply the Werner's model that relates the mean (ϕ_{bm}) and apparent (ϕ_{B0}) barrier height as follows

$$\phi_{B0} = \phi_{bm}(T = 0) - \frac{q\sigma_S^2}{2kT} \qquad [5.4]$$

This is based on the assumption of a Gaussian distribution of the barrier height, where the apparent barrier height is the experimentally measured values of ϕ_{B0}, and σ_S is the standard deviation with a lower value indicating a more homogeneous barrier.

The apparent barrier height ϕ_{B0} as a function of $q/2kT$ is shown in Fig. 5.4 (a). The mean barrier height and standard deviation as determined from the slope and intercept are $\phi_{bm} = 1.30\ eV$ and $\sigma_S = 1.18\ eV$ for graphene/C-SiC junction over the temperature range of 250-340 K. The standard deviation of 14% suggests a large interface inhomogeneity. Similar analysis for the

graphene/Si-SiC junction yields a mean barrier height of 1.16 eV with a standard deviation of 0.16 eV. Alternatively, the influence of spatial inhomogeneities can be considered by calculating the flat band barrier height (zero electric field in semiconductor), which is an intrinsic parameter given by [33]

$$\phi_{bf} = \eta\phi_{B0} - (\eta - 1)\left(\frac{kT}{q}\right) ln\left(\frac{N_C}{N_d}\right) \quad [5.5]$$

where N_C is the effective density of states in the conduction band and N_d is the donor concentration. Fig.5.4 (b) shows the variation of ϕ_{bf} as a function of temperature for graphene/Si-SiC and graphene/C-SiC. Linear fitting using

$$\phi_{bf} = \phi_{bf}(0) + \alpha T \quad [5.6]$$

leads to $\phi_{bf}(0)$ of 3.20 and 2.38 eV with corresponding α of 1.27×10^{-3} and 1.39×10^{-3} eVK^{-1} for graphene/Si-SiC and graphene/C-SiC, respectively. Where $\phi_{bf}(0)$ and α are the flat band barrier height extrapolated to the absolute zero and the temperature coefficient of the flat band barrier height, respectively. It is found that ϕ_{bf} is always larger than ϕ_{B0}, but unlike ϕ_{B0}, it appears to be nearly constant over the whole range of temperature (250- 340 K) with a slight variation around the average value of 3.57 eV and 2.78 eV for graphene/Si-SiC and graphene/C-SiC, respectively and this behavior is similar to the previous studies on normal metal-semiconductor junctions [34]. In addition, Equation [5.5] provides a relationship between the measured zero bias barrier height ϕ_{B0} and ideality factorη. Under the assumption of bias independent ideality factor with values larger than one, this relationship takes a linear form as explained by Werner *et al*. [36] and shown by Schmitsdrof *et al.* [34]. The zero bias barrier height as a function of ideality factor is shown in Fig. 5.4(c) for both the junctions. Extrapolation of the barrier height at unity ideality factor leads to the lateral homogeneous barrier height of 1.29 and 1.22 eV for graphene/C-SiC and graphene/Si-SiC junctions, respectively, similar to earlier studies of Ag/Si (111) Schottky junctions [35]. These

SBH values are also in excellent agreement with the mean SBH values obtained from the temperature dependent apparent barrier height in Fig. 5.4(a), indicating that transport across the graphene/SiC Schottky junctions is consistent with a modified thermionic emission with a Gaussian distribution of barrier heights.

In summary, monolayer graphene/SiC Schottky junctions are studied using STM/STS and temperature dependent I-V measurements. Deviations from ideal behavior are explained by barrier height variations present at the interface, caused by intrinsic spatial inhomogeneities such as graphene ridges and ripples, and SiC substrate steps. Our findings reveal the critical role of the spatial fluctuations in the intrinsic Schottky barrier height, and is directly applicable to other 2D materials/semiconductor Schottky junctions.

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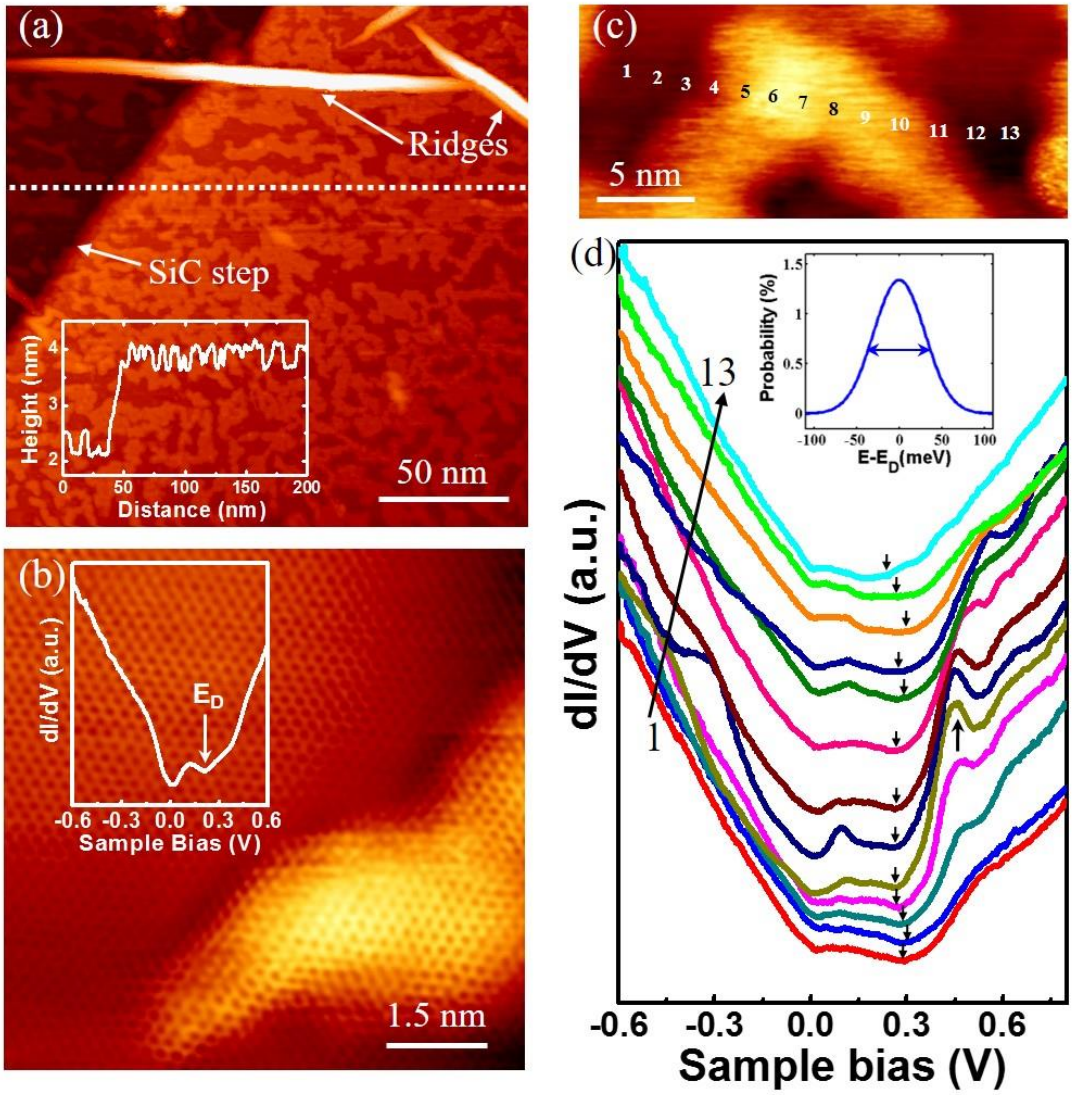

Figure 5.1: (a) STM image of graphene transferred on Si-SiC substrate annealed at 600 ^{0}C (I_t = 0.1 nA, Vs = -0.75 V). Inset shows a line profile taken along the dashed line. (b) Atomic resolution STM image of graphene ripples (I_t = 0.2 nA, V_s = -0.2 V). Inset: dI/dV spectra taken at a flat region. (c) STM image of a ripple where (d) spatially resolved dI/dV spectra are taken. Inset: normal probability distribution of Dirac energy

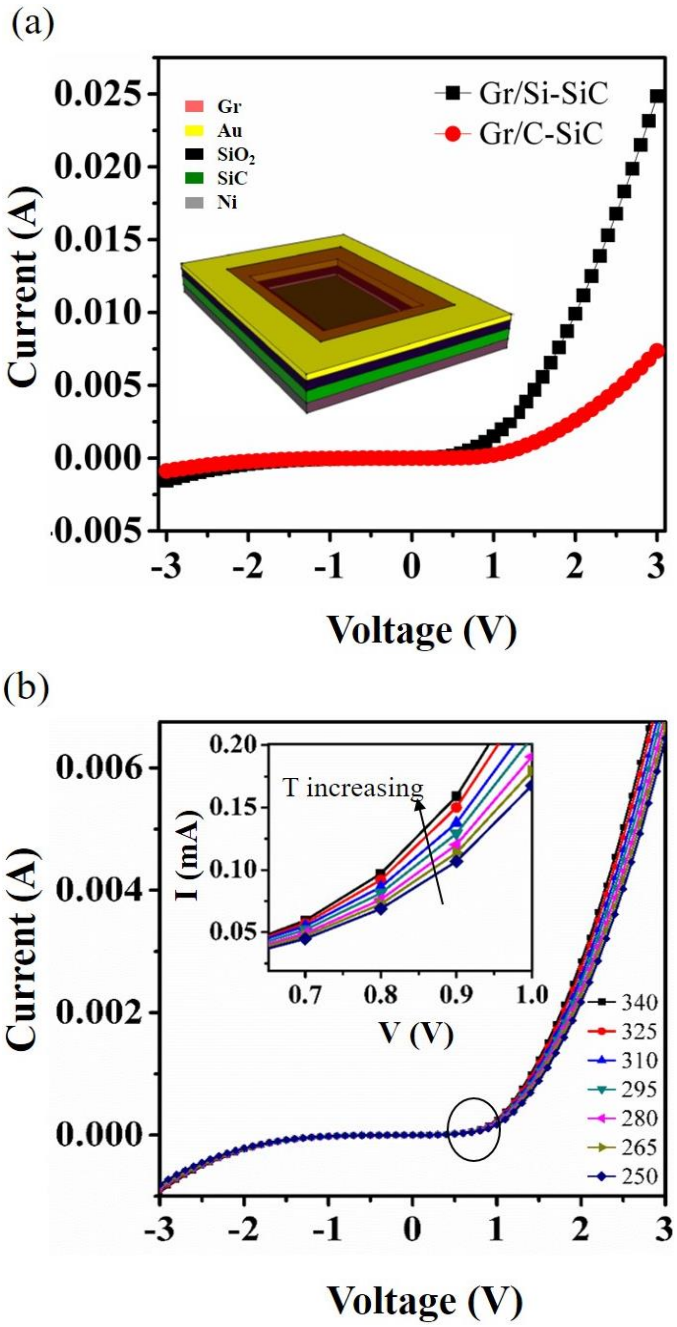

Figure 5.2: (a) Rectifying I-V characteristics of graphene/C-SiC and graphene/Si-SiC Schottky junctions at 310 K (Inset shows device schematic diagram). (b) Temperature dependent I-V curves of graphene/C-SiC Schottky junction from 250-340 K (inset shows the close-up view of forward bias current).

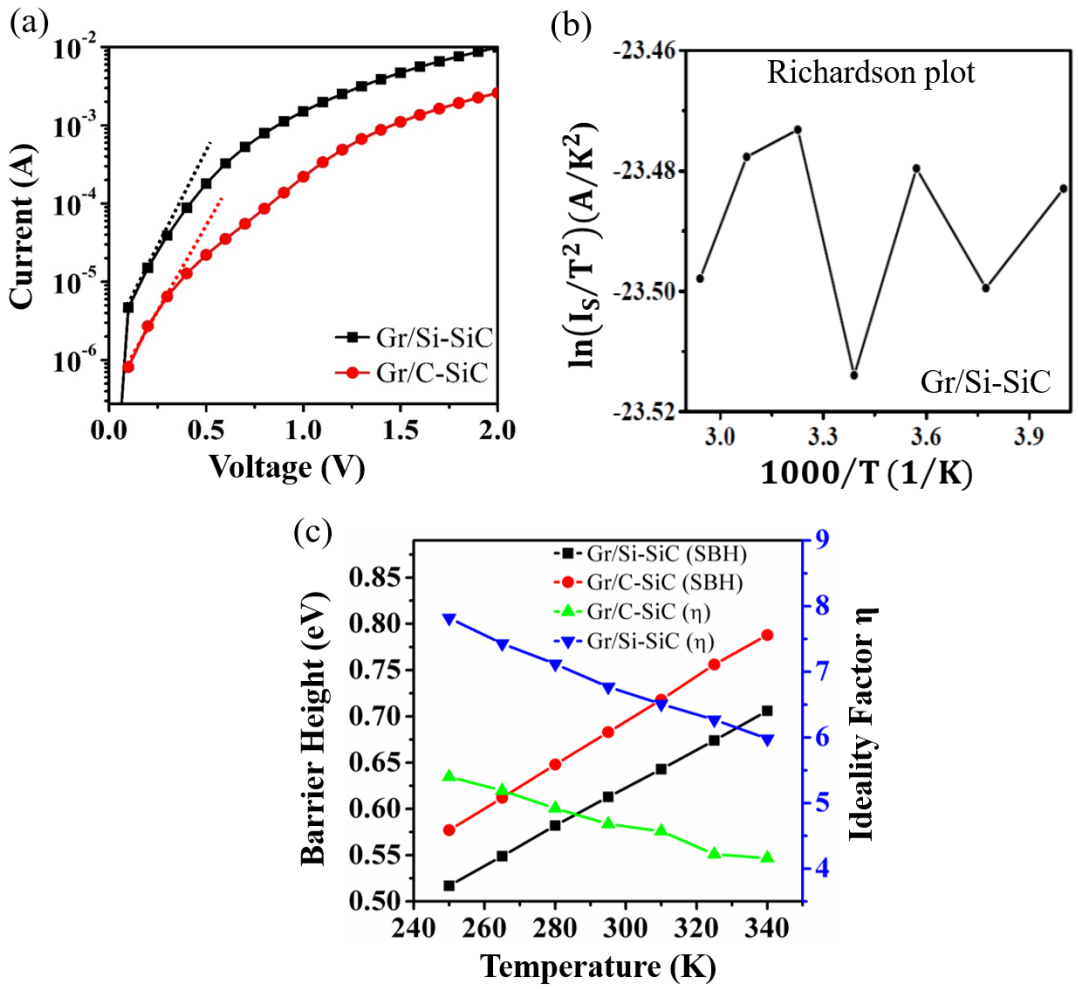

Figure 5.3: (a) Semi logarithmic I-V for graphene/SiC junctions at 310 K. (straight lines represent fits to the linear regions). (b) Non-linear Richardson plot for graphene/Si-SiC Schottky junction. (c) Barrier height and ideality factor as a function of temperature for graphene/SiC Schottky junctions.

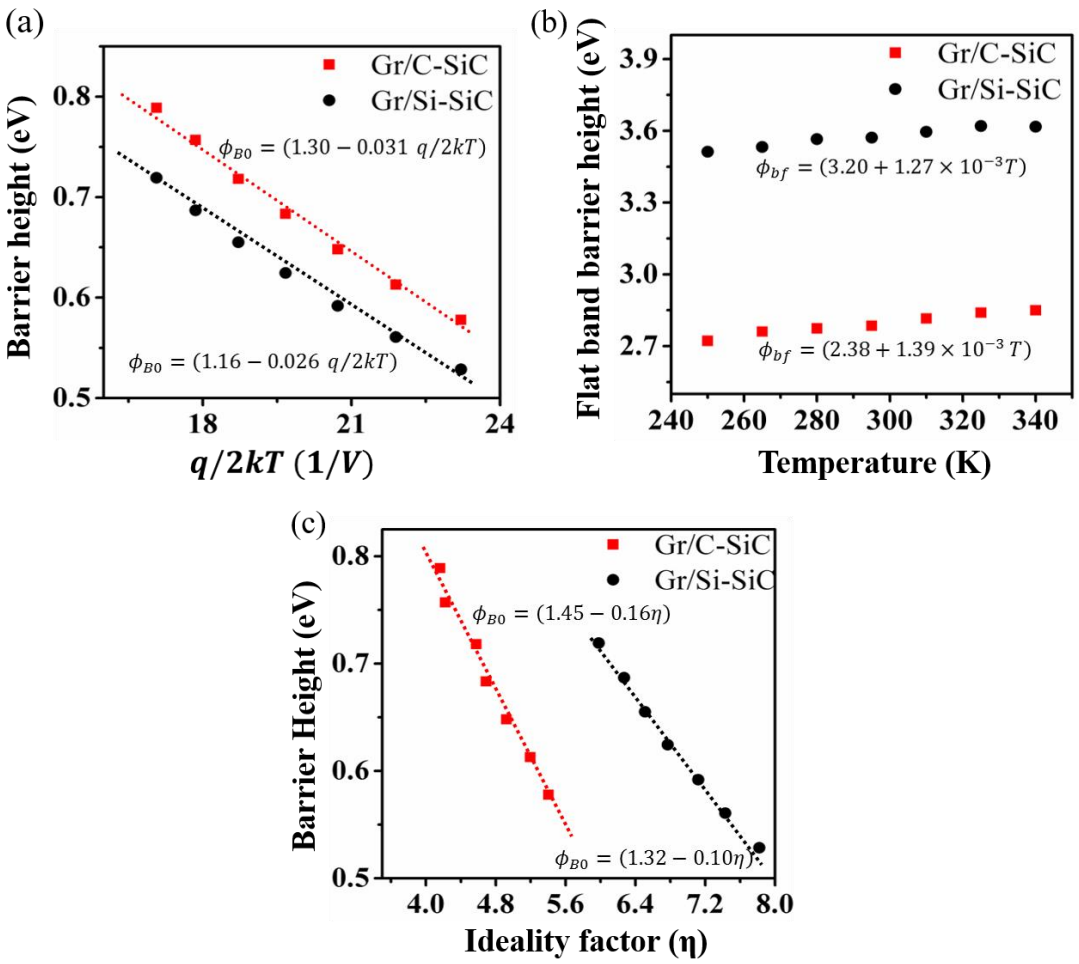

Figure 5.4: (a) ϕ_{B0} versus $q/2kT$ and (b) flat band barrier height ϕ_{Bf} versus T for graphene/SiC junctions in temperature range 250-340 K. (c) Zero-bias barrier height as a function of ideality factor for same junctions.

Chapter 6
Inhomogeneity in barrier height at graphene/Si (GaAs) Schottky junctions

6.1 Introduction

In chapter 5, graphene/SiC Schottky junctions were investigated by using STM/S and temperature dependent I-V measurements. In such junctions, a temperature dependence of SBH and ideality factor was observed and attributed to intrinsic interface inhomogeneities [1]. In the absence of interface states in hydrogen passivated SiC substrates, the electronic properties were found directly correlated to interface topographic corrugations which come from graphene ripples, ridges and SiC steps as revealed by STM/S [2]. However, such assumption would not be valid for the semiconductors which are more prone to form thin oxide layer even after proper cleaning e.g. Si and GaAs. Similar to SiC case, graphene Schottky junctions with Si and GaAs have also been demonstrated in various electronic, optoelectronic and sensing applications [3-8]. However, the effect of interface inhomogeneities on junction parameters and conduction mechanism is not addressed, especially in presence of interface states.

In this chapter, the effect of both types of inhomogeneities (intrinsic due to graphene ripples and ridges, and extrinsic coming from interface states) on the electrical properties of graphene/Si and graphene/GaAs Schottky junctions is investigated by using STM/S and temperature dependent I-V measurements. Similar to graphene/SiC junctions, the observed increment in SBH and decrement in ideality factor with increasing temperature is attributed to the inhomogeneous interface. However, in contrast to SiC, no direct correlation to topographic variations is found for graphene Schottky junctions with Si and GaAs.

6.2 Results

The Schottky junctions are fabricated by transferring chemical vapor deposited (CVD) graphene onto n-type Si (111) and GaAs (100) with carrier densities Nd ~ 10^{17} cm^{-3} and ~10^{16} cm^{-3}, respectively. Detailed information about substrate preparation and device fabrication is given in chapter 4. T dependent I-V measurements are carried out using a Keithley 2400 source meter between 215 and 350 K. STM/STS is carried out at liquid nitrogen temperature. The dI/dV tunneling spectra are acquired using lock-in detection by turning off the feedback loop and applying an AC modulation of 9 mV (r.m.s.) at 860 Hz to the bias voltage.

6.2.1 STM/STS on graphene/Si and graphene/GaAs junctions

The surface morphology of transferred graphene is first characterized by STM. Fig. 6.1(a) shows an image of graphene/Si substrate after annealing at ~300^{o}C in UHV for 30 min. Clearly evident is a non-uniform surface with vertical undulations of ~0.5 nm over length scales of tens of nanometers (marked by a circle), likely due to roughness of the underlying Si substrate. Fig. 6.1(b) is a close-up view showing the characteristic graphene honeycomb lattice that is continuous over these fluctuations. These features are similar to earlier STM studies of graphene ripples [9,10], which are attributed to either graphene in contact with the underlying substrate (dark regions), or buckled up from it (bright regions).

The electronic properties of the graphene are further investigated by tunneling spectroscopy. Fig. 6.1(c) shows spatially resolved dI/dV spectra taken across a ripple at locations marked in Fig. 6.1(b) for graphene/Si. All spectra exhibit two characteristic minima, one at zero bias (E_F) caused by phonon-assisted inelastic tunneling [11], and the other at negative bias marked by downward arrows attributed to the Dirac point (E_D), indicating n-type doping [12]. Moving from bright to dark to bright regions [Fig. 6.1(c)], while E_D varies between 105 and 130 meV, no

direct correlation is found to the topographic fluctuations, in contrast to the case of graphene transferred on SiC substrates [1,2]. In addition, atop the brightest regions (spectra 1-3 and 7, 8) peaks also appear, as marked by upward arrows, possibly due to states arising from disorder from the partial hydrogen termination of the Si substrate [13].

Similar features are observed for graphene/GaAs as shown in Fig. 6.2(a). Large scale corrugations of ~ 1 nm in height and hundreds of nm in width likely originated from substrate roughness. At the atomic scale, ripples ~ 0.35 nm in height are also seen (Fig. 6.2(b)). A series of dI/dV spectra, taken at positions 1-11 in Fig. 6.2(b), are shown in Fig. 6.2(c). While all spectra exhibit the similar phonon-assisted inelastic tunneling [11] at E_F, the Dirac point (marked by downward arrows) is now above E_F, indicative of p-type doping. Again, fluctuations in Dirac energy between 110 and 160 meV are also observed, but with no direct correlation is found with the undulation of the ripples. Likely substrate disorder induced states peaked at ~0.24 eV are again observed at some locations (spectra 1-3, 5).

The local fluctuations in the Dirac point lead to variation in carrier concentration ($\Delta n(p)$) that can be calculated by $\Delta n(p) = \frac{4\pi(\Delta E_D)^2}{(hv_f)^2}$, where v_f is the Fermi velocity of graphene (~ c/300, where c is the speed of light) and *h* the Plank's constant. This yields variations of 3.79×10^{10} cm^{-2} and 1.57×10^{11} cm^{-2} in electron and hole concentrations for graphene/Si and graphene/GaAs junctions, respectively.

These observations clearly indicate that graphene is prone to ripple formation when interfaced with Si and GaAs substrates, similar to CVD graphene transferred on hydrogen-terminated SiC substrates [1, 2 and exfoliated graphene on SiO_2 [10]. Interestingly, unlike the graphene/SiC junctions, the spatial variations in E_D for both junctions do not follow the topographic fluctuations [1, 2]. The local carrier fluctuations due to Dirac point variation

nevertheless results in electron and hole puddles, similar to that of graphene / SiO_2 [10]. As discussed below, this inherent spatial inhomogeneity in graphene can lead to fluctuations in the SBH determined by the temperature dependent I-V measurements.

6.2.2 I-V measurements on graphene/Si and graphene/GaAs junctions

Between 215 and 350 K, both graphene/Si and graphene/GaAs junctions show rectifying I-V, as shown in Fig. 6.3(a) and (b), respectively, suggesting the formation of Schottky diodes. The thermally excited transport across the junction follows the TE model [14]

$$I(T,V) = I_S(T)\left[exp\left(\frac{qV}{\eta kT}\right) - 1\right] \quad [6.1]$$

where V is the applied voltage, q the electron charge, k the Boltzmann's constant, and η the ideality factor. The saturation current, $I_s\ (T)$, can be expressed as [14]

$$I_S(T) = AA^*T^2 exp\left(\frac{-q\phi_{B0}}{kT}\right) \quad [6.2]$$

where A is the diode area, A* the effective Richardson constant of the semiconductor, and ϕ_{B0} the zero bias SBH, which can be obtained from the extrapolation of $I_S(T)$ in the semi-log forward bias $ln(I) - V$

$$\phi_{B0}(T) = \frac{kT}{q} ln\left(\frac{AA^*T^2}{I_S}\right) \quad [6.3]$$

The ideality factor is a dimensionless parameter that accounts for any deviation from the standard TE theory ($\eta = 1$ for an ideal junction), and can be calculated from the slope of the linear region of the forward $ln(I) - V$

$$\eta = \frac{q}{kT}\left(\frac{dV}{d(lnI)}\right) \quad [6.4]$$

Temperature dependent forward bias $ln(I) - V$ plots of graphene/Si and graphene/GaAs junctions are shown in Fig. 6.4(a) and (b), respectively. At low bias voltages, both are linear over ~3-4 orders of current, and the deviation from the linearity is likely due to large series resistance [15] in both

types of junctions. Fig. 6.5(a) shows the temperature dependence of ϕ_{B0} and η, calculated using equations [6.3] & [6.4], with a total diode area of 1.62 mm^2 (=2×0.9×0.9 mm^2), and Richardson constant of 1.12×10^6 Am^{-2} K^{-2} and 0.41×10^4Am^{-2}K^{-2} for n-Si [16] and n-GaAs [17], respectively. For graphene/Si, ϕ_{B0} increases from 0.66 to 0.82 eV and η decreases from 2.62 to 1.66 from 215 to 350 K. A similar trend is also seen for graphene/GaAs, where ϕ_{B0} changes from 0.48 to 0.62 eV and η varies from 1.88 to 1.44. This temperature dependence clearly deviates from the ideal TE theory, suggesting barrier inhomogeneities [18-20].

This is further supported by the analysis of the Richardson plot, $ln(I_S/T^2)\ versus\ 1000/T$ [Fig. 6.5(b)]. The deviation from the linearity below 275K indicates temperature dependent barrier height for both junctions. Linear fitting of the data above ~275 K (dashed line) yields SBH of 0.47 and 0.36 eV, and A^* of 1.04×10^1 and 8.72×10^{-1} Am^{-2}K^{-2} for Si and GaAs, respectively. The large deviation of A^* from the known experimental values of 1.12×10^6 Am^{-2}K^{-2} for Si and 0.41×10^4 Am^{-2}K^{-2} for GaAs clearly indicates inhomogeneous SBHs due to potential fluctuations at the interface [21].

6.3 Discussion

Assuming a Gaussian distribution of the barrier height, the deviation from ideal TE theory can be explained by the Werner model [22] that correlates the mean (ϕ_{bm}) and apparent (ϕ_{B0}) barrier height as follows

$$\phi_{B0}(T) = \phi_{bm} - \frac{q\sigma_S^2}{2kT} \qquad [6.5]$$

where σ_S is the standard deviation. Fig. 6.6 (a) shows the plot of $\phi_{B0}(T)$ as a function of $q/2kT$ which yields a mean barrier height of 1.104 eV and σ_S = 141 mV for graphene/Si, and 0.76 eV and σ_S =98 mV for graphene/GaAs.

The modified Richardson plot,[$ln(I_S/T^2) - q^2\sigma_S^2/2k^2T^2]$ vs $1000/T$, is shown in Fig. 6.6 (b). Since

$$ln\left(\frac{I_S}{T^2}\right) - \left(\frac{q^2\sigma_S^2}{2k^2T^2}\right) = ln(AA^*) - \frac{q\phi_{bm}}{kT} \quad [6.6]$$

this plot should be a straight line with the mean barrier height (ϕ_{bm}) determined by slope and y-intercept [$ln(AA^*)$] that would directly yield A*. The mean barrier height is found to be 1.15 eV for graphene/Si and 0.74 eV for graphene/GaAs, with corresponding Richardson constants of 1.14×10^6 and 0.27×10^4 A $m^{-2}K^{-2}$, respectively, in much better agreement with previously defines values.

Alternately, the barrier inhomogeneities can be considered by calculating the flat band barrier height ϕ_{bf}, an intrinsic parameter given by [23]

$$\phi_{bf} = \eta\phi_{B0} - (\eta - 1)\zeta \quad [6.7]$$

where $\zeta = (kT/q)ln(N_C/N_d)$, and $N_C = 2(2\pi m^* kT/h^2)^{3/2}$is the effective density of states, and N_d the donor concentration. Fig. 6.7(a) & 6.7(b) show ϕ_{bf} as a function of temperature, where the dashed line is a linear fit with

$$\phi_{bf}(T) = \phi_{bf}(0) + \alpha T \quad [6.8]$$

where $\phi_{bf}(0)$ is the zero-temperature flat band barrier height and α the temperature coefficient. This yields $\phi_{bf}(0)$ of 1.54 and 0.86 eV with α = 6.48×10^{-4} and 1.09×10^{-4} eV K^{-1} for graphene/Si and graphene/GaAs, respectively. Clearly, the flat band barrier heights $\phi_{bf}(0)$ are not only always greater than the zero bias values ϕ_{B0} but are also with a weak temperature dependence.

In addition, equation [6.7] also correlates the measured zero bias SBH ϕ_{B0} and ideality factorη. For homogeneous junction,$\eta = 1$, thus $\phi_{bf} = \phi_{B0}$. For inhomogeneous junctions, η is always greater than one. In the current case, since the magnitude of ϕ_{B0} is more than 10× greater than ζ for graphene/Si and ~5× greater for graphene/GaAs junctions, the term $\eta\phi_{B0}$ is much larger

than $\zeta(\eta - 1)$, hence $\phi_{B0} \sim \phi_{bf}/\eta$. Two conclusions can be drawn. First, the flat band barrier height ϕ_{bf} is always greater than the zero bias value ϕ_{B0} since η is greater than one, consistent with experimental data. Second, in the limits when η is small (or large), e.g., < 2.6, a linear relationship (with a negative slope) between ϕ_{B0} and η can be approximated.

Indeed, as shown in Fig. 6.8, a linear relationship provides an excellent fit for the plot of the zero bias barrier heights as a function of ideality factor, similar to earlier studies of graphene/SiC [1] and Ag/Si [24] Schottky junctions. Extrapolation of the barrier height at the unity ideality factor leads to barrier heights of 0.98 eV and 0.72 eV for graphene/Si and graphene/GaAs junctions, respectively. These values are in good agreement with the mean SBH values obtained from the temperature dependent apparent barrier heights in Fig. 6.6(a) and modified Richardson plot in Fig. 6.6(b), confirming that transport across the graphene/Si and graphene/GaAs Schottky junctions is consistent with modified thermionic emission with a Gaussian distribution of barrier heights.

In summary, graphene/Si and graphene/GaAs Schottky junctions are investigated using atomic resolution STM imaging, dI/dV tunneling spectroscopy, and temperature dependent I-V measurements. The temperature dependent zero bias barrier height and ideality factor show clear deviations from the standard thermionic emission theory, which is explained by barrier height fluctuations caused by Dirac point inhomogeneities likely induced by semiconductor substrate disorder. Together with our earlier work on the graphene/SiC Schottky junctions, where Dirac point fluctuations correlate directly with topographical undulations of graphene ripples [11, 12], these findings reveal two types of intrinsic inhomogeneities that can cause barrier height fluctuations in graphene / semiconductor Schottky junctions. Which mechanism dominates will

depend on the nature of the semiconductor (e.g., polar vs non-polar), and/or the degree of disorder and roughness of the semiconductor surface.

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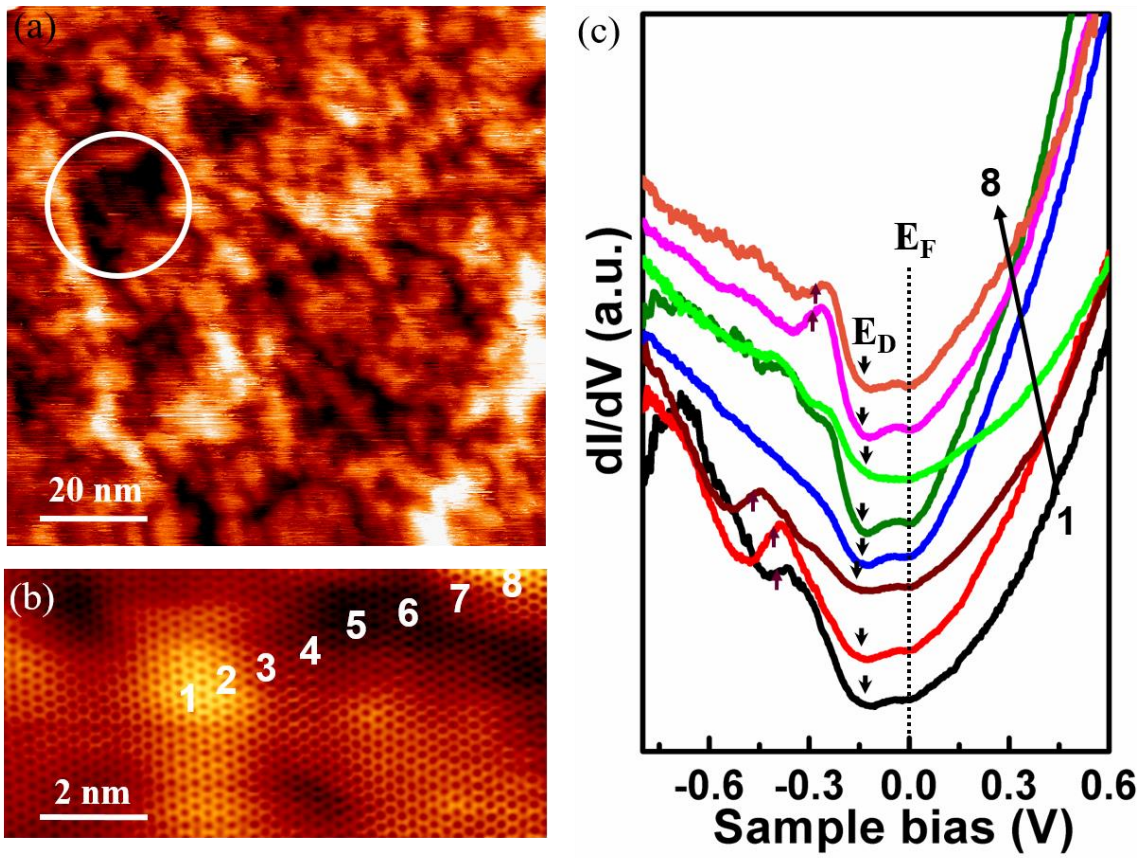

Figure 6.1: (a) STM image of CVD graphene transferred onto n-Si substrate (I_t = 0.1 nA, Vs = -0.65 V). (b) Atomic resolution STM image of graphene ripples (I_t = 0.1 nA, V_s = -0.3 V). (c) Spatially resolved dI/dV spectra taken at the locations marked in (b).

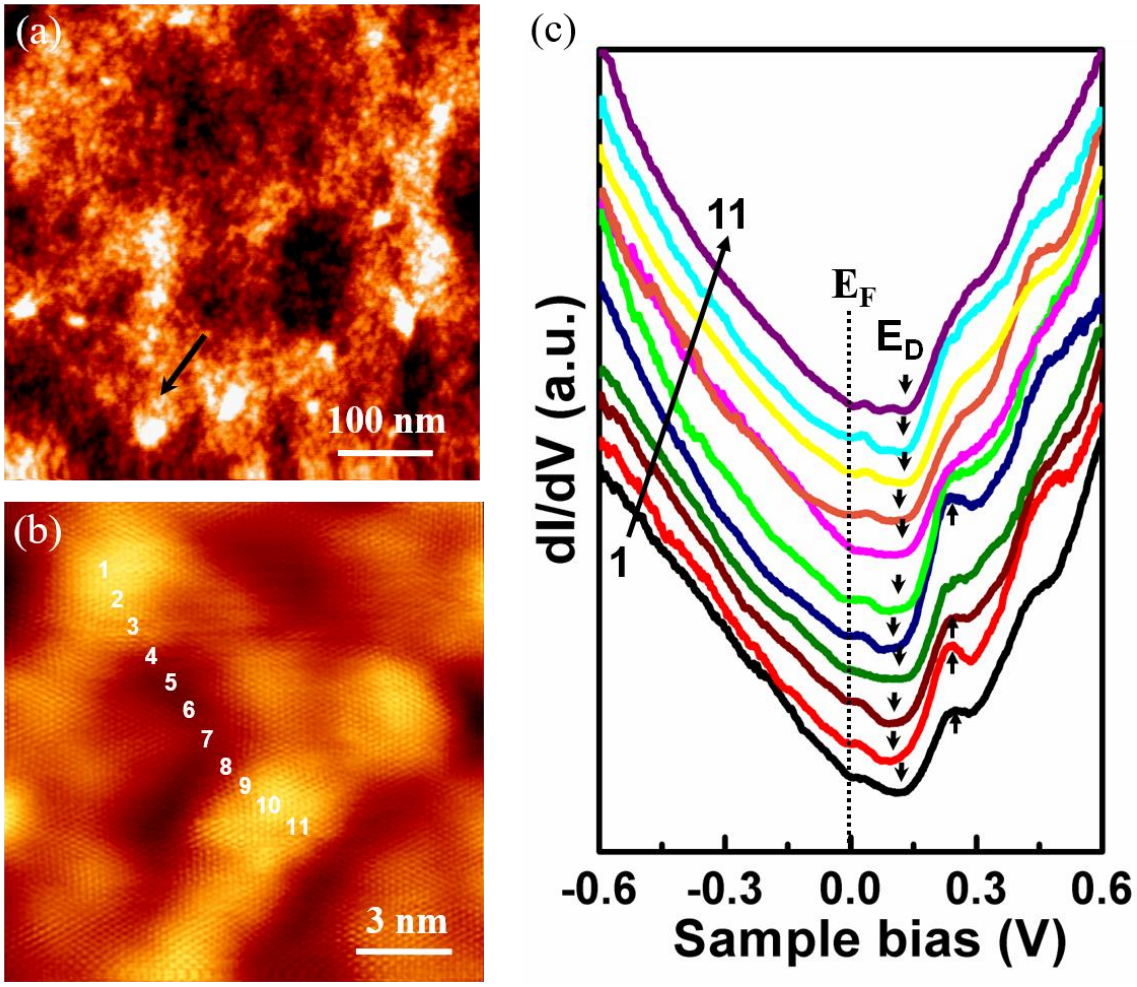

Figure 6.2: (a) STM image of CVD graphene transferred onto n-GaAs substrate (I_t = 0.1 nA, Vs = -0.3 V). (b) Atomic resolution STM image of graphene ripples (I_t = 0.2 nA, V_s = -0.3 V). (c) Spatially resolved dI/dV spectra taken at the locations marked in (b).

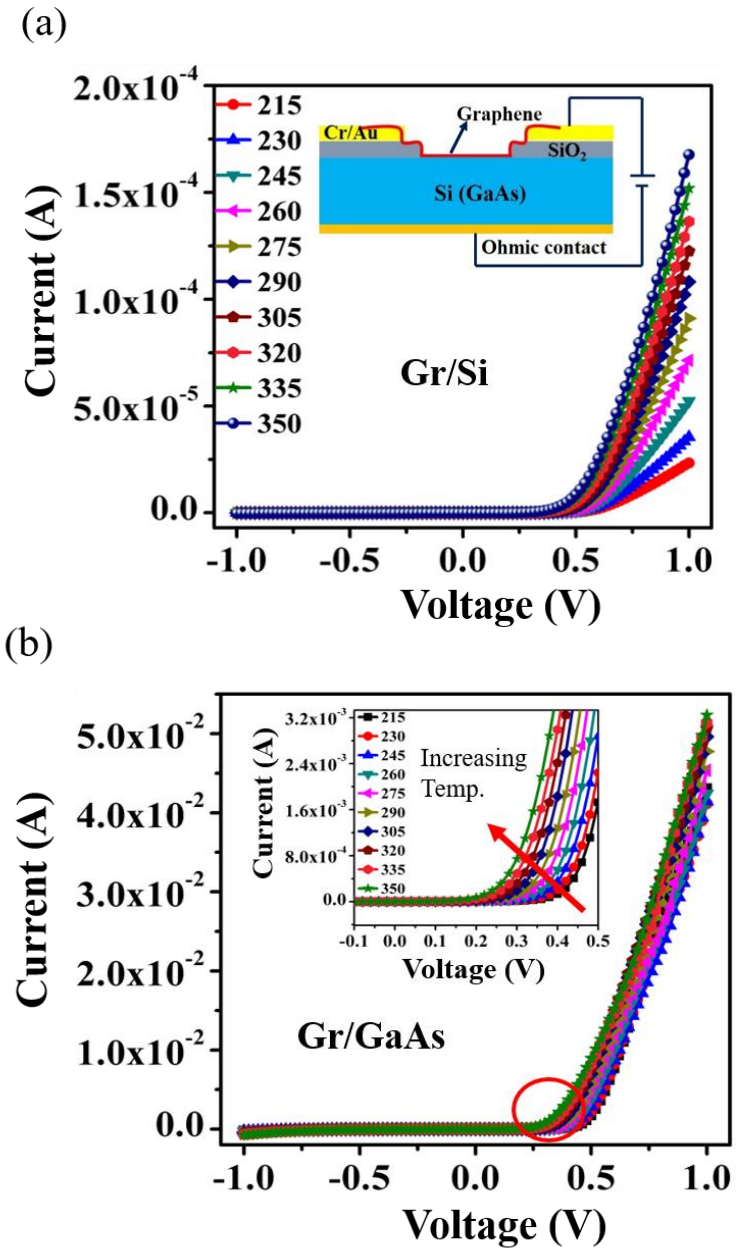

Figure 6.3: (a) Temperature dependent *I-V* curves of graphene/Si Schottky junction between 215 and 350 K (inset: schematic diagram of the device). (b) Temperature dependent *I-V* curves of graphene/GaAs Schottky junction (inset: close-up view of forward bias current).

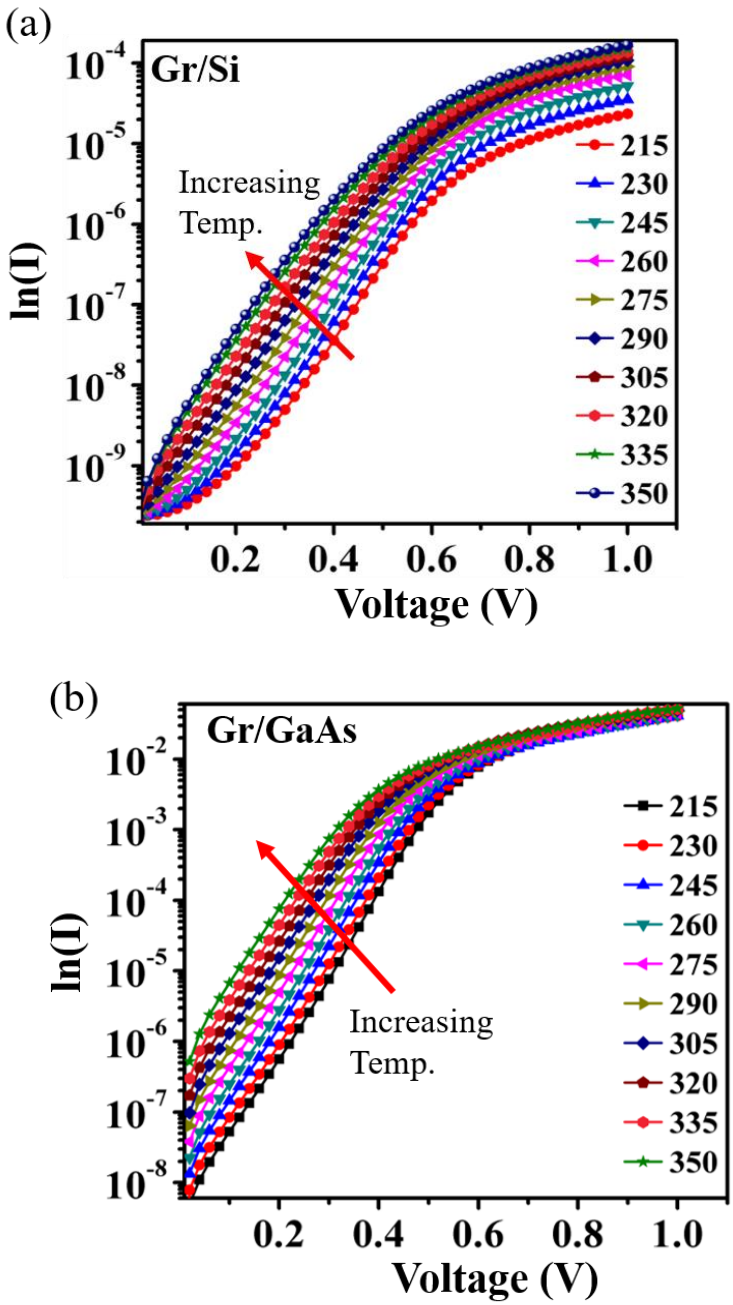

Figure 6.4: Temperature dependent semi-logarithmic forward bias *I-V* curves of (a) graphene/Si and (b) graphene/GaAs Schottky junctions, respectively.

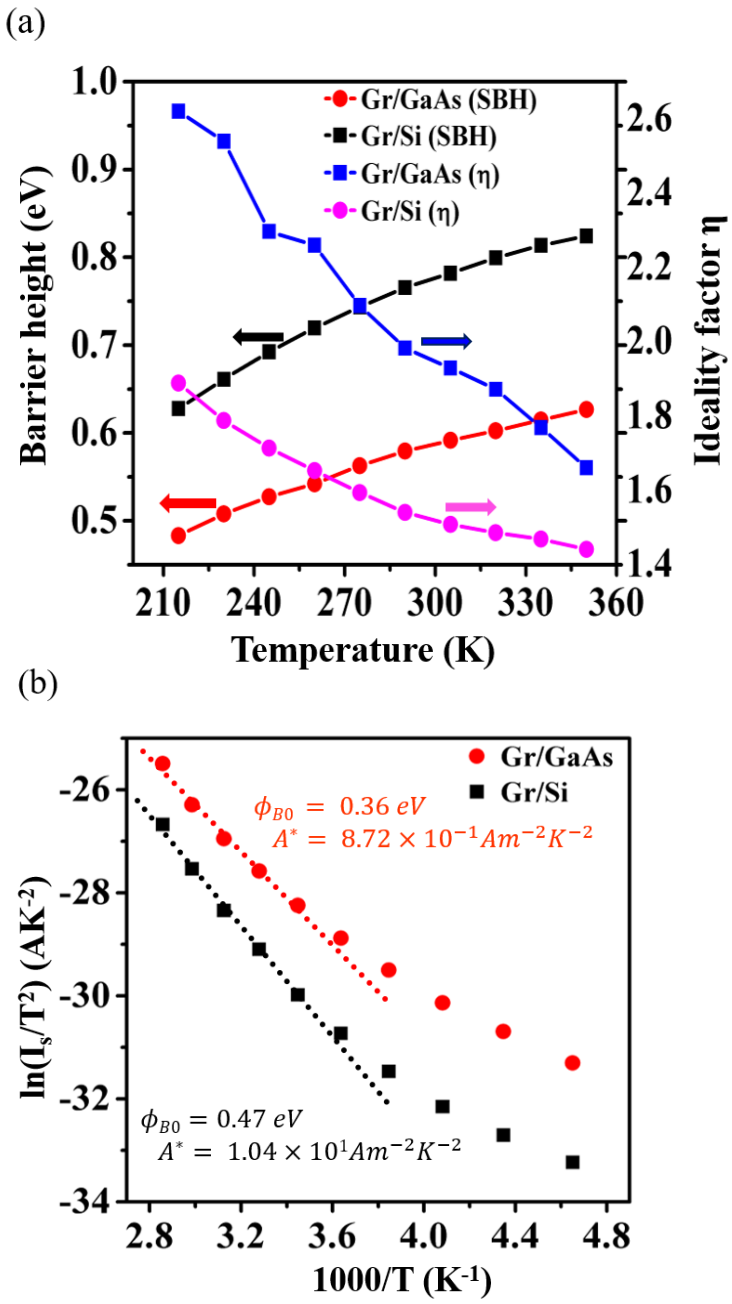

Figure 6.5: (a) Zero bias barrier height (ϕ_{B0}) and ideality factor (η) as a function of temperature for graphene/Si and graphene/GaAs Schottky junctions. (b) Richardson plot for graphene/Si and graphene/GaAs.

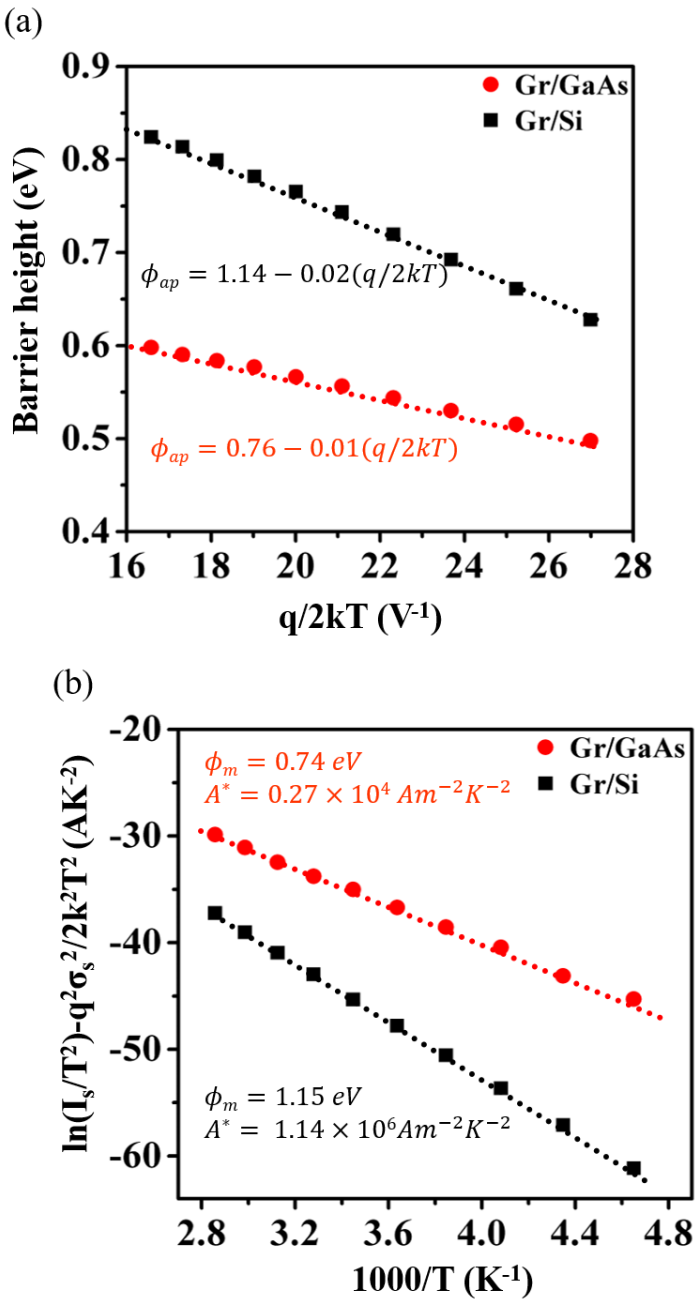

Figure 6.6: (a) Apparent zero bias barrier height ϕ_{ap} vs as a function of $q/2kT$ for graphene/Si and graphene/GaAs junctions. (b) Modified Richardson plot for the same junctions.

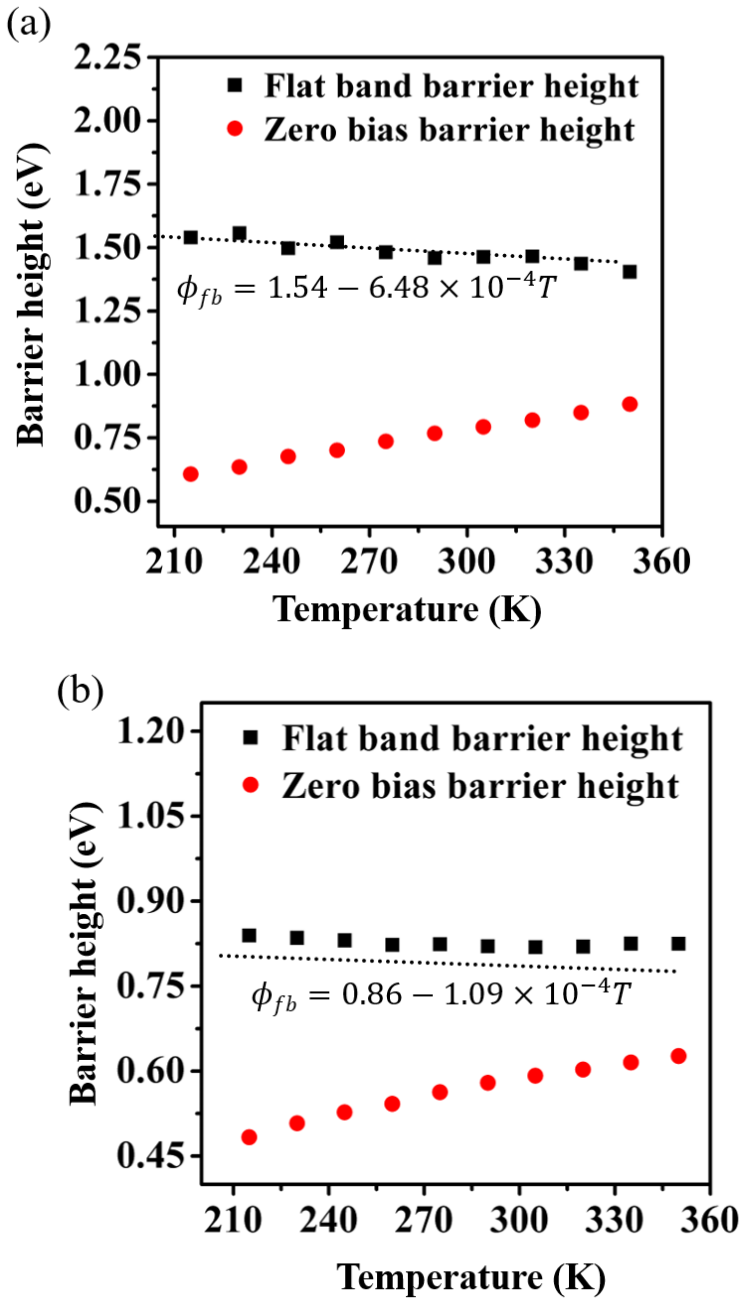

Figure 6.7: Flat band barrier height ϕ_{bf} as a function of temperature for (a) graphene/Si and (b) graphene/GaAs junctions.

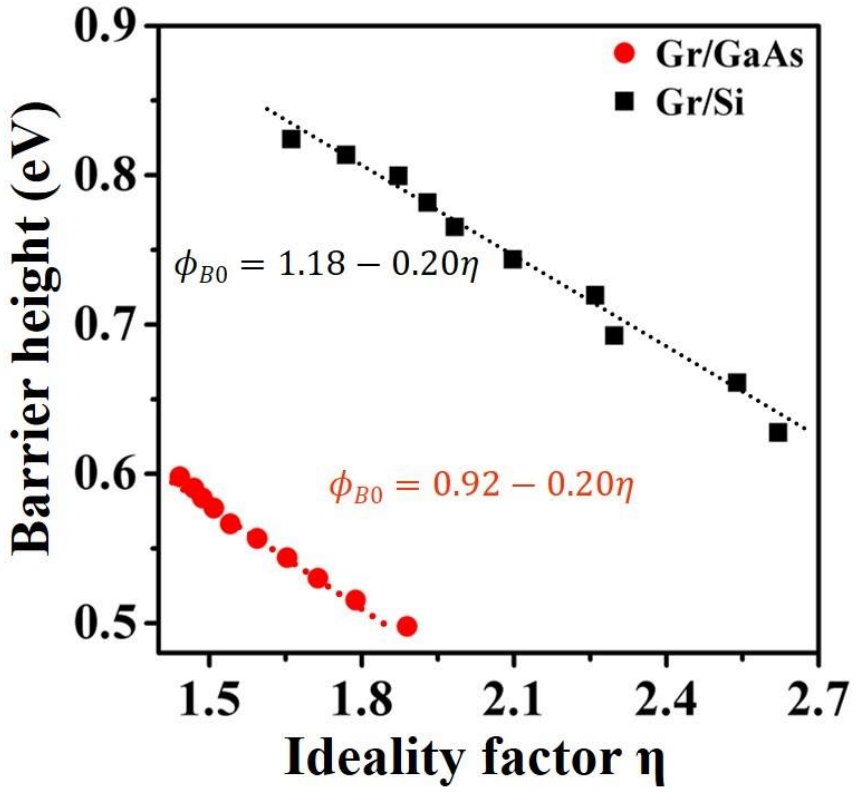

Figure 6.8: Zero-bias barrier height (ϕ_{B0}) as a function of ideality factor (η) for the same junctions.

Chapter 7
Spatial inhomogeneity in Schottky barrier height at graphene/MoS_2 Schottky junctions

7.1 Introduction

The effect of intrinsic and extrinsic inhomogeneities on characteristics parameters of graphene/3D semiconductors (SiC, Si and GaAs) Schottky junction has been discussed in chapter 5 and 6. From that work, it can be concluded that the presence of graphene ripples, ridges, substrate steps and interface states at junction interface leads to temperature dependent barrier height and ideality factors [1, 2]. Such behavior deteriorates the device performance, therefore must be avoided. One possible solution is to replace 3D conventional semiconductors with their 2D counterparts. Similar to 3D semiconductors, graphene/2D semiconductor Schottky diodes has also been used in various electronic, optoelectronic and flexible device applications [3-8]. It is the weak (van der Waals) inter-layer and strong (covalent) intra-layer bonding which makes them better candidate for graphene based Schottky junctions [9, 10]. Recently, the existence of ripple free graphene on top of 2D semiconductors is reported, attributed to the van der Waals interlayer bonding [11, 12]. Furthermore, the lack of unsaturated dangling bonds in 2D semiconductor allows to form an interface states free junction with graphene [12]. Nevertheless, there are few studies where a substantial carrier scattering and density fluctuation is observed in graphene/2D semiconductors heterostructures, which is attributed to local defects such as S vacancies [13]. Therefore, the actual picture at junction interface is not clear, which motivates us to explore graphene/MoS_2 junctions.

In this chapter, we fabricate graphene/MoS_2 Schottky junctions and investigate their atomic structures and transport properties by STM/STS and temperature dependent I-V measurements.

Several topographic deformations including atomic scale Moiré patterns, nanoscale graphene ridges, and ripples are observed, leading to a spatially inhomogeneous interface. The graphene/MoS_2 junctions exhibit rectifying I-V characteristics with an increase in zero bias SBH and decrease in ideality factor with increasing temperature, attributed to the spatial inhomogeneities present at the interface.

7.2 Results

To fabricate the graphene / MoS_2 Schottky junctions, multilayer MoS_2 flakes (~100 nm thick) are first exfoliated from MoS_2 bulk crystals (2D semiconductor Inc.) using thermal release tape under ambient conditions. They are then transferred onto hydrogen etched n-type 6H-SiC (0001) substrates. Electrodes are formed by ~50 nm gold (Au) deposited by electron beam evaporation (base pressure ~ 2×10^{-6} Torr) at room temperature. One Au electrode is deposited directly onto MoS_2, while the second one is isolated by ~ 60 nm Al_2O_3 layer. Finally, chemical vapor deposited monolayer graphene (Graphene Platform, Inc.) is transferred on MoS_2/SiC with pre-patterned electrodes using the well-established PMMA assisted method as described in chapter 3. These devices are annealed at 300^{o}C for 5 hours in an argon + hydrogen atmosphere to reduce polymer residues. The transfer of graphene is confirmed by atomic force microscopy (AFM) in ambient conditions, and scanning tunneling microscopy (STM) in ultra-high vacuum (UHV) with a base pressure of 1×10^{-10} Torr. dI/dV tunneling spectra are acquired at liquid nitrogen temperature using lock-in detection by turning off the feedback loop and applying an AC modulation of 12 mV (r.m.s.) at 860 Hz to the bias voltage. Temperature dependent $I-V$ measurements are carried out using a Keithley 2400 source meter between 210 and 300 K.

7.2.1 AFM/STM/STS Results

Prior to graphene transfer, the surface of exfoliated MoS_2 flakes was imaged using AFM, as shown in Fig. 7.1(a), where a flat surface morphology is observed with a 14 nm height step running diagonally across. A close up view of the MoS_2 surface obtained by STM indicates presence of defects [shown in Fig. 7.1(b)], likely sulfur vacancies that are typically present in mechanically exfoliated samples [14, 15]. From a number of similar STM images, we estimate a defect density on the order of 10^{11} cm^{-2} in our samples, two orders of magnitude smaller than those reported for exfoliated monolayer MoS_2 [14].

After graphene transfer, however, the surface exhibits a non-uniform morphology with the presence of ridges and water puddles [as shown in Fig. 7.1(c)], as marked by an arrow and a circle, respectively. Graphene ridges, a few nm in height, tens of nm in width, and hundreds of nm in length, are bulged regions of graphene that occur during CVD growth due to the negative thermal expansion coefficient of graphene, which are clearly preserved during the transfer process. Water puddles are likely formed between graphene and MoS_2 during transfer, some of which remained even after annealing at 300^{o}C for 2 hours in UHV. As shown in Fig. 7.1(c), while the density of water puddles is reduced due to the dissipation of smaller ones, the annealing does not eliminate the larger ones. On the flat areas, on the other hand, nanoscale topographic fluctuations of ~0.2 nm in height are observed, similar to those found on graphene on SiC and SiO_2 substrates [16, 17]. Clearly, the graphene/MoS_2 interface is not homogeneous as previously believed [11], or at least for the polymer based transfer method. Features such as ridges, ripples, and water puddles all contribute to spatial inhomogeneities.

Furthermore, atomic scale periodic topographic corrugations, known as Moiré patterns, are also observed in atomic resolution STM images [Fig. 7.2(a)]. A line profile taken along the blue

line in Fig. 7.2(a) indicates a periodicity of 0.95 nm [Fig. 7.2(b)]. This periodicity is a function of the relative rotation angle, and thus varies spatially due to random alignment between polycrystalline CVD graphene and MoS_2 [12, 13]. The corrugation due to the Moiré structure is only ~ 0.1 nm [Fig. 7.2(b)], smaller than that observed for graphene on h-BN substrate [18].

Moiré patterns are known to modulate the local electronic properties such as those in graphene/h-BN [19], here we investigate their impact on graphene/MoS_2 junctions using scanning tunneling spectroscopy. Fig. 7.2(c) shows the differential conductance (dI/dV) spectra taken at bright and dark regions of the Moiré pattern in Fig. 7.2(a). Two characteristic minima are seen one at zero bias (E_F) due to phonon-assisted inelastic tunneling [20], and the other at 0.12 V below the Fermi level attributed to the Dirac point (E_D), indicating n-type doping. No variation in E_D is observed between the bright and dark regions of the corrugation, indicating that these atomic scale Moiré patterns do not contribute to electronic fluctuations at these graphene/MoS_2 junctions. Nonetheless, these findings indicate inherent spatial inhomogeneities such as ridges and ripples at the graphene/MoS_2 interface, which can lead to fluctuations in the SBH as revealed by the temperature dependent I-V measurements discussed below.

7.2.2 Temperature dependent I-V measurements

Temperature dependent I-V measurements are carried out on Au/graphene/MoS_2/Au junction between 210 and 300 K. Before fabricating graphene/MoS_2 heterojunctions, ~ 50 nm Au pads are deposited on MoS_2 flakes to form Ohmic contact. Fig. 7.3(a) shows the temperature dependent I-V measurements of one such Au/MoS_2/Au junction (a schematic diagram of the device is shown in the inset). A linear behavior is observed for this temperature range, indicating Ohmic contact between the Au and MoS_2. Others and our own work have also shown that Au also forms Ohmic

contact with graphene [1, 2, 20], hence our transport measurements should be dominated by the graphene/MoS_2 Schottky junctions.

Fig. 7.3(b) shows the temperature dependent I-V measurements of an Au/graphene/MoS_2/Au junction. A characteristic rectifying behavior is seen, indicative of Schottky contact formation between the graphene and MoS_2. The increase in forward bias current with increasing temperature suggests thermally activated transport across the junction that can be expressed by standard TE model [21]

$$I(T,V) = I_S(T)\left[exp\left(\frac{qV}{\eta kT}\right) - 1\right] \quad [7.1]$$

where V is the applied voltage, q the electron charge, k the Boltzmann's constant, and η the ideality factor. The saturation current, $I_S(T)$, can be expressed as [21]

$$I_S(T) = AA^*T^2 exp\left[\frac{-q\phi_{B0}}{kT}\right] \quad [7.2]$$

where A is the diode area, A^* the effective Richardson constant of the semiconductor, and ϕ_{B0} zero bias SBH, which can be obtained from the extrapolation of $I_S(T)$ in the semi-log forward bias $ln(I) - V$ [21]

$$\phi_{B0}(T) = \frac{kT}{q} ln\left(\frac{AA^*T^2}{I_S}\right) \quad [7.3]$$

The ideality factor can be calculated from the slope of the linear region of the forward $ln(I) - V$ plot [33]

$$\eta = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right) \quad [7.4]$$

Fig. 7.4(a) shows the temperature dependence of ϕ_{B0} and η, calculated by using Equations [7.3] & [7.4], with a total diode area A of ~5mm^2, and Richardson constant A^* of 5.40×10^5 Am^{-2} K^{-2} for MoS_2 [22]. For graphene/MoS_2, ϕ_{B0} increases from 0.42 to 0.58 eV and η decreases from 3.09 to 2.11 between 210 and 300 K, a behavior indicating clear deviation from the ideal TE theory, thus

barrier inhomogeneities [23].

This is further supported by the analysis of the Richardson plot, $ln\ (I_S/T^2)$ versus $1000/T$, obtained from Equation [7.2]. For temperature independent SBH, this plot should yield a straight line with a slope and intercept indicating the SBH and ideality factor, respectively [21]. However, a nonlinear behavior is observed for graphene/MoS_2 junction, as shown in Fig. 7.4(b), indicating temperature dependent barrier height, consistent with that shown in Fig.7.4(a). Linear fitting of the higher temperature data points [dashed line in Fig. 7.4(b)] yields a SBH of 0.31 eV, and A^* of 1.04×10^{-1} $Am^{-2}K^{-2}$ for MoS_2. The large deviation of A^* from the known value of 5.40×10^5 $Am^{-2}K^{-2}$ (for MoS_2 bulk[25]) indicates inhomogeneous SBHs resulting from potential fluctuations at the interface [24, 25].

7.3 Discussion

Temperature dependent SBH and ideality factor can potentially be explained by taking into account tunneling and image force in the ideal TE theory. For heavily doped semiconductors and/or at low temperatures, electrons can tunnel across the Schottky barrier with a characteristic tunneling energy E_{00} [26]

$$E_{00} = \frac{\hbar}{2}\sqrt{\frac{N_d}{m^*\epsilon_s}} \qquad [7.5]$$

where N_d is the donor concentration, m^* the electron effective mass, and ϵ_S the dielectric constant of MoS_2. Given N_d= 5.0×10^{15} cm^{-3}, $\epsilon_S \sim 11$, and $m^* \sim 0.71m_0$ [22, 27, 28], this yields an E_{00} of 0.47 meV, much smaller than the thermal activation energy of 26 and 18 meV at 300 and 210 K, respectively. This suggests that tunneling is negligible in our measurement temperature range. Furthermore, temperature dependent ideality factor, including a tunneling component, can be expressed as [29]

$$\eta_{tunn} = \frac{q_{E_{00}}}{kT} \coth\left(\frac{qE_{00}}{kT}\right) \quad [7.6]$$

which yields a η_{tunn} of 1.00004 and1.00010 at 300 and 210 K, respectively, for MoS_2. Again, these values are very close to ideal and much lower than the measured values of 2.10 and 3.17 at 300 and 210 K, respectively, further confirming that tunneling is not a significant factor in the observed temperature dependence of SBH and ideality factor.

The other possible explanation is image force barrier height reduction due the potential associated with charge buildup at metal electrode of Schottky junctions, which can be expressed as [21]

$$\Delta\phi_{imf} = \sqrt{\frac{qE_{max}}{4\pi\epsilon_s}} \quad [7.7]$$

where E_{max} is maximum field at the interface. At 300 K, Equation [7.7] gives $\Delta\phi_{imf}$= 24.79 meV with a maximum electric field E_{max} of 4.70×10^4 V/cm, and $\Delta\phi_{imf}$ of 24.20 meV with a maximum electric field E_{max} of 4.50×10^4 V/cm at 210 K. Although there is a decrease in SBH from 300 to 210 K, the reduction is too low to account for our measured SBH values of 585 and 422 meV at 300 and 210 K, respectively. Therefore, we conclude that neither electron tunneling nor image force lowering can explain the temperature dependent SBH and ideality factor in graphene/MoS_2 junctions.

To explain the deviation from ideal TE theory, we consider Werner's potential fluctuation model which assumes a continuous distribution of barrier heights at the interface [22]. This model correlates the mean (ϕ_{bm}) and apparent (ϕ_{B0}) barrier height as follows [23]

$$\phi_{B0}(T) = \phi_{bm} - \frac{q\sigma_s^2}{2kT} \quad [7.8]$$

where ϕ_{bm} and σ_S are the mean barrier height at 0 K and its standard deviation of a Gaussian distribution, respectively. $\phi_{B0}(T)$ is plotted as a function of $q/2kT$ in Fig. 7.5(a), where linear

fitting yields a mean barrier height of $\phi_{bm} = 0.96\, eV$ and$\sigma_S = 142\, mV$, higher than those previously reported [25], possibly due to difference in effective area at the junction.

The Richardson plot, $ln(I_S/T^2)$ versus$1000/T$, can be modified by combining Equation [8.2] and [8.8] [23]

$$ln\left[\frac{I_S}{T^2}\right] - \left[\frac{q^2\sigma_S^2}{2k^2T^2}\right] = \ln(AA^*) - \frac{q\phi_{bm}}{kT} \quad [7.9]$$

As shown in Fig. 7.5(b), a linear plot is observed with a slope yielding a mean barrier height of 0.97 eV, in excellent agreement with the experimentally observed value of 0.96 eV [Fig. 7.5(a)]. The extracted Richardson constant (A^*= 3.35×10^5 Am^{-2}K^{-2}) is also in much better agreement with previously reported values. Thus, the temperature dependence of SBH of graphene/MoS_2 heterostructures can be attributed to a Gaussian distribution of SBHs due to spatial inhomogeneity.

Alternately, the barrier inhomogeneities can also be considered by calculating the flat band barrier height ϕ_{bf}, an intrinsic parameter, given by [31]

$$\phi_{bf} = \eta\phi_{B0} - (\eta - 1)\xi \quad [7.10]$$

where ζ = *(kT/q)ln(N_c/N_d)*, where N_c = *2M_C(2πm*kT/h^2)$^{3/2}$* is the effective density of states, N_d~ 5.0×10^{15} cm^{-3} is the donor concentration in bulk MoS_2, and M_C is conduction band minima (M_C = 6 for MoS_2) [14]. Fig. 7.6(a) shows ϕ_{bf} as a function of temperature, where the dashed line is a linear fit with [31]

$$\phi_{bf}(T) = \phi_{bf}(0) + \alpha T \quad [7.11]$$

where $\phi_{bf}(0)$is the zero-temperature flat band barrier height and α the temperature coefficient. This yields $\phi_{bf}(0)$=1.03 eV with α = 1.02×10^{-4} eV K^{-1} for graphene/MoS_2. Clearly, the values of ϕ_{bf} are not only always greater than the ϕ_{B0}, they also exhibit a weak temperature dependence.

In addition, Equation [7.10] also correlates the measured zero bias SBH ϕ_{B0} and ideality factor η. For homogeneous junction, $\eta = 1$, thus $\phi_{bf} = \phi_{B0}$. For inhomogeneous junctions, η is always greater than 1. In the current case, since the magnitude of ϕ_{B0} is three times greater than ζ for graphene/MoS_2 junctions, the term $\eta\phi_{B0}$ is much greater than $\zeta(\eta - 1)$, hence $\phi_{B0} \sim \phi_{bf}/\eta$. From here we can draw two conclusions. First, the flat band barrier height $\phi_{bf}$is always greater than the zero bias value $\phi_{B0}$for $\eta = 1$, which is consistent with our experimental data. Second, a linear relationship (with a negative slope) between ϕ_{B0} and η can be approximated in the limits when η is either close to 1 or much larger than 1.

Indeed, as shown in Fig. 7.6 (b), a linear relationship provides an excellent fit to the plot of the zero bias barrier heights as a function of ideality factor, similar to earlier studies of graphene/semiconductor Schottky junctions [1, 2]. Extrapolation of the barrier height at ideality factor of unity yields a value of 0.79 eV for graphene/MoS_2 junctions, which is in agreement with the mean SBH obtained from the temperature dependent apparent barrier heights in Fig. 7.5(a) and modified Richardson plot in Fig. 7.5(b). This analysis confirms that transport in graphene/MoS_2 Schottky junctions are consistent with modified thermionic emission theory with a Gaussian distribution of barrier heights.

In summary, we have investigated graphene/MoS_2 Schottky junctions using scanning probe microscopy/spectroscopy and temperature dependent I-V measurements. Variations in SBH and ideality factor with temperature clearly indicate deviation from standard thermionic emission theory, which can be corroborated assuming a Gaussian distribution of the barrier height with a mean value of 0.96±0.14 eV. This distribution in barrier height is attributed to the interfacial inhomogeneities evident from graphene ridges, ripples and water bubbles. These findings reveal

the critical role of spatial fluctuations in the intrinsic barrier height in graphene/2D semiconductor Schottky junctions.

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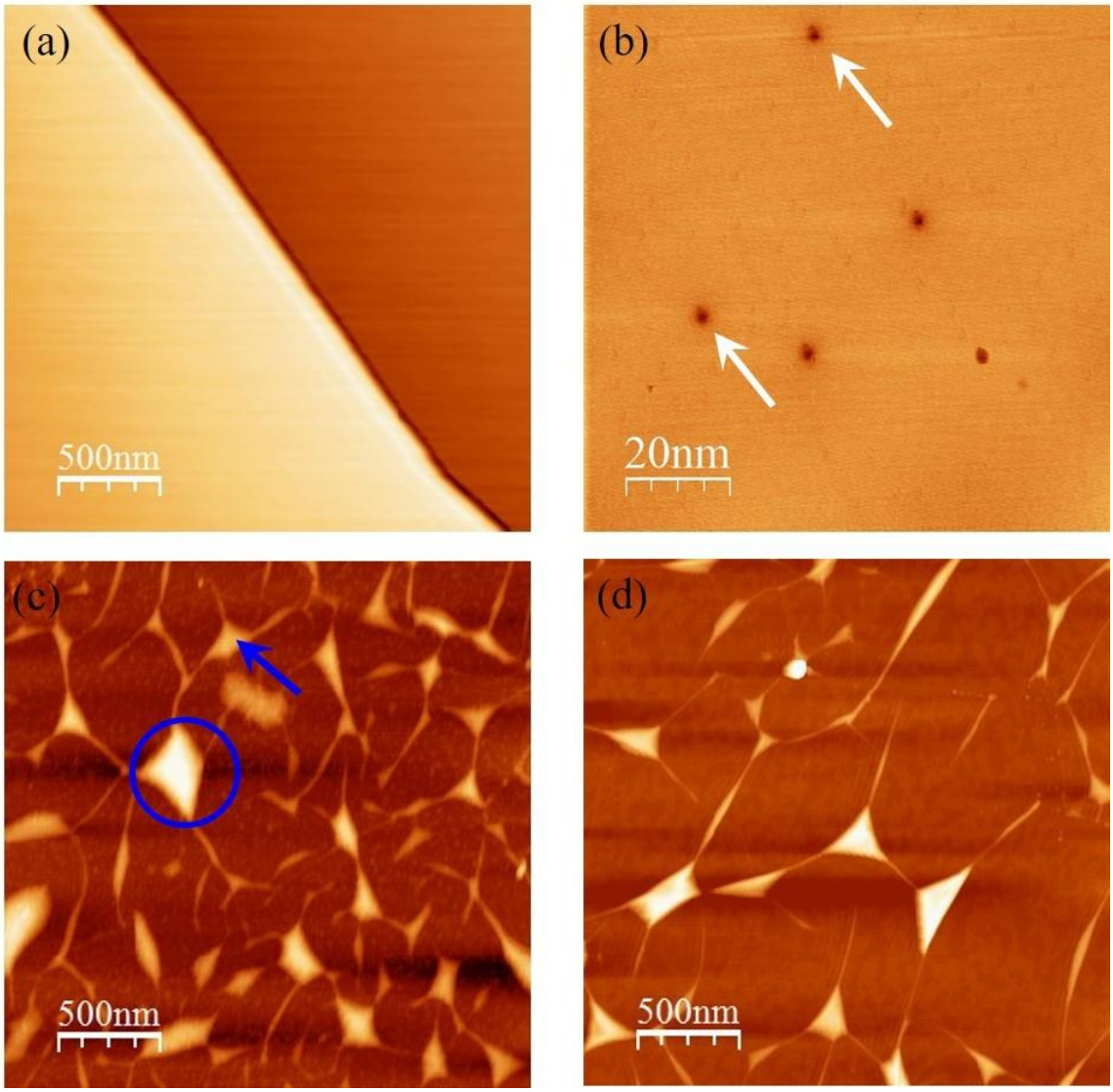

Figure 7.1: (a) AFM image of mechanically exfoliated MoS_2 crystal exhibits atomically flat surface. (b) STM image of the MoS_2 surface (V_s = 0.8 V, I_t = 0.6 nA). AFM image of CVD graphene transferred onto MoS_2 before (c) and after (d) annealing in ultrahigh vacuum at 300 °C for 2 hours.

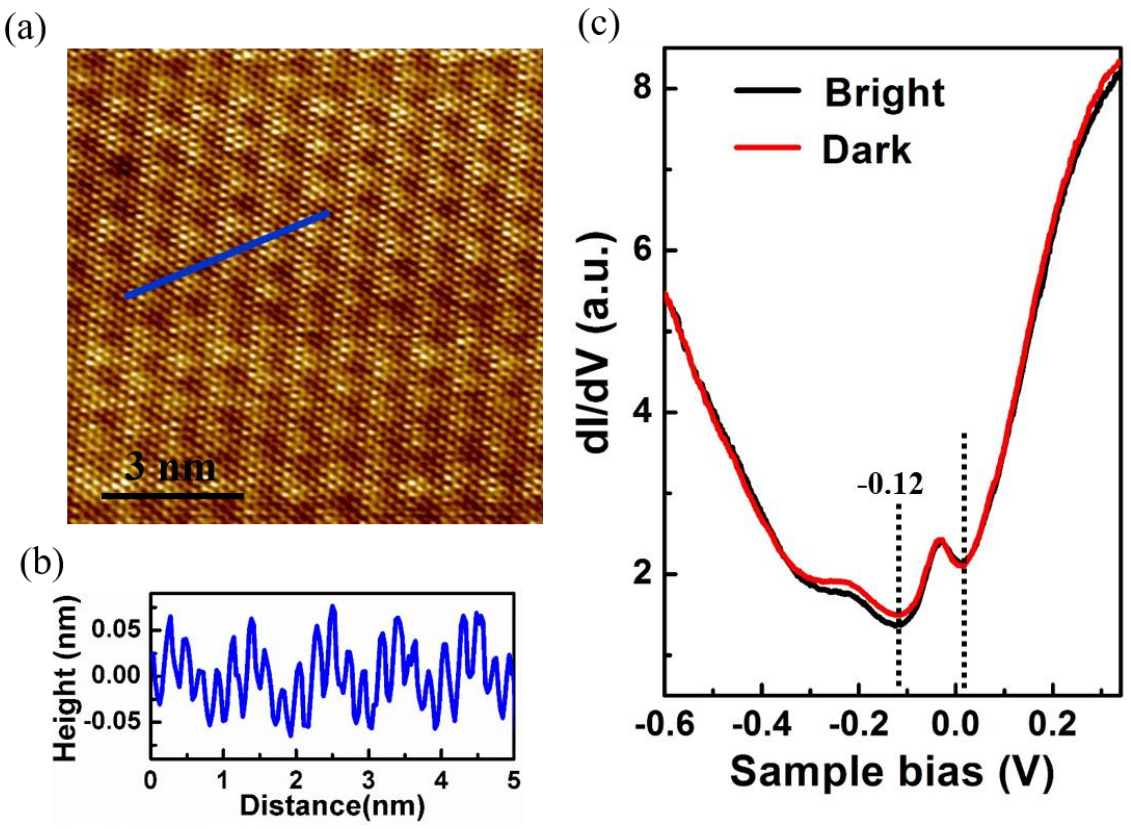

Figure 7.2: (a) Atomic resolution STM image showing moiré pattern on graphene / MoS_2 (V_s = -0.1 V, I_t = 1.2 nA). (b) Line profile taken along the blue line marked in (a). (c) dI/dV spectra of graphene/MoS_2 taken at the bright and dark periodic modulations within the Moiré pattern.

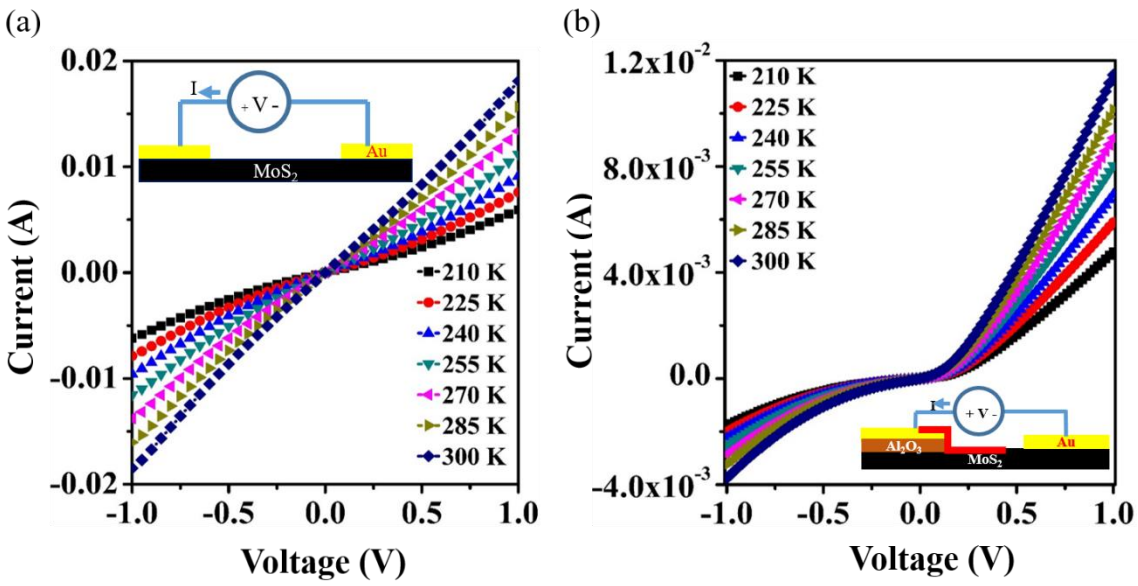

Figure 7.3: (a) Temperature dependent $I-V$ curves of Au/MoS_2/Au junctions between 210 and 300 K (inset: schematic diagram of the device). (b) Temperature dependent $I-V$ curves of graphene/MoS_2 Schottky junctions (inset: schematic diagram of the device, red segment indicates graphene).

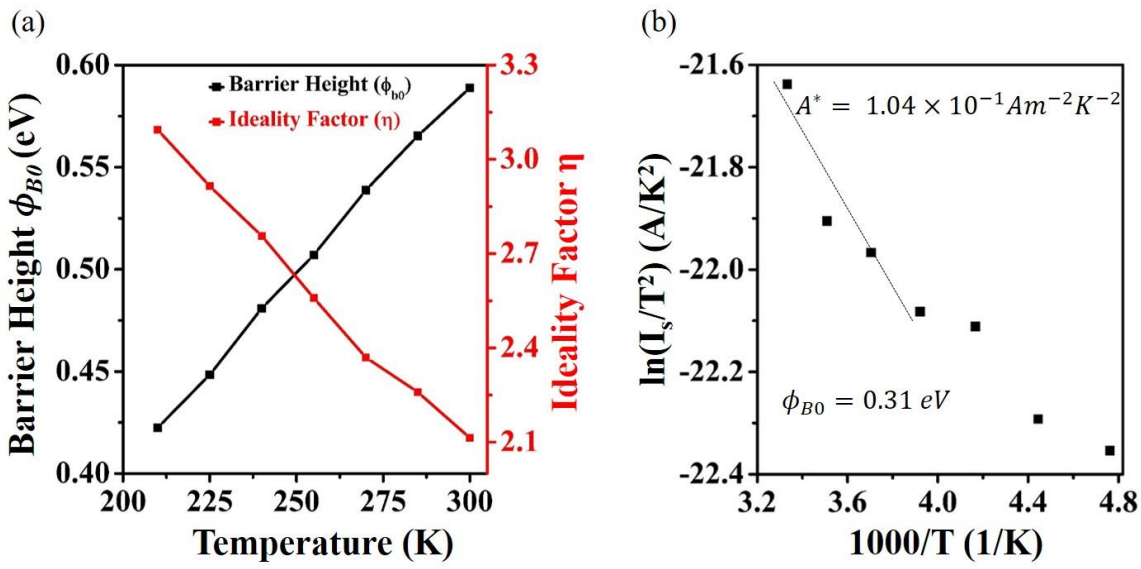

Figure 7.4: (a) Zero bias SBH and ideality factor as a function of temperature. (b) Richardson plot, $ln\left(\frac{I_S}{T^2}\right)$ versus $1000/T$, for graphene/MoS_2 junctions.

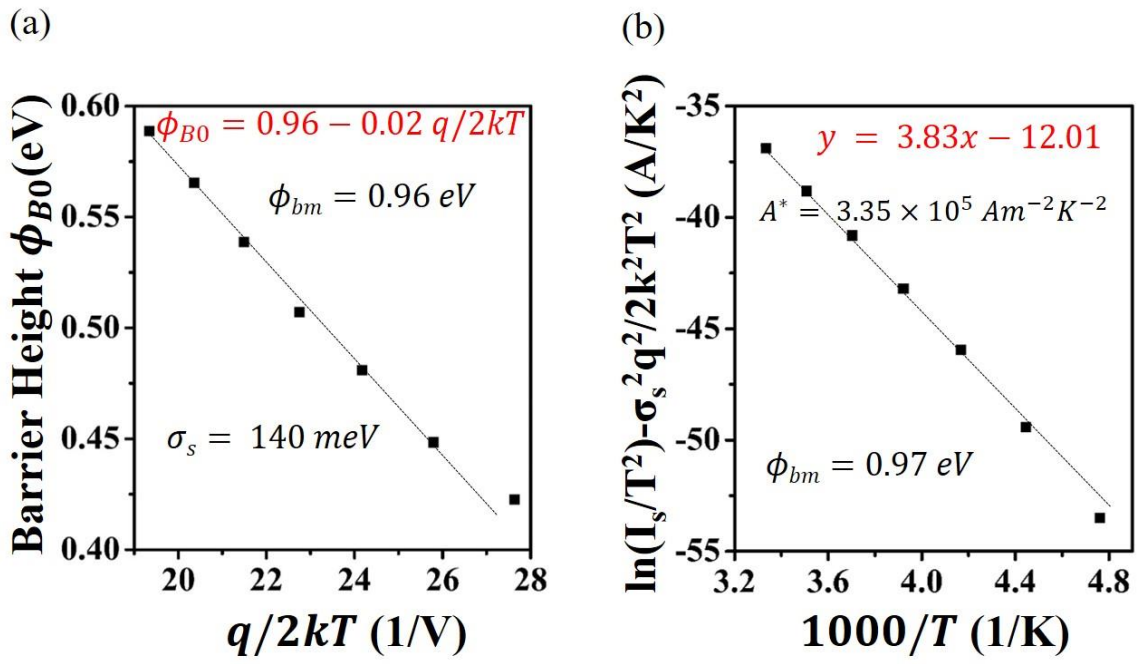

Figure 7.5: (a) Apparent zero bias barrier height (ϕ_{B0}) as a function of $q/2kT$ for graphene/MoS_2 junctions. (b) Modified Richardson plot, $ln\left(\frac{I_S}{T^2}\right) - \frac{q^2\sigma_S^2}{2k^2T^2}$ versus $1000/T$, for the same.

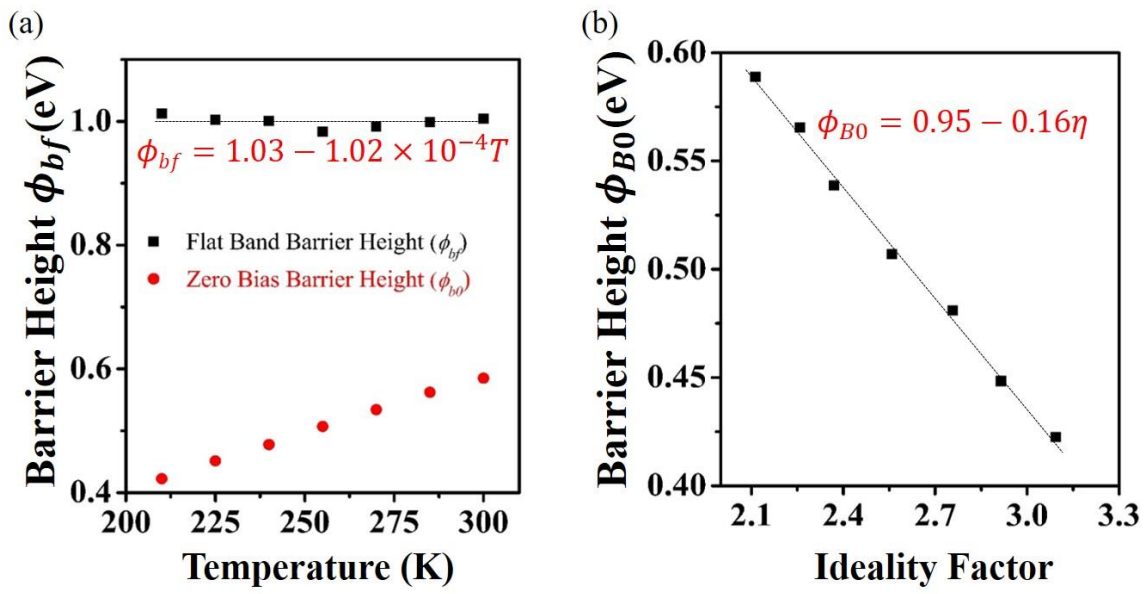

Figure 76: (a) Flat band barrier height as a function of temperature, and (b) Zero-bias barrier height ϕ_{B0} as a function of ideality factor (η) for the graphene/MoS_2 junctions.

Chapter 8
Carrier transport in reverse-biased graphene/semiconductor Schottky junctions

8.1 Introduction

The investigation of current conduction mechanism in forward biased graphene Schottky junctions with 3D (SiC, Si and GaAs) and 2D (MoS_2) semiconductors has been reported in last three chapters. In forward bias regime, the I-V characteristics of a perfect Schottky junction must follow ideal TE theory that assumes a homogeneous junction interface [1]. However, we have already shown that the intrinsic (graphene ripples, ridges and substrate steps) and extrinsic (interface/surface states) inhomogeneities at graphene/semiconductor junction interface leads to non-ideal behavior such as temperature dependent SBH and ideality factor >1 [2-4]. The TE theory cannot explain such non-ideal behavior. Therefore, a modified TE model assuming a Gaussian distribution of the barrier height is applied to explain the carrier transport in graphene/semiconductor inhomogeneous Schottky junctions [5].

Similar to forward bias regime, graphene/semiconductor Schottky junctions can be used under reverse bias, particularly in gas sensing applications due to the exponential dependence of the reverse bias current on the SBH [6-11]. Despite showing excellent sensing properties, carrier transport across graphene/semiconductor junctions under reverse bias is much less studied. In a recent work, strong bias dependent SBHs and non-saturating reverse bias current in graphene/n-Si junctions are observed and attributed to interfacial charges [12]. However, a better understanding is still required to explain non-saturating current and to describe transport mechanism in graphene/semiconductor Schottky junctions under reverse bias.

In this chapter, we present systematic studies of the temperature- and electric-field dependence of current and SBH of graphene Schottky junctions with SiC, Si and GaAs under reverse bias. We observed a reduction in barrier height with increasing bias for all junctions, suggesting electric field enhanced thermionic emission. Further analysis of the field dependence of reverse bias current revealed that while carrier transport in graphene/SiC Schottky junctions follows the Poole-Frenkel mechanism, it deviates from both the Poole-Frankel and Schottky mechanisms in graphene/Si and graphene/GaAs junctions, particularly for low temperatures and electric fields.

8.2 Results

The Schottky junctions are fabricated by transferring chemical vapor deposited (CVD) monolayer graphene onto hydrogen-terminated hexagonal SiC [Si-face (0001) and C- face ($000\,\overline{1}$)] and Si (111), and sulfur-terminated GaAs (100) substrates. The detailed description about device fabrication is given in chapter 4. All junctions exhibit rectifying behaviors, as shown in Fig. 8.1(a) for graphene/GaAs at 310 K [2, 3]. Under the reverse bias, however, the current rises with increasing bias voltage, as better seen in the semi-logarithmic plots for graphene/GaAs and Si-face SiC diodes between 250 and 340 K [Fig. 8.1(b) & 8.1(c)]. This is clearly inconsistent with the simple TE picture [1]. For $V < -3kT/q$, the reserve bias current must saturate according to

$$I(T) = AA^{*}T^{2}\, exp\left(\frac{-q\phi_{B0}}{kT}\right) \qquad [8.1]$$

where A is the junction contact area (~1.96 mm^2 for graphene/SiC and 1.62 mm^2 for graphene/Si and graphene/GaAs), A^* the effective Richardson constant (1.46x10^6, 1.12x10^6, and 0.41x10^4 $Am^{-2}K^{-2}$ for SiC, Si and GaAs, respectively), and ϕ_{B0} zero bias barrier height. Similarly, reverse bias dependent current is observed for graphene/C-SiC and graphene/Si Schottky junctions.

The non-saturating current under reverse bias suggests that the barrier height is a function of the bias voltage, as calculated following Equation [8.1] and shown in Fig. 8.2. At 310 K. The calculated ϕ_{B0} decreases with increasing reverse bias for all junctions, similar to a previous work on graphene/Si Schottky junctions [12,13], with the graphene/GaAs junction showing a lower barrier and larger variation. These behaviors suggest low interfacial states at these graphene Schottky junctions, since they are known to pin the Fermi level in the semiconductors, which leads to reverse current saturation in conventional metal/semiconductor junctions [14].

To account for the reduction of barrier height with increasing reverse bias, electric-field enhanced thermionic emission is further investigated following the Poole-Frenkel [15] and Schottky [16] mechanisms. The reverse current considering Poole-Frenkel emission is given by [15]:

$$I \propto E \exp\left(\frac{q}{kT}\sqrt{\frac{qE}{\pi\epsilon_S}}\right) \quad [8.2]$$

Whereas in the case of Schottky emission it is given by:

$$I \propto T^2 \, exp\left(\frac{q}{2kT}\sqrt{\frac{qE}{\pi\epsilon_S}}\right) \quad [8.3]$$

where E is the applied electric field given by $E = \sqrt{\frac{2qN_D}{\epsilon_S}(V + V_{bi} - \frac{kT}{q})}$, ϵ_S is the relative dielectric constant of the semiconductor (~9.66 for Si [17]), N_D the donor density of the semiconductor (~10^{18} cm^{-3}) [2], V applied bias, and V_{bi} the built-in potential. The built-in potential is a function of forward-biased SBH and the effective density of states in semiconductor conduction band (N_C) at room temperature [1], taken as 1.69 x 10^{19} for Si-SiC [17]. The mean SBH value of 1.16 eV is taken for graphene/Si-SiC Schottky junction [2].

Thus, if the Poole-Frenkel effect contributes to the reverse current, then the plot of $ln\,(I/E)$ versus $\sqrt{E}$ should be linear. Similarly, if a linear plot is found for $ln\,(I/T^2)$ versus $\sqrt{E}$, then the

Schottky mechanism is present. Fig. 8.3(a) and8.3(b) shows plots of $ln\ (I/E)$ and $ln\ (I/T^2)$ as a function of $\sqrt{E}$, respectively, for the Graphene/Si-SiC Schottky junction. Clearly, both are near linear for all temperatures, indicating that both Schottky and Poole-Frenkel emissions are present.

To distinguish which mechanism the carrier transport is dominated by, we calculate the emission coefficient following [15]

$$S = \frac{q}{nkT}\sqrt{\frac{q}{\pi\epsilon_S}} \qquad [8.4]$$

where n=1 for Poole-Frenkel and n=2 for Schottky emission. The calculated coefficients are compared with that obtained by curve fitting for both Poole-Frenkel and Schottky emissions at different temperatures, as shown in Table 8.1 between 250 and 340 K for the Graphene/Si-SiC Schottky junction. For the Poole-Frenkel emission, the experimental values are almost ~2-2.3 times that of the calculated value at all temperatures. For Schottky emission, the experimental values are ~3.5 times larger. Similar trend is also found for graphene/C-SiC junction. Thus, carrier transport in graphene/SiC Schottky junctions under reverse bias is more consistent with the Poole-Frenkel mechanism for these temperatures.

Similar analysis was performed for graphene/GaAs and graphene/Si junctions, as shown in Fig. 8.4 and 8.5, where ϵ_S is taken as 12.9 [18] and 11.7 [19], N_D ~10^{16} and 10^{17} cm^{-3}, N_C = 4.70×10^{17} and 2.86×10^{19} cm^{-3} for GaAs, and Si, respectively [17], and the mean SBH values of 1.14 and 0.76 eV are taken for graphene/Si and graphene/GaAs Schottky junctions [3]. For graphene/GaAs [Fig. 8.4(a) & (b)], both the Poole-Frenkel and Schottky emission plots are linear above 310 K, suggesting a possible co-existence of both mechanisms at higher temperatures. Again the Poole-Frenkel and Schottky emission coefficients must be considered to identify their contributions to carrier transport. At 340 K, the Poole-Frenkel coefficient obtained from the fit is

0.119 $(V/cm)^{1/2}$, ~ 16 times the calculated value of 0.007 $(V/cm)^{1/2}$. For the Schottky emission, the experimental value (0.128 $(V/cm)^{1/2}$) is ~35 times greater than that calculated (0.0036 $(V/cm)^{1/2}$).

For the graphene/Si Schottky junction, the Poole-Frenkel and Schottky emission plots are shown in Fig. 8.5 (a) & (b). In both cases, although they are still linear at 340 K, non-linearity is found for temperatures below 310 K, particularly in the low electric field region. Fittings to the linear plots at 340 K yield an experimental emission coefficient of 0.0615 $(V/cm)^{1/2}$, ~ 8 times greater than the calculated value (0.0076 $(V/cm)^{1/2}$) for the Poole-Frenkel mechanism. For the Schottky emission, the experimental value (0.0658 $(V/cm)^{1/2}$) is ~17 times greater than that calculated (0.0038 $(V/cm)^{1/2}$).

8.3 Discussion

These results suggest that carrier transport in the reverse-biased graphene/GaAs and graphene/Si Schottky diodes deviate from the Poole-Frenkel and Schottky emission, particularly at low temperatures and electric fields. This may be due to the much larger depletion width, ~ 0.1-0.5 μm, for the graphene/Si and graphene/GaAs Schottky junctions, comparable to that reported for graphene/Si [20]. For comparison, the depletion width is only ~35-48 nm for the graphene/Si-SiC junctions. In addition, other conduction mechanisms such as bias dependent doping [12], i.e., electric field dependence of the Fermi level in graphene, should also be taken into account in these non-linear regimes.

In conclusion, reverse-biased graphene/SiC, graphene/GaAs, and graphene/Si Schottky junctions are studied by temperature dependent I-V measurements between 250 and 340 K. A reduction in barrier height with increasing reverse bias is observed for all junctions, consistent with electric-field enhanced thermionic emission. Analysis of the field dependence of the reverse

current reveals that while carrier transport in graphene/SiC Schottky junctions follows the Poole-Frenkel mechanism, it deviates from both the Poole-Frankel and Schottky mechanisms in graphene/Si and graphene/GaAs junctions, particularly in the low temperature and field regimes, where field dependent doping in graphene should also be taken into account. These findings present the direct experimental evidence for electric-field enhanced thermionic emission in graphene/semiconductor Schottky junctions under reverse bias, providing insights on carrier transport mechanisms to help improving functionalities of graphene-based devices.

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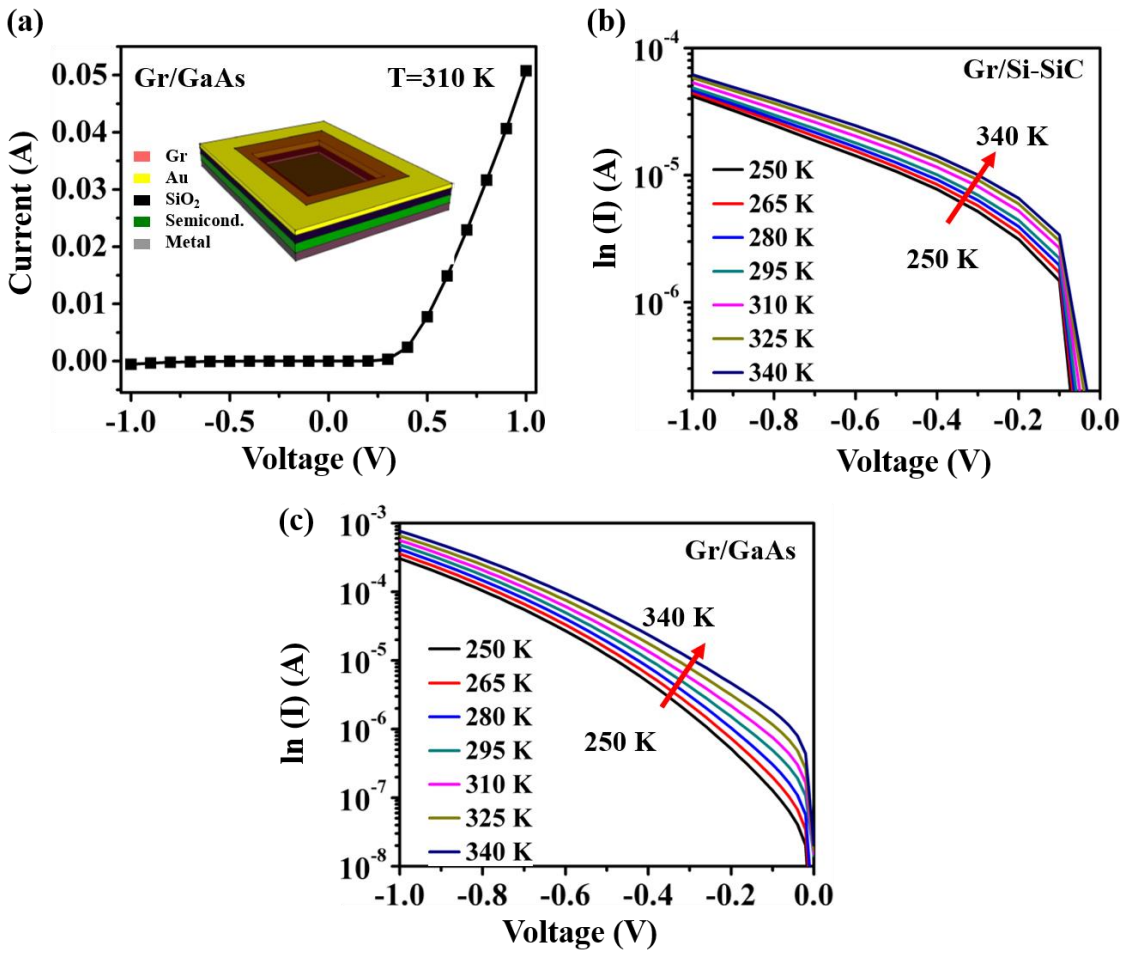

Figure 8.1 (color online) (a) I-V curve of graphene/GaAs Schottky junction at 310 K showing a rectifying behavior (inset: schematic diagram of the devices). Temperature dependent I-V characteristics of (b) graphene/Si-SiC and (c) graphene/GaAs Schottky junctions in the reverse bias regime between 250 and 340 K.

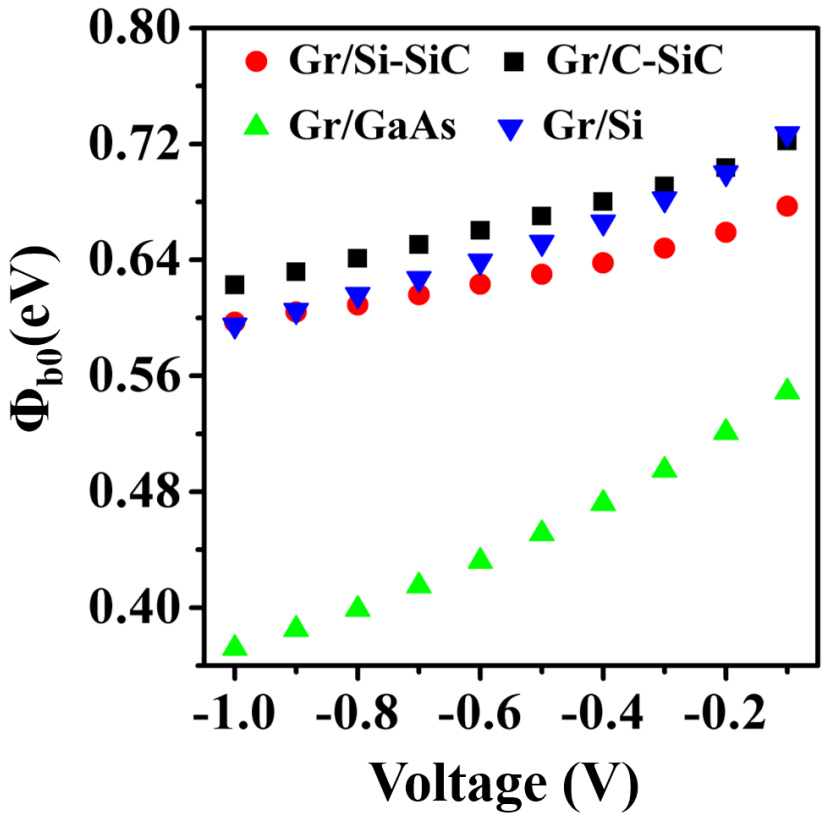

Figure 8.2: Calculated Schottky barrier height ϕ_{B0} as a function of reverse bias voltage at 310 K.

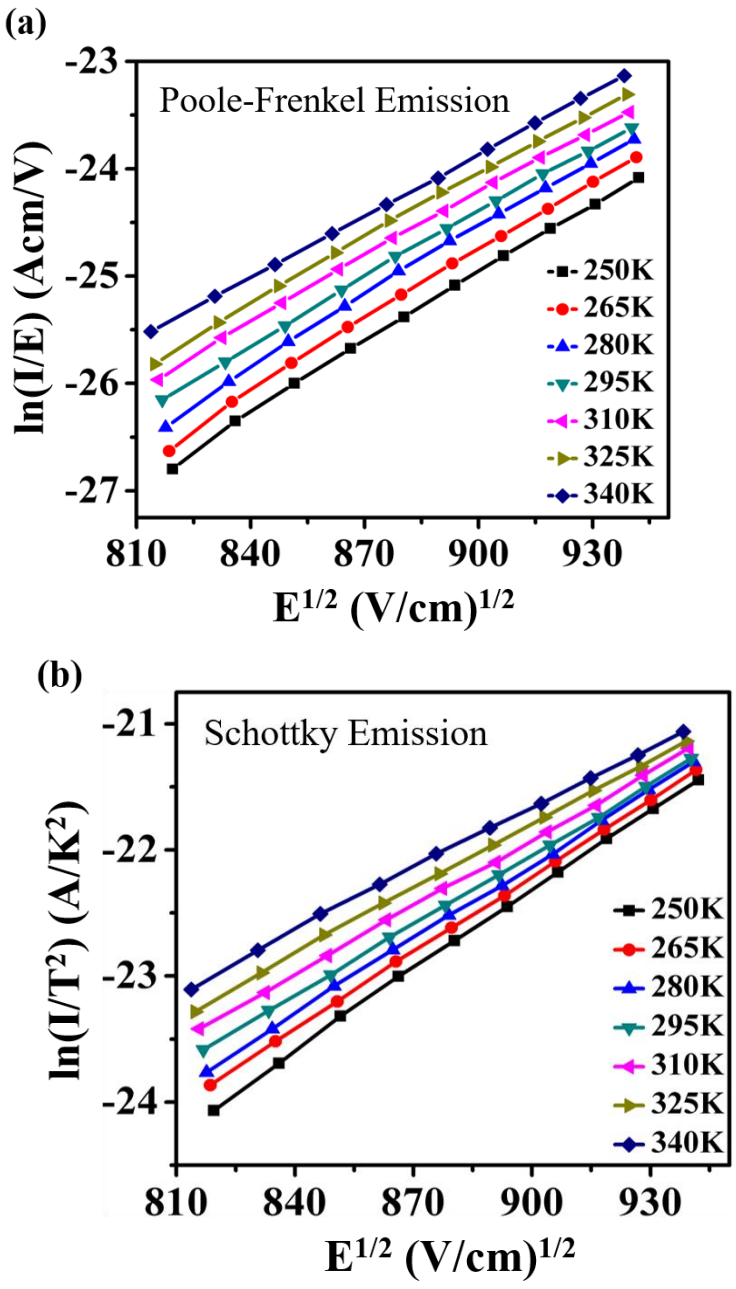

Figure 8.3: Temperature dependent (a) Poole-Frenkel and (b) Schottky emission plots for graphene/Si-SiC Schottky junctions.

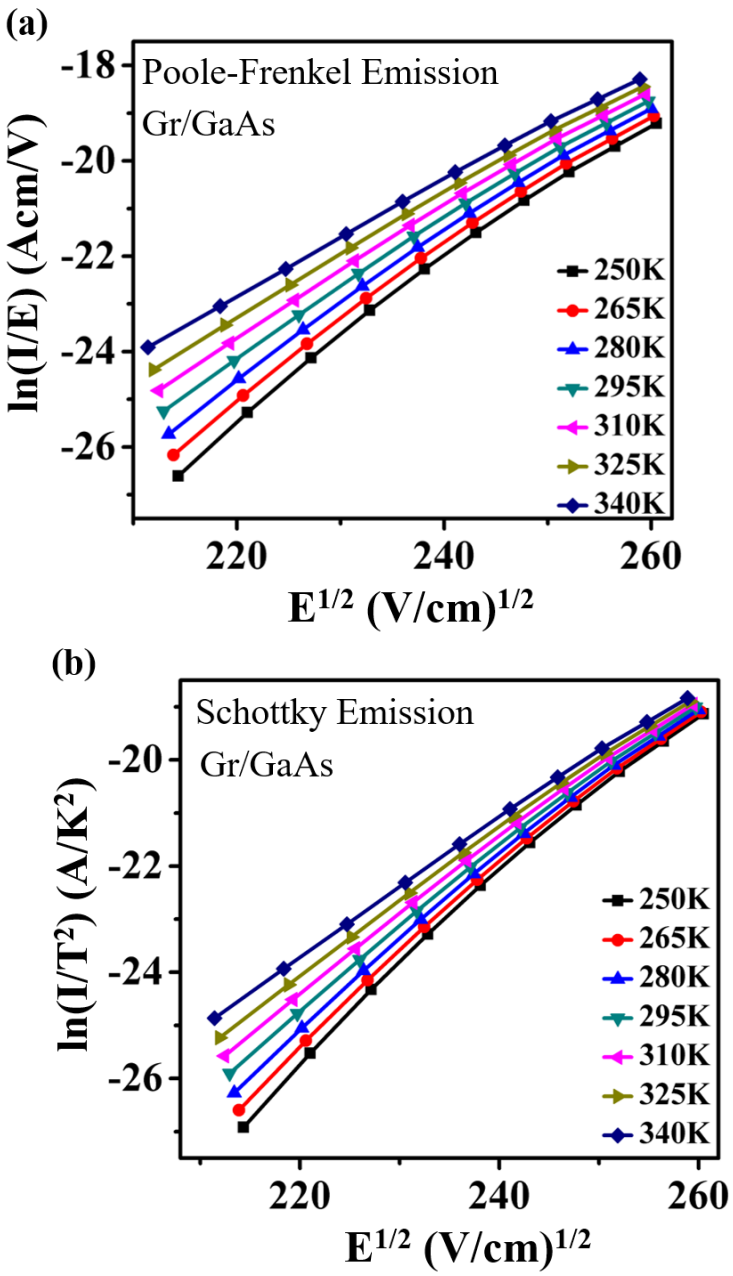

Figure 8.4: Temperature dependent (a) Poole-Frenkel and (b) Schottky emission plots for graphene/GaAs Schottky junctions.

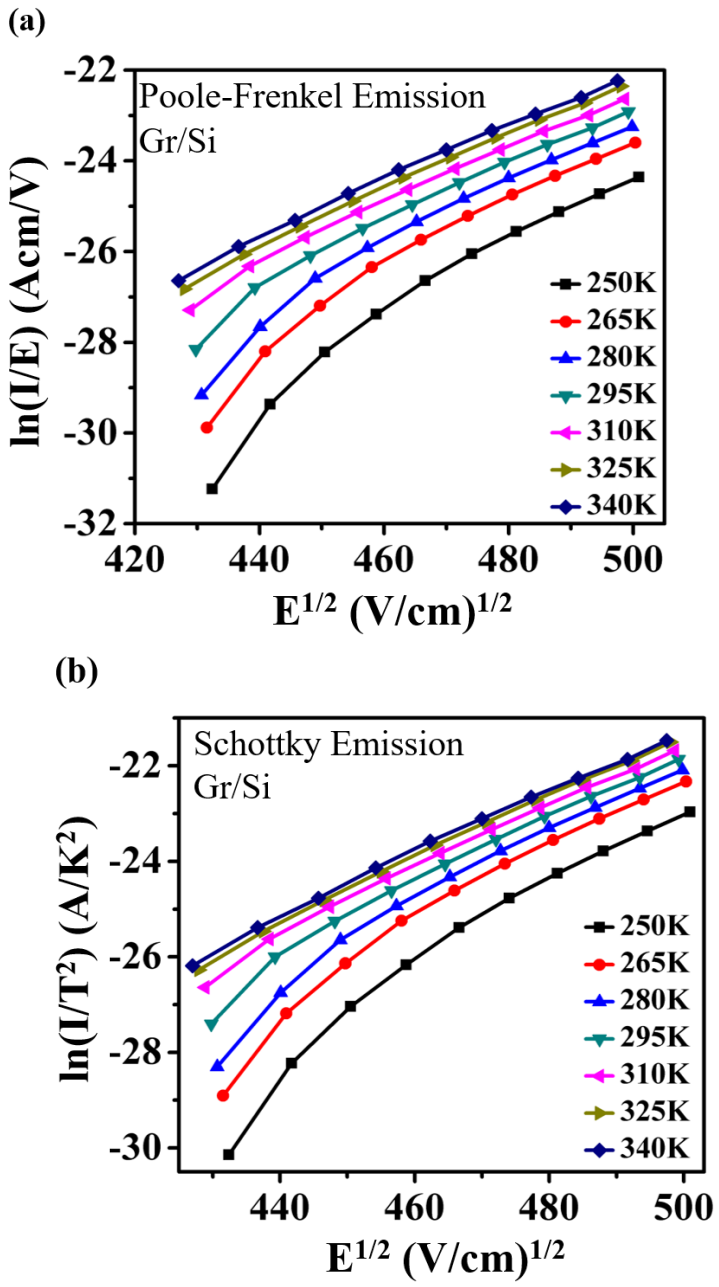

Figure 8.5: Temperature dependent (a) Poole-Frenkel and (b) Schottky emission plots for graphene/Si Schottky junctions.

Temperature (K)	Poole-Frenkel emission $(V/cm)^{1/2}$		Schottky emission $(V/cm)^{1/2}$	
	Calculated	From fit	Calculated	From fit
250	0.0113	0.0224	0.0056	0.0213
265	0.0107	0.0219	0.0053	0.0202
280	0.0101	0.0215	0.0050	0.0198
295	0.0096	0.0206	0.0048	0.0185
310	0.0091	0.0199	0.0046	0.0178
325	0.0087	0.0194	0.0044	0.0171
340	0.0083	0.0191	0.0041	0.0161

Table 8.1 Comparison of calculated and experimental Poole-Frenkel and Schottky emission coefficients between 250 and 340 K for the graphene/Si-SiC Schottky junction

Chapter 9
Summary and Outlook

9.1 Summary

When graphene is interfaced with a semiconductor, a Schottky junction with rectifying I-V properties forms at the interface. This dissertation investigates the impact of interface inhomogeneities on the electronic and transport properties of graphene/semiconductor Schottky junctions.

We transfer CVD grown graphene on SiC, Si, GaAs and MoS_2 semiconducting substrates to fabricate such Schottky junctions. For graphene/(C- and Si-face) SiC Schottky junctions, we observe the formation of graphene ripples and ridges which results an inhomogeneous junction interface. We find that the observed fluctuations in graphene Dirac point position are directly correlated to such topographic corrugations which leads to variation in SBH. Furthermore, we observe temperature dependence of barrier height and ideality factor in I-V-T measurements. To explain such behavior, we apply a model of Gaussian distribution of barrier heights, applicable to inhomogeneous interface, and obtain a temperature independent SBH. In this work, graphene ripples, ridges and SiC steps contribute to inhomogeneity at interface.

Similar to graphene/SiC junctions, we observe a temperature dependence of junction parameters in graphene/Si and graphene/GaAs Schottky junctions too. However, in contrast to graphene/SiC, no direct correlation of topographic corrugation with Dirac point fluctuations is observed in such Schottky junctions. We observe random fluctuations in Dirac point position and attribute it to the interface states and/or charge impurities of semiconductors, more obvious in Si and GaAs. Overall, we discover two types of atomic-scale inhomogeneities that cause fluctuations

in the SBH at graphene/semiconductor junctions: (a) graphene ripples, ridges and substrate steps in SiC, and (b) trapped charge impurities and surface states in Si and GaAs.

Next, we choose a 2D layer semiconductor; MoS_2, to overcome the deteriorating effect of interface inhomogeneities. Besides graphene ripples, ridges and small water bubbles, we observe atomic scale moiré patterns at graphene/MoS_2 junction interface. We notice that there are no fluctuations in Dirac point position related to such moiré patterns. However, we still observe a temperature dependent barrier height and ideality factor as in previous cases of graphene Schottky junctions with conventional semiconductors. Under our experimental conditions, we attribute such behavior to graphene ripples, ridges and water bubbles.

At last, we study the reverse bias characteristics of graphene Schottky junctions with SiC, Si, and GaAs. We observe a non-saturating reverse bias current and bias dependent SBH for all these junctions. We demonstrate that Poole-Frenkel emission can explain the reverse bias behavior of graphene/C- and Si-SiC Schottky junctions. However, the behavior of graphene/Si and graphene/GaAs Schottky junctions could not be explained by any of the considered models; Poole-Frenkel and Schottky emission. These findings reveal the critical role of spatial inhomogeneities in the intrinsic SBH in graphene/3D (and 2D) semiconductor Schottky junctions.

9.2 Outlook

We demonstrate that the formation of graphene ripples and ridges at graphene/semiconductor junction interface is inevitable, irrespective of semiconductor type; polar, non-polar, 3D or 2D semiconductors. We also demonstrate the negative effects of such features on the transport properties of these Schottky junctions. To make better performance devices, several potential solutions are given in next sections.

9.2.1 Graphene dry transfer process

It has been reported that a thin layer of PMMA preserves the ripples and ridges of graphene upon drying in PMMA assisted wet transfer process [1, 2]. Furthermore, it could cause cracks and tears in monolayer graphene. This can be avoided by applying a second layer of PMMA coating before dissolving the first PMMA layer [3]. Second layer of PMMA gives relaxation to partially dissolved first PMMA layer and allows it to make better contact with substrate. This PMMA double layer method provides large size graphene transfer with only a few cracks, holes and less ripples. However, the formation of native oxide (particularly in Si) and trapped water cannot be avoided due to the involvement of water in such graphene transfer processes.

Such water dipping related issues can be avoided by using dry transfer method where a thin film of PDMS is coated on graphene/Cu and slowly peeled off from Cu substrate [4-6]. Graphene is transferred to PDMS due to the higher adhesion force of PDMS-graphene than that between graphene-copper. After putting PDMS/graphene onto any substrate, NMP/TBAF solution can be used to remove PDMS. Such process provides clean graphene transfer that can offer relatively homogeneous junction interface [4-6].

9.2.2 Nanoscale Schottky junctions

For graphene/MoS_2 Schottky junctions, we observe moiré patterns, which don't lead to fluctuations in Dirac point. This suggests that a Schottky junction fabricated only in the flat area can suppress the effect of inhomogeneities. In our work, we find an average flat area of less than 100 nm^2 in all junctions, therefore a device with dimensions in nanometer range can overcome the formation of ripples, ridges and other inhomogeneities.

9.2.3 Direct growth of graphene on semiconductors

Graphene transfer process related complexities and contaminations at junction interface can be avoided by CVD growth of graphene directly on any substrate. Recently, CVD growth of monolayer graphene on sapphire is reported at ~ 1350^{o}C with H_2/CH_4 ratio of 10 [7]. This method lightens the path to grow graphene directly on semiconductors which would eliminate/reduce the spatial inhomogeneities and provide better performance devices.

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Education

Ph.D., Condensed Matter Physics (Aug 2010- Jul 2016)
University of Wisconsin, Milwaukee, WI, USA
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Technical skills

- **Micro-fabrication:** Class 1000 cleanroom processes, photolithography, wet chemical etching, reactive ion etching, rapid thermal annealing, optical mask design and wire bonding
- **Thin film deposition:** Physical vapor deposition (DC/RF sputtering, e-beam evaporation, molecular beam epitaxy), and Chemical vapor deposition (CVD)
- **Thin film characterization:** AFM, XRD, SEM, XPS, EDS, optical microscopy, Raman microscopy, and scanning tunneling microscopy/spectroscopy
- **Device characterization**: Electrical and magneto transport at cryogenic temperature

Research Publications

1. X. Dong, C. Yan, **D. Tomer**, C. H. Li and L. Li. Spiral growth of few-layer MoS_2 by chemical vapor deposition. *App. Phys. Lett*. **109**, (2016).
2. D. Tomer, **S. Rajput**, L. J. Hudy, C. H. Li and L. Li. Inhomogeneity in barrier height at graphene/Si (GaAs) Schottky junctions. *Nanotechnology* **26,** 215702 (2015).
3. D. Tomer, **S. Rajput**, L. J. Hudy, C. H. Li and L. Li. Carrier transport in reverse biased graphene-semiconductor Schottky junctions. *Appl. Phys. Lett.* **106,** 173510 (2015).
4. T. Hosseini, D. Tomer, **S. Raiput**, L. Li and N. Kouklin. Transport and photoconduction characteristics of metal-graphene-4H-SiC (0001) heterojunction devices. *Appl. Phys. Lett.* **105,** 223107 (2014).
5. D. Tomer, **S. Rajput**, L. J. Hudy, C. H. Li and L. Li. Intrinsic inhomogeneity in barrier height at monolayer graphene/SiC Schottky junction. *Appl. Phys. Lett.* **105**, 021607 (2014).

Conference Presentations

- "Spatially inhomogeneous barrier height in graphene/MoS2 Schottky junctions" [Oral Presentation] APS March meeting 2016, Baltimore, MD, U.S.A.
- "Barrier inhomogeneities at monolayer graphene based Schottky junctions" [Poster Presentation] MRS Spring meeting 2015, San Francisco, CA, U.S.A.
- "Temperature and bias dependence of barrier heights in graphene / semiconductor Schottky diodes under reverse bias", [Oral Presentation] APS March meeting 2015, San Antonio, TX, U.S.A.
- "Intrinsic inhomogeneity in barrier height at monolayer graphene/SiC Schottky junction", [Oral Presentation] Physical Electronics Conference 2014, La Crosse, WI, U.S.A.
- "Measuring the Schottky barrier height at graphene/SiC junction", [Oral Presentation] APS March meeting 2014, Denver, CO, U.S.A.

Awards/Achievements

- David Litchman scholarship for best experimental physics graduate student 2015, UWM, USA
- Ministry of Human Resource and Development (MHRD) fellowship 2007, IITD, India
- Graduate Aptitude Test in Engineering (GATE) award 2005, INDIA