

DESIGN OF ACTIVE FILTER USING SUBSTRATE INTEGRATED WAVEGUIDE

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Lastly, I would like to thank my family for the constant encouragement and love that I have relied on during graduate studies and my stay away from home.

ABSTRACT

In this project we have designed circuit models for Substrate Integrated Waveguide (SIW) filter at X band with a bandwidth of 1 GHz. These equivalent models are designed in ADS using lumped and semi-lumped approach. Based on these models a 3D structure of the filter is designed in CST. This design is fabricated on a Rogers 5880 substrate using photolithography and corresponding measurements are done to compare with simulations.

In the second half of the project SIW filter is used with an active element to achieve non-negative insertion loss. This can be achieved by using a negative resistance element such as Gunn Diode, Tunnel Diode etc. Gunn diode model is designed using JFETs which is integrated with the filter to demonstrate active filtering. Alternatively another method is explored using PHEMTS. PHEMT used in this case is VMMK 1225 from Avago Technologies.

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CHAPTER 1

SIW INTRODUCTION

Substrate Integrated Waveguide (SIW) is a promising candidate for mm-wave technology because it is easy to fabricate, flexible and cost effective [1]. This technology also preserves most of the advantages of conventional metallic waveguide namely complete shielding, low loss, high quality-factor and high power handling capability. SIW has received tremendous attention at mm wave frequencies of around 60 GHz. SIW structure is fabricated by using two periodic rows of metallic vias connecting the top and bottom ground planes of a dielectric substrate [2].

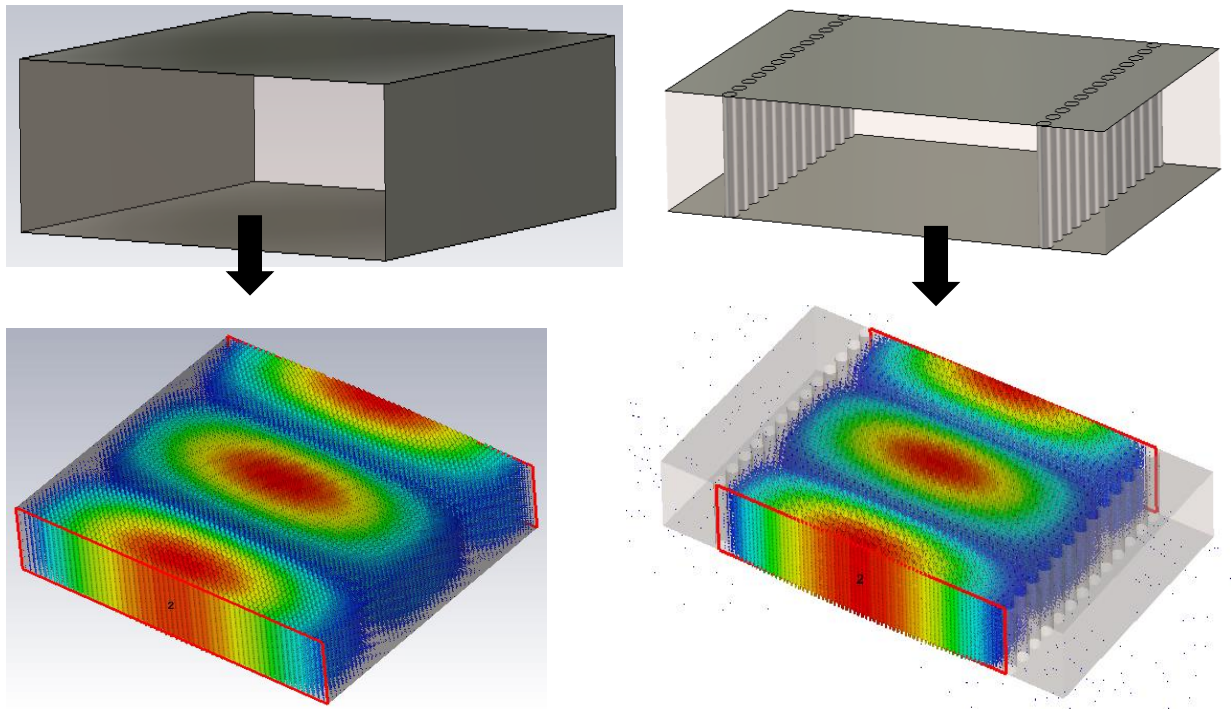


Fig 1. Field Distribution of a waveguide structure (left) and SIW structure (right)

To compare the field distribution of SIW vs conventional waveguide, X band simulations were done. Figure 1 compares the field distribution of SIW and conventional waveguide. We can see striking similarities between the two in particular the electromagnetic field distribution is TE₁₀ like. SIW is marginally leakier compared to conventional waveguide due to leakage between metallic vias. By carefully designing the diameter and pitch of the vias we can make this loss negligibly small. Dimensions

of the SIW structure can be derived from conventional waveguide width (a_w) using the following formulation.

$$a_{siw} = \frac{a_w}{\sqrt{\xi_r}}$$

$$a_{eff} = a_{siw} - 1.08 \frac{d_v^2}{p_v} + 0.1 \frac{d_v^2}{a_{siw}}$$

SIW width a_{eff} is calculated based on the corresponding rectangular waveguide width a_w . In the above equation parameters ξ_r , d_v and p_v represent substrate dielectric constant, via diameter and pitch of the vias respectively. The diameter and pitch needs to be set such that there is no leakage between metallic vias. The following constraints are put on the diameter and pitch to ensure that.

$$d_v < \frac{\lambda_g}{5}$$

$$p_v \leq 2d_v$$

CHAPTER 2

TRANSITION DESIGN

To build an entire system based on SIW there is a need to integrate passive components like filters, couplers and antennas with active circuits [3]. Transitions are an important bridge between non planar and planar circuits. But they are often expensive, bulky and require run time tuning. Integration of waveguides into the substrate allows for efficient wideband transitions between waveguide and planar circuits like microstrip, coplanar waveguide, stripline etc.

2.1 *SIW with Microstrip Transitions*

There are various approaches for integrating waveguide with planar circuits. In this work a simple tapered microstrip transition was used. The impedance of a waveguide is quite high ($\sim 400\text{-}500\ \Omega$). We have to smoothly transform this impedance to $50\ \Omega$. Figure 3 shows S21 response of this transition, insertion loss is about 0.6 dB in the band of interest [4].

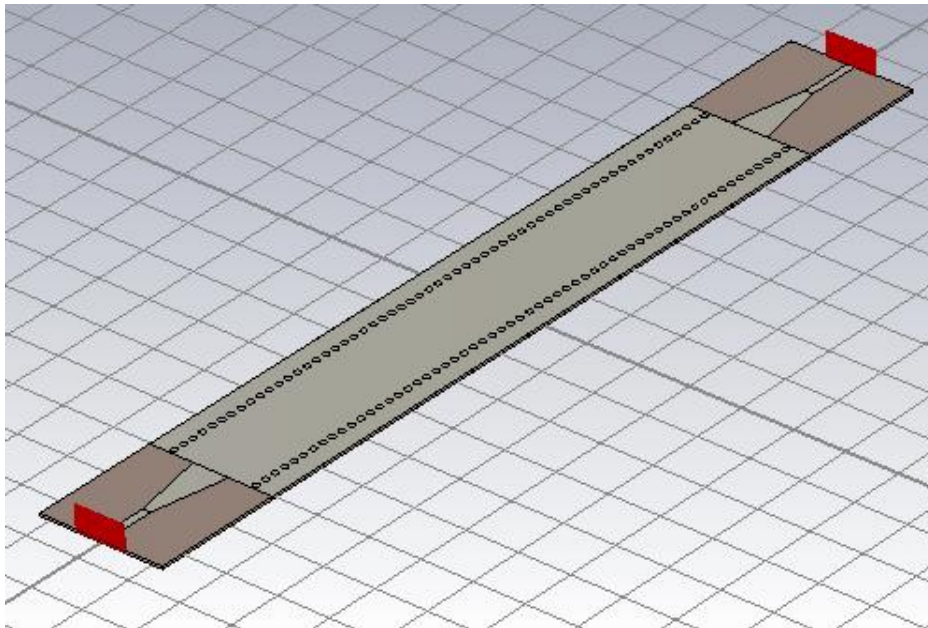


Fig 2. Design of the SIW structure with microstrip transitions

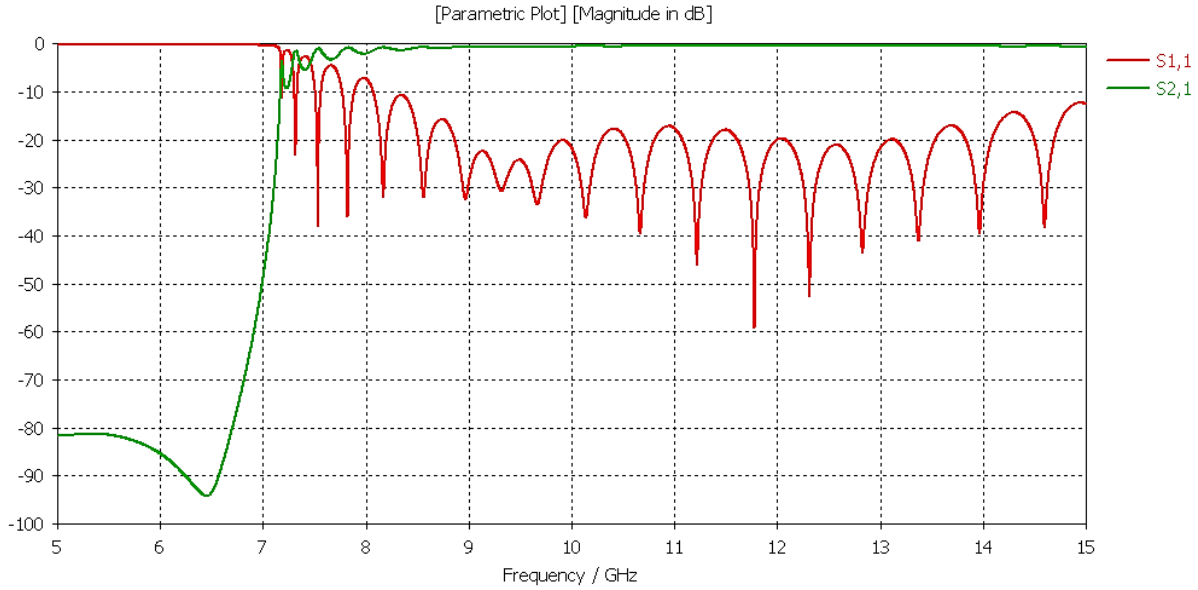


Fig 3. S parameter response of the SIW to microstrip transition

Simulations were done to optimize the length and width of this taper. Figure 4 & 5 show simulation results for varying lengths and widths of the taper. Such simulations are necessary to determine the best transition with minimum S21 loss. Best results were observed for a width of 6cm and length of 14 cm with an average loss of about 0.6 dB. In our case a microstrip width of 1.53 mm gives 50 Ω impedance at the input. This calculation was done using Linecalc tool in ADS. Figure 6 shows the E field distribution along the length of the transition. This provides a good understanding of how the mode travels along the length.

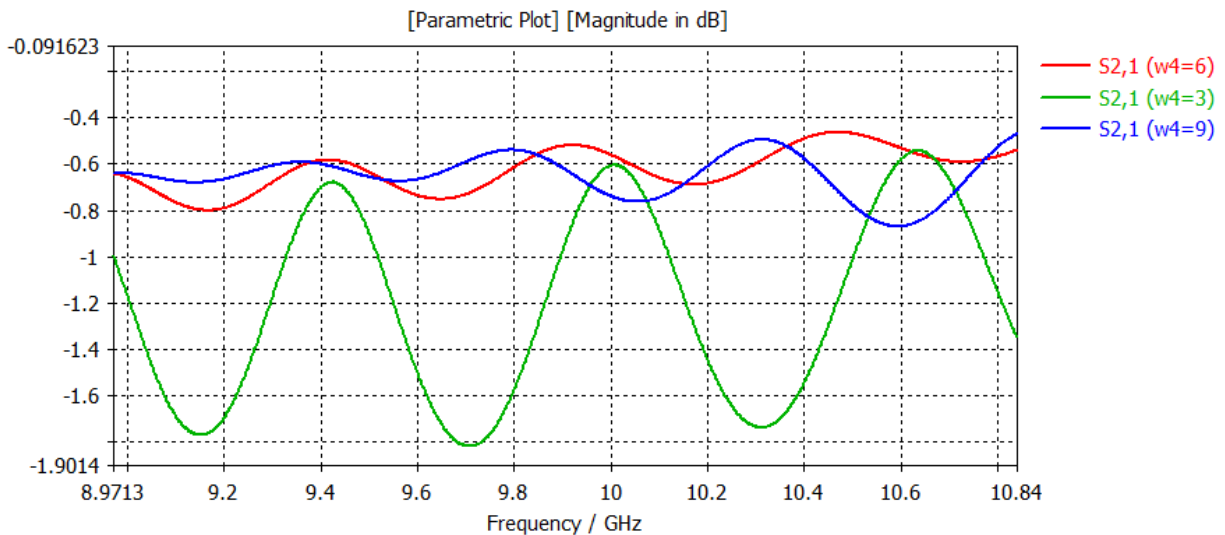


Fig 4. S21 response of the SIW structure for 3 different values of microstrip transition widths

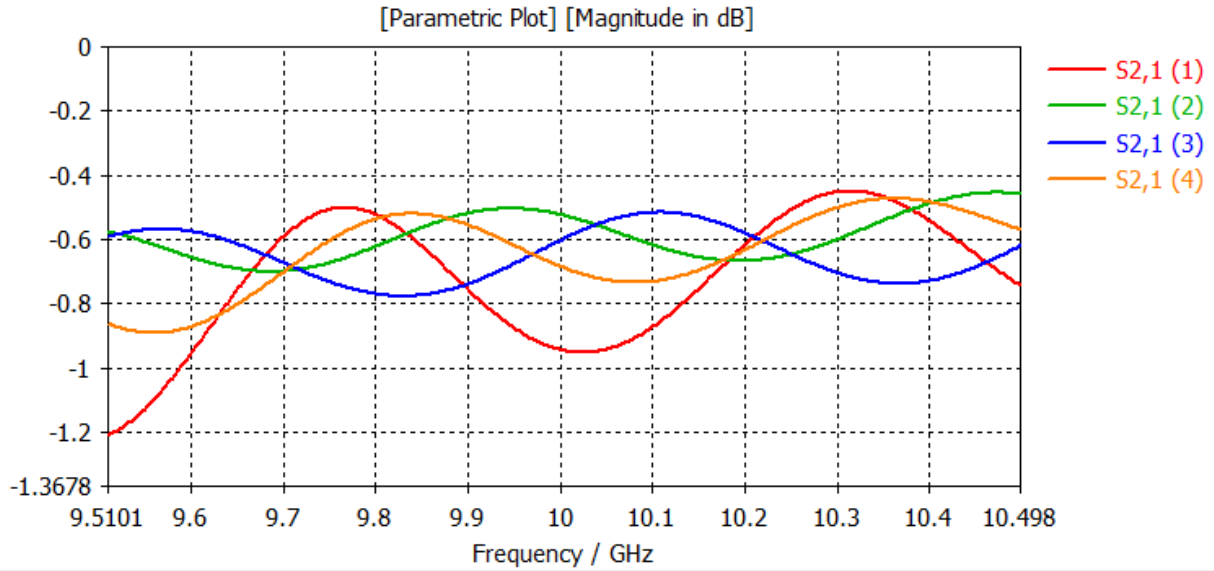


Fig 5. S21 response of the structure with microstrip transitions at lengths 10, 13.33, 16.67, 20 mm respectively

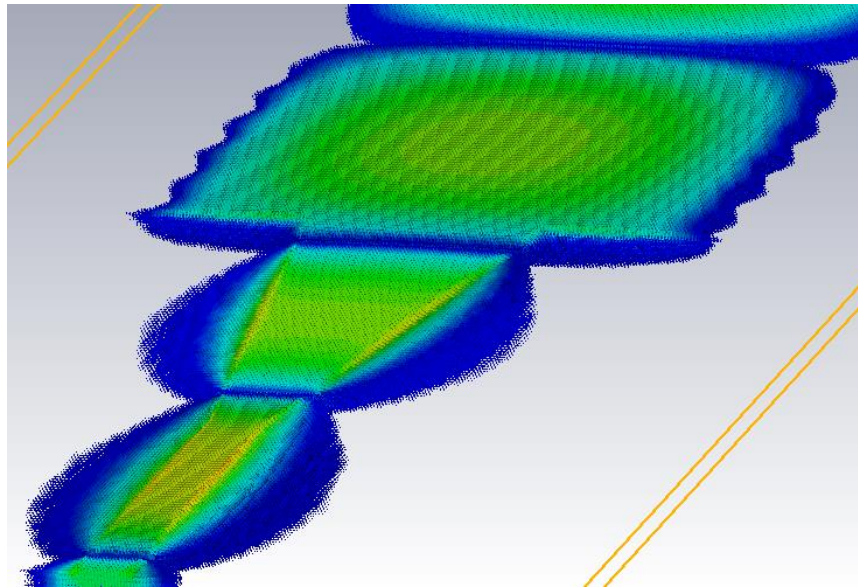


Fig 6. Electric field distribution at SIW to Microstrip transition

2.2 SIW to Stripline Transition

For low power level applications SIW is usually interfaced with microstrip. Other transitions for surface mount applications include coplaner waveguides, slotlines etc. All these interconnects assume low power

application which transmission lines can handle. But SIW being a waveguide based technology can handle medium power levels [5].

Stripline is a TEM transmission line capable of handling much higher powers. Here we study SIW-stripline interconnect that is capable of handling medium power level capability of both SIW and stripline. This design is based on SIW-microstrip transition discussed in section 2.1. Another substrate layer is added in order to excite the stripline mode directly from the SIW end.

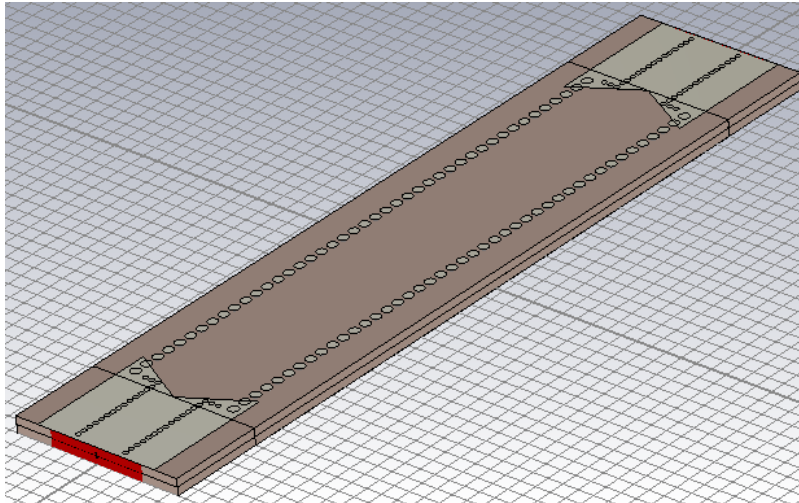


Fig 7. A 3 dimensional view of SIW to Stripline transition

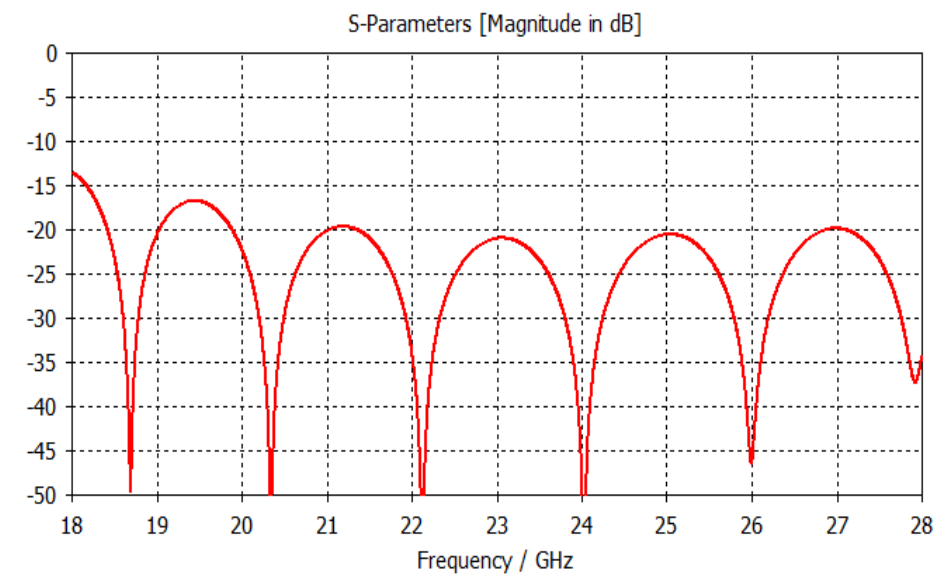


Fig 8. S₁₁ response of SIW to Stripline transition

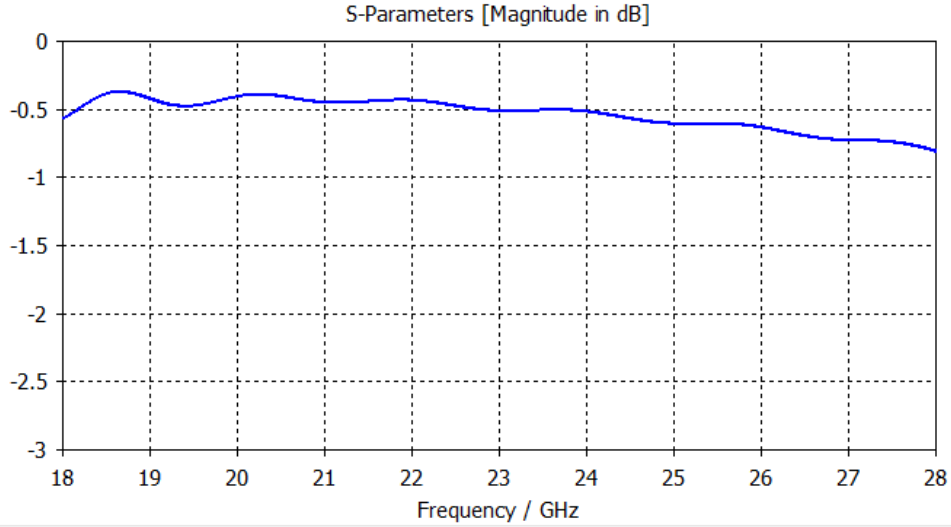


Fig 9. S21 response of SIW to Stripline transition

Figure 7 shows the SIW structure with stripline transitions. The chosen substrate is RT/Duroid 6002 with dielectric constant $\epsilon_r = 2.94$, height = 0.508 mm and metal thicknesses $t = 17.5 \mu\text{m}$. Table 1 has all the design parameters. Stripline width is chosen such that its characteristic impedance is 50Ω .

The top layer introduces the top ground plane of the stripline. The lower substrate contains the SIW top conductor and stripline center conductor. There is a taper very similar to the microstrip transition. The tapered feature facilitates conversion to stripline mode. The vias connecting top and bottom ground planes of the stripline help in suppressing unwanted modes waveguide and parallel plate modes [5].

Parameter	Value
SIW Width	6.71 mm
SIW Pitch	0.86 mm
SIW Diameter	0.62 mm
Stripline Width	0.63 mm
Taper Length	3.32 mm
Taper Width	2.83 mm
Stripline Pitch	0.44 mm
Stripline Diameter	0.31 mm

Table 1. Design parameters for SIW to Stripline transition

Figure 10 shows the top view of the transition with top dielectric hidden such that SIW and stripline center conductors are also visible. To observe the transition from waveguide to stripline mode we observe E field at 6 points along the length of the transition. Figure 11 (A) shows TE_{10} mode of operation in SIW. E fields are mostly confined in the lower dielectric slab. Upon entering the tapered region in figure 11 (B) E fields partially rotates and concentrates in the slot. More and more fields also start extending into the top substrate. Figure 11 (C), (D) show transition to TEM stripline mode. Finally in figure 11 (E) we observe that the transition to stripline mode is complete.

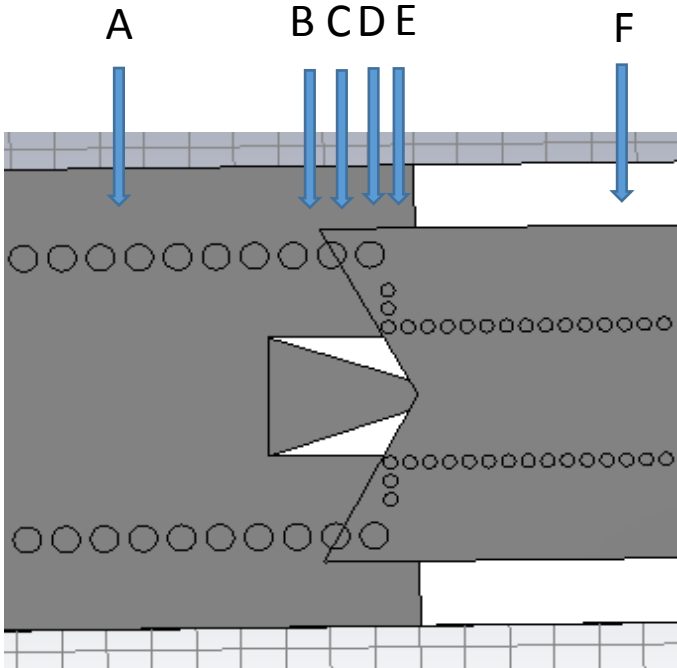
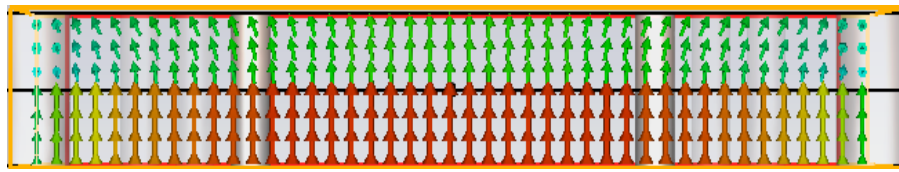
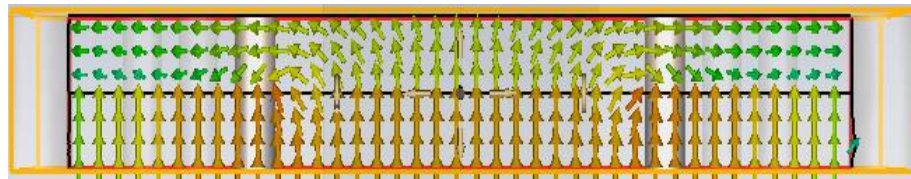


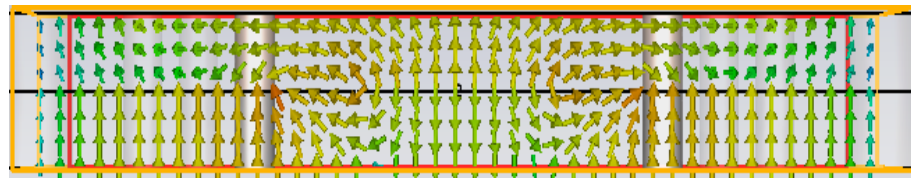
Fig 10. Top view of SIW to Stripline transition with top dielectric hidden



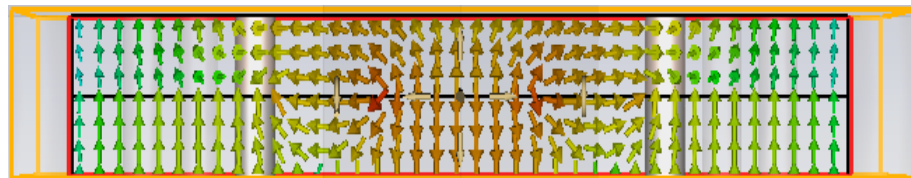
(A)



(B)



(C)



(D)



(E)



(F)

Fig 11. Electric field lines at various point along the length of the transition

CHAPTER 3

FILTER DESIGN

To design a filter using SIW Technology it is imperative to first design the filter at circuit level for a better understanding of the design. Using the circuit model a 3D model of the filter can be designed in CST. Such models are investigated using lumped and semi-lumped approach. Based on the available resources in the lab we decided to build the model for X-Band (8 – 12 GHz), but the design can easily be translated to higher frequencies.

3.1 Lumped Model

The response of an IRIS filter is very similar to lumped equal-ripple Chebyshev filter [6]. A Chebyshev filter is also called equal ripple filter. The following polynomial can be used to specify the insertion loss of N-order low-pass filter.

$$P_{LR} = 1 + k^2 T_N^2 \frac{W}{w_c}$$

Where $T_N(x)$ is a Chebyshev polynomial of order N which oscillates between ± 1 for $x \leq 1$. Thus k^2 determines passband ripple. Tables exist for design of equal-ripple low pass filter with normalized impedances and cut off frequency. These values can then be translated to the desired impedance and frequency. Finally a low-pass to bandpass transformation is done to get the desired frequency response. The following equations were used for the transformation. Here L_k 's and C_k 's are filter coefficients which can be found in the literature.

$$L_1 = L_k R_o / \Delta w_o$$

$$C_1 = \Delta / R_o L_k w_o$$

$$L_2 = \Delta R_o / w_o C_{k+1}$$

$$C_2 = C_{k+1} / R_o \Delta w_o$$

For this design we are using a 0.1 dB equal ripple Chebyshev Filter. The chosen bandwidth (Δ) is 10 % and impedance (R_o) of the waveguide is taken 443 Ω (Calculated using Linecalc tool in ADS). Figure 12 shows the designed lumped model filter. Figure 13 shows its frequency response where we can see 5 equal ripples corresponding to the 5th order filter.

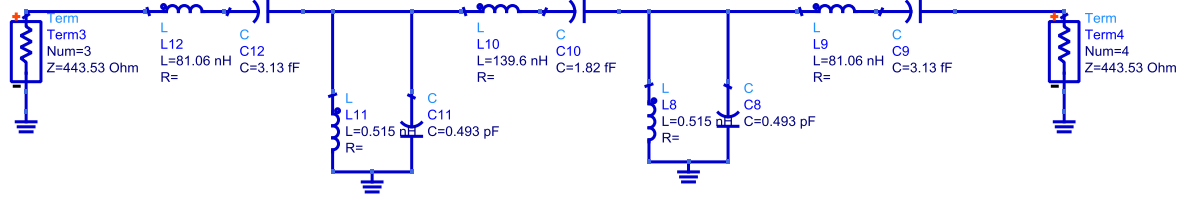


Fig 12. Lumped Equivalent of a Chebyshev Filter

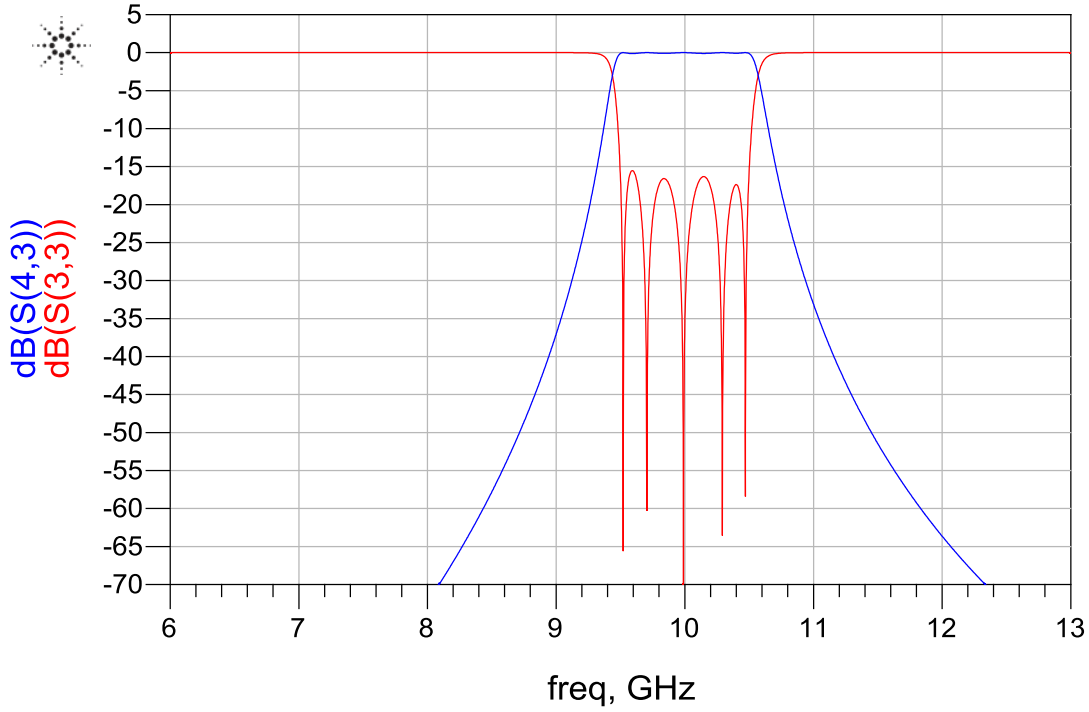


Fig 13. Frequency response of the designed 5th order Chebyshev Filter

3.2 Semi Lumped Model

The previous synthesis was a classical one which can be applied to any technology. For waveguides, filter synthesis based on impedance and admittance invertors is generally used. Considering the bandpass topology depicted in figure 12, such a topology can be transformed using impedance invertors. Hence, the modified prototypes are composed of six impedance invertors and five lumped elements. [6].

$$K_{01} = Z_{TE10} \sqrt{\frac{l_1}{g_0 g_1}}, \quad K_{56} = Z_{TE10} \sqrt{\frac{l_5}{g_5 g_6}}$$

$$K_{i,j+1} = Z_{TE10} \sqrt{\frac{l_i l_{i+1}}{g_i g_{i+1}}}$$

Where g_i 's are the Chebyshev coefficients, normalized inductances l_i 's are chosen arbitrarily, in this case we have chosen them all to be the same value.

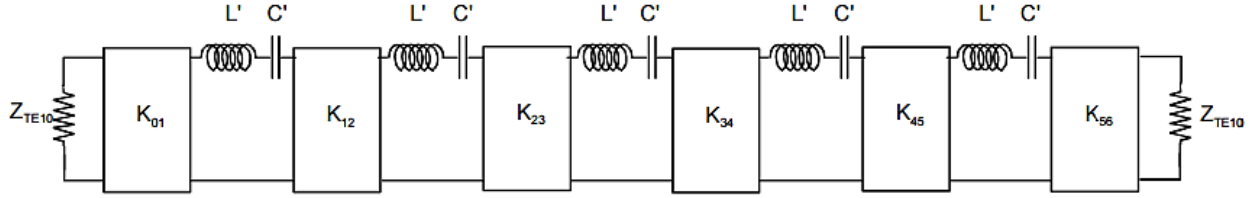


Fig 14. Bandpass filter prototype using impedance invertors

Technology implementation

The bandpass filter prototype with impedance invertors is composed of series L-C circuits. They behave like series resonant circuits. To get realistic fundamental mode impedance, slope parameters of the LC circuit and half wavelength transmission line are equalized. The normalized inductance value l_i is determined to be $\Delta\pi/2$.

It only remains to transform invertors into technology. Using the following transformation we can implement impedance invertors K using T-network based on shunt inductors and transmission line sections. The equivalence between the two can be verified by equating their ABCD matrices.

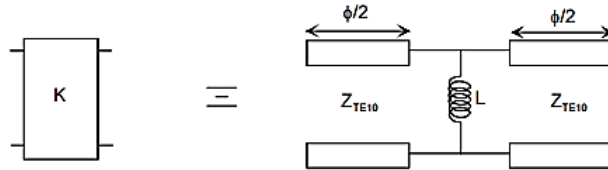


Fig 15. Technology implementation of an impedance inverter

$$K = Z_{TE10} \tan \frac{\phi}{2}$$

$$\phi = -\arctan \frac{2X_L}{Z_{TE10}}$$

$$\frac{X}{Z_{TE10}} = \frac{\frac{K}{Z_{TE10}}}{1 - \left(\frac{K}{Z_{TE10}}\right)^2}$$

Where ϕ is the corresponding transmission line length, X is the susceptance of the shunt inductor and Z_{TE10} is the impedance of transmission line segments. As a consequence inverters can be realized using inductive irises and additional transmission lines. L_{res} is the final length of the transmission line after absorbing the series L and C (shown in Fig 16) into the transmission line length.

$$L_{res_i} = \frac{\lambda_g}{2} \left(1 + \frac{\phi_{i-1,j} + \phi_{i,j+1}}{2\pi} \right)$$

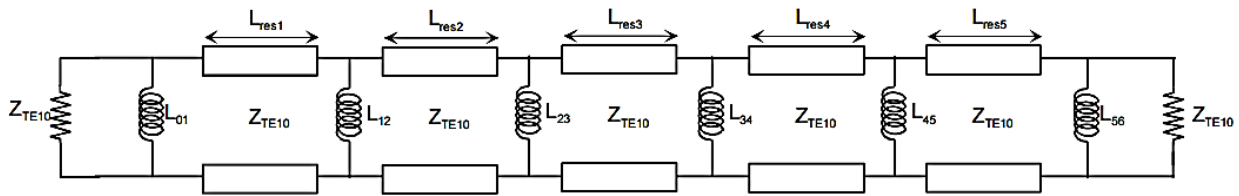


Fig 16. 5th order Bandpass filter network

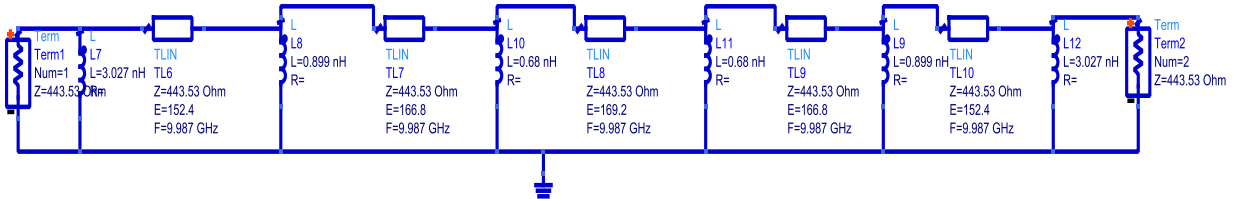


Fig 17. Equivalent Semi-Lumped model designed in ADS

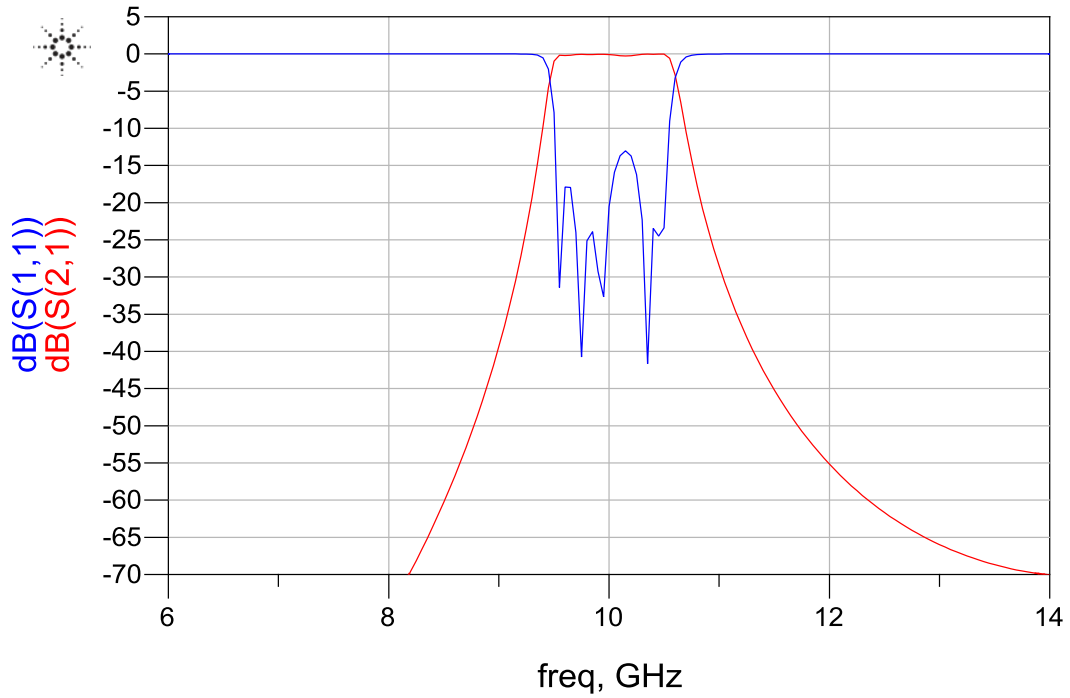


Fig 18. Frequency response of the extracted semi-lumped model

The equations given above were used to do hand calculations of K values which were then used to determine transmission line lengths and shunt inductor values. Figure 18 shows the frequency response of the designed semi-lumped model. This transmission line based model was translated to a 3D model in CST as described in chapter 4.

CHAPTER 4

DESIGN OF SIW FILTER IN CST

The design of the IRIS filter was built using already designed SIW cavity with microstrip ends as shown in Figure 2. The electrical lengths calculated in section 3.2 were used to determine the spacing between each IRIS. The IRIS aperture width can be approximated by considering each via to be an inductor in parallel. The total shunt inductance will be the effective inductance of all the inductors in parallel. The IRIS aperture controls the bandwidth of the filter and the central frequency is primarily controlled by the transmission line lengths.

The calculated values had to be fine-tuned to get the central frequency and bandwidth. Parametric sweeps were done on each parameter to get the desired response. Figure 19 shows the structure of the IRIS filter with each parameter marked. The substrate used is Rogers 5880 of thickness 0.508 mm. Table 2 tabulates the tuned parameter values. Figure 20 shows the S21 response of the filter with desired bandwidth. The central frequency needs to be tuned further to get it closer to 10GHz.

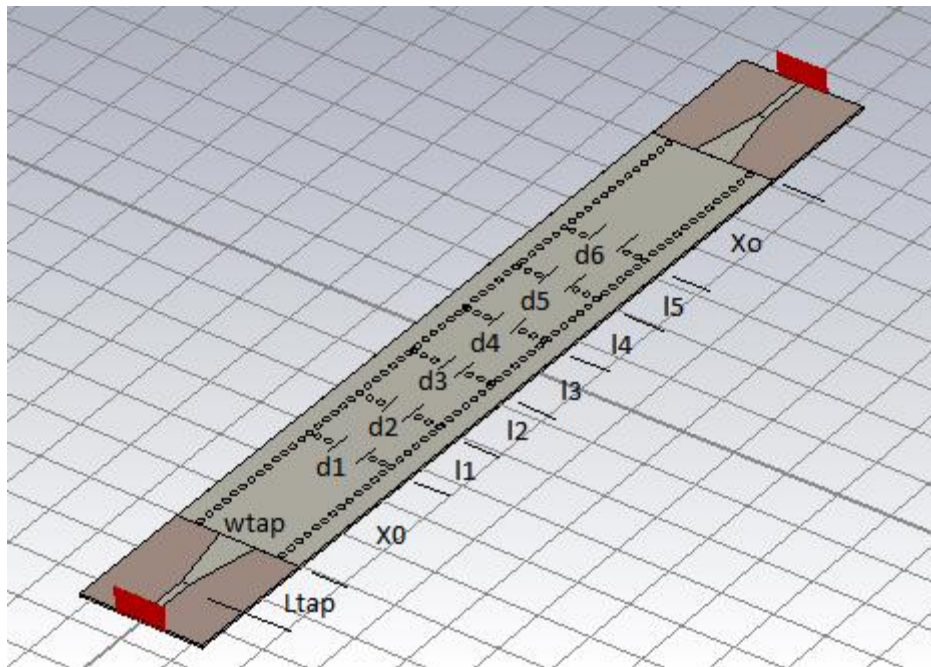


Fig 19. CST simulation of the designed SIW Filter

Parameter	Value	Parameter	Value
Via Pitch (p_v)	2.1 mm	d1	7.9 mm
Via Diameter (d_v)	1.2 mm	d2	6 mm
SIW Width (a_{siw})	15 mm	d3	5.5 mm
Microstrip width (w _{tap})	6 mm	l1	11.9 mm
Microstrip length (w _{tap})	14 mm	l2	12.95 mm
X0	16.75 mm	l3	13.2 mm

Table 2. Design parameters for the SIW filter

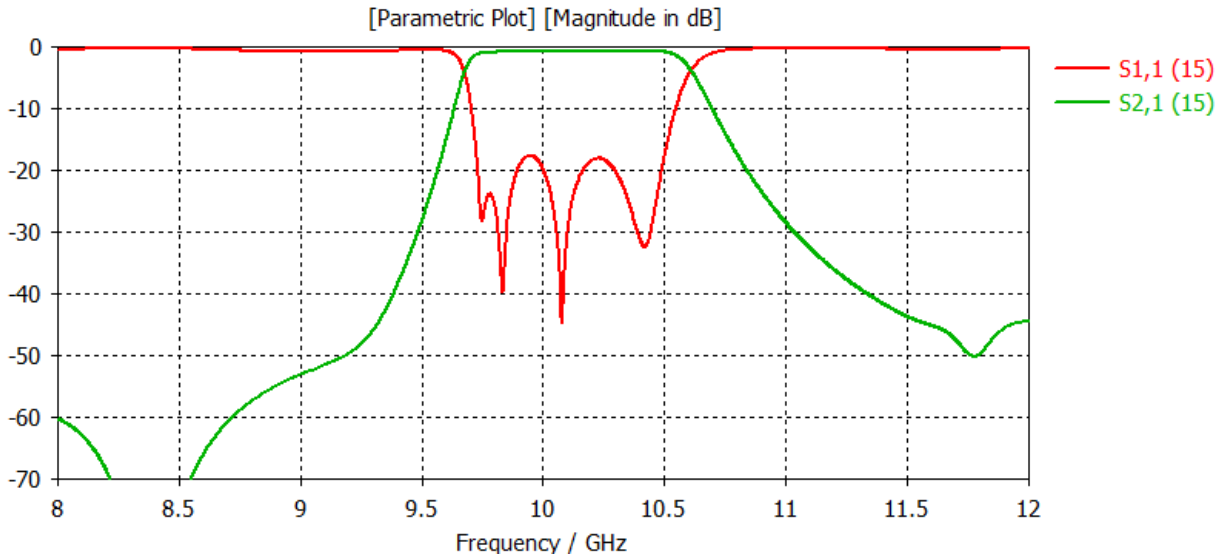


Fig 20. S21 response of the Filter Designed in CST at X Band

Design of 60GHz SIW filter

As a proof of concept a 5th order IRIS bandpass filter is also designed at 60 GHz. The design procedure is very similar to the one already discussed for 10 GHz filter. The design parameters are tabulated in Table 3. Figure 21 and 22 show the structure and the frequency response respectively. The design goal in this case was central frequency of 60 GHz and bandwidth of 1 GHz [1].

Parameter	Value
Pitch Via (p_v)	0.35 mm

Via Diameter (d_v)	0.2 mm
SIW Width (a_{siw})	2.8 mm
SIW Effective Width (a_{eff})	2.678 mm
Substrate (Rogers 5880)	0.508 mm

Table 3. Design Parameters for the filter designed at 60GHz

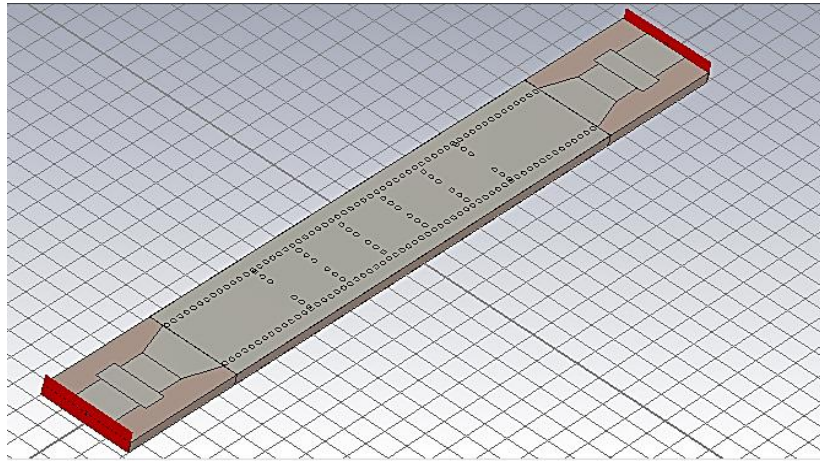


Fig 21. CST Schematic of the 5th order SIW Filter with microstrip transitions on both ends

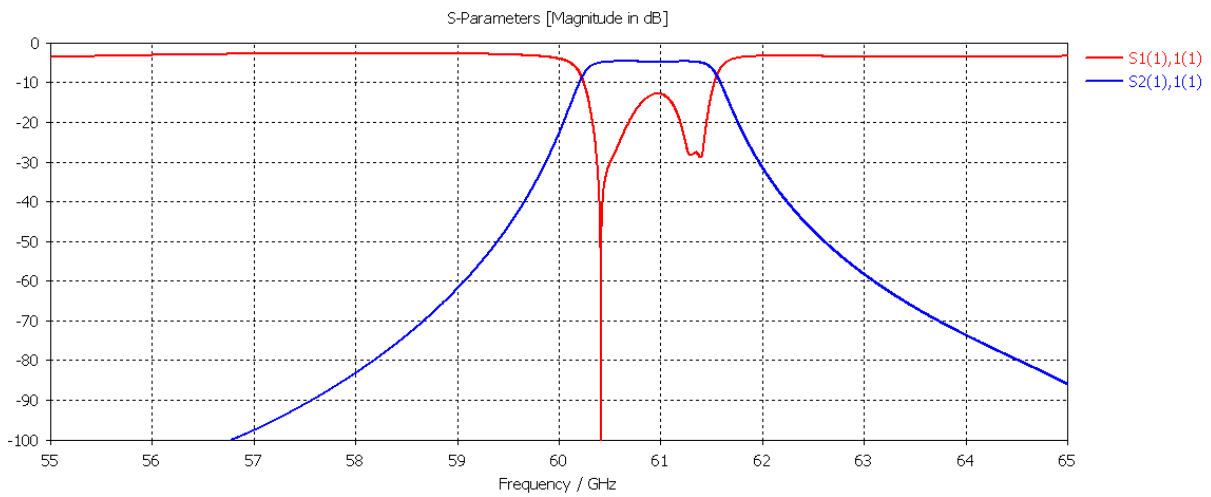


Fig 22. Frequency response of the designed filter at 60 GHz

CHAPTER 5

ACTIVE FILTERING WITH GUNN DIODES

The designed SIW filter when integrated with an active element like a Gunn diode can be used to compensate for insertion loss. The active element needed to compensate for losses is placed in the center of the filter. It can be characterized by complex admittance $Y=G+jB$. The resulting transmission matrix A^{res} is defined as follows [7]:

$$A^{res} = A_{in} * A_Y * A_{out}$$

Where A_{in} is the first half of the filter, A_Y is the ABCD matrix of the Gunn diode & A_{out} is the second half of the filter.

5.1 Matlab Simulation using ABCD Matrices

The extracted semi-lumped model (figure 17) comprises of transmission line segments and shunt inductors. A_{tx} is the ABCD matrix of a transmission lines segment and A_L is the ABCD matrix of shunt inductor. Using the ABCD Matrices of individual elements and cascading them together we can calculate A_{in} . Since the filter is symmetric A_{in} is equal to A_{out} .

$$A_{tx} = \begin{bmatrix} \cos \theta & jZ_o \sin \theta \\ \frac{j \sin \theta}{Z_o} & \cos \theta \end{bmatrix}, \quad A_L = \begin{bmatrix} 1 & 0 \\ \frac{1}{j\omega_o L} & 1 \end{bmatrix}$$

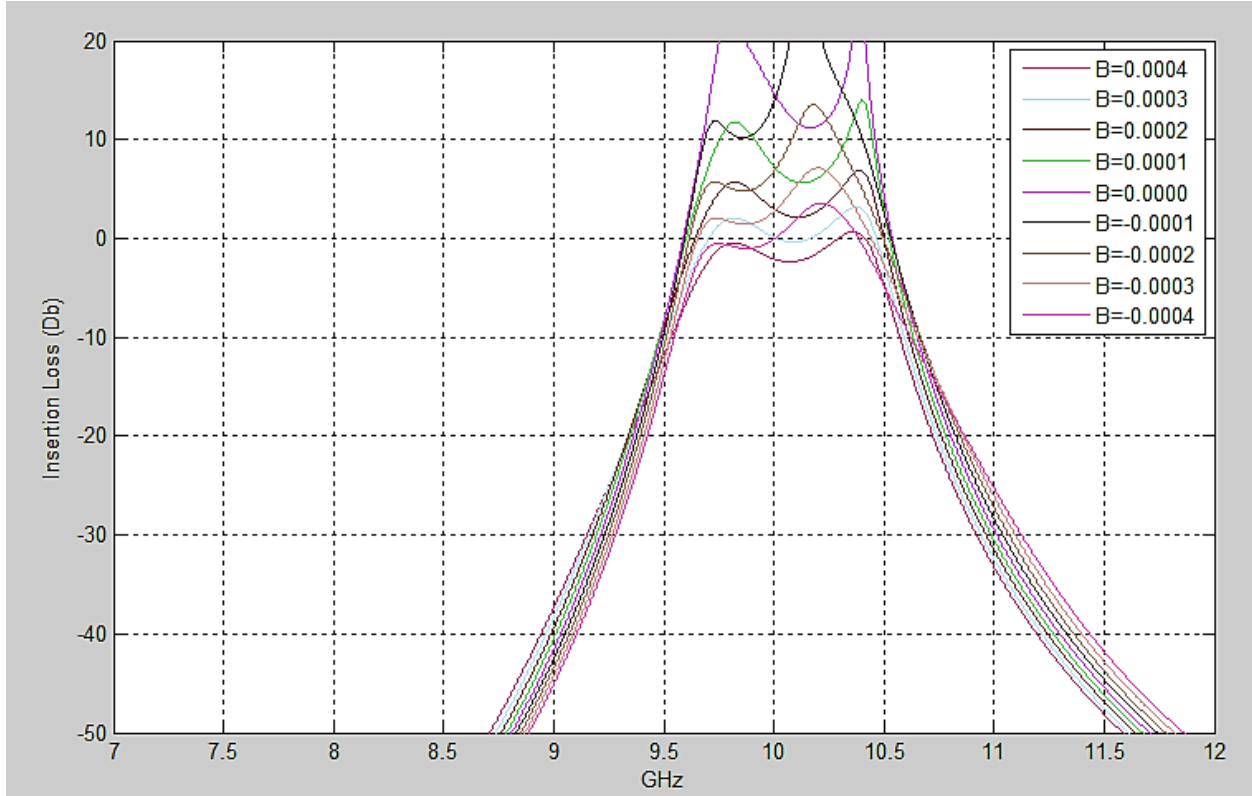


Fig 23. Matlab plot of insertion loss vs frequency with $G=-0.0004$ and varying B from: -0.0004 to $+0.0004$

$$A_Y = \begin{bmatrix} 1 & 0 \\ G + jB & 1 \end{bmatrix}$$

A_Y is the ABCD matrix for shunt negative impedance. ABCD matrix can easily be converted to S parameters using the following formula [8]. Figure 11 shows a Matlab plot of S11 in dB swept across 7-12 GHz frequency range using different values of G & B . We can see that by carefully choosing the value of G & B we can find a combinations with above 0 dB loss.

$$S_{21} = \frac{2Z_0}{AZ_0 + B + CZ_0^2 + DZ_0}$$

5.2.1 Modeling of Gunn Diodes

Gunn Diodes are two terminal ‘transferred-electron’ devices which are finding increasing application as a basic ‘low noise’ active component in the design of microwave circuits. The most general model of a Gunn Diode consists of a non-linear resistor, a non-linear current source and two capacitors. The element parameters are defined as follows [9,10]:

- 1) Cathode to Anode capacitance: $C1 = \xi A/L$, where L and A are length and cross sectional area of the device.

- 2) Domain Capacitance : $C_2 = \xi A/W$, where W is the width of the domain.
- 3) Nonlinear Resistor R : $I_R = G(V_R) = Aq n_0 v(V_R/L)$, where q is the charge of an electron, n_0 is the donor concentration and $v()$ is the velocity vs field characteristic.
- 4) Nonlinear controlled current source $I_D(v_1, v_2) = C_2 \int_{v_1/L}^{E_m} \left[v\left(\frac{v_1}{L}\right) - v(E) \right] dE$, where v_1 and v_2 are instantaneous voltages on capacitors C_1 and C_2 and E_m is the maximum electric field in the domain.

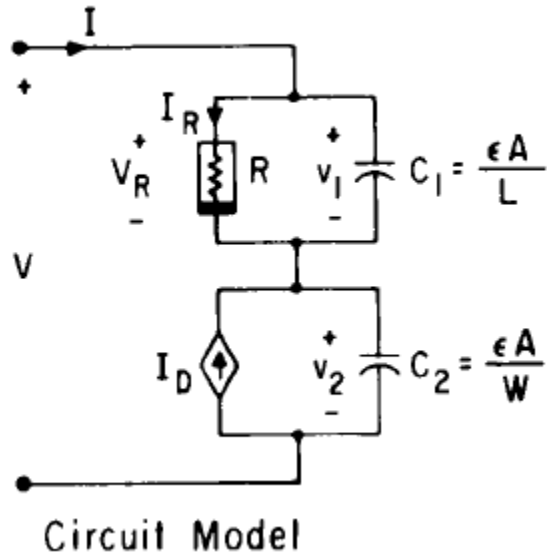


Fig 24. Schematic of a nonlinear model for Gunn Diode

Modelling of nonlinear resistor in ADS:

$$I_R = 1.6 \times 10^{-11} \times \left\{ \frac{8 \times 10^6 V_R + 3.125 \times 10^4 V_R^4}{1 + 3.9 \times 10^{-3} V_R^4} \right\}$$

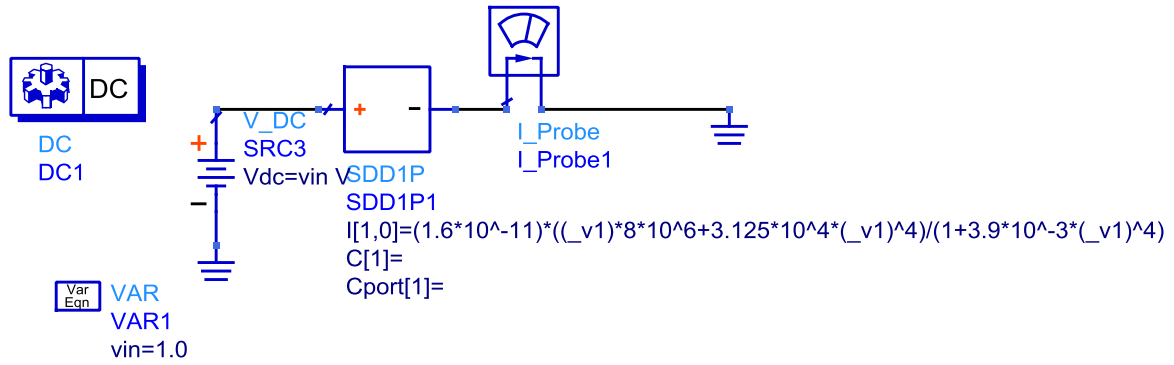


Fig 25. ADS Schematic of the nonlinear resistor

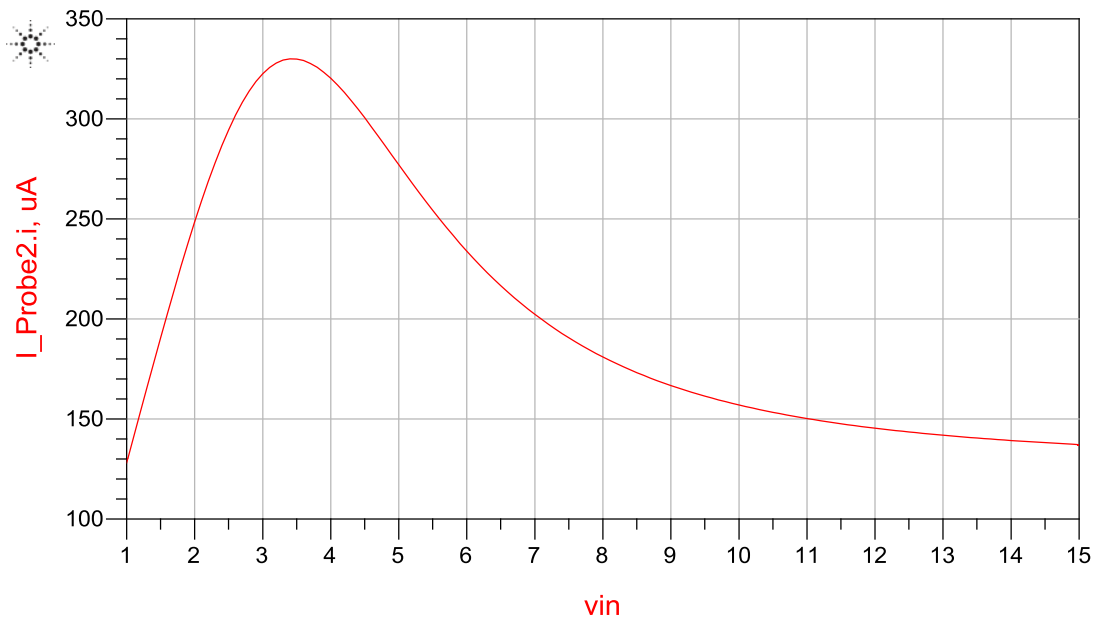


Fig 26. DC sweep of voltage applied across the nonlinear resistor and the current flowing through the resistor

5.2.2 Alternative Approach

The nonlinear current source shown in figure 24 is difficult to model in ADS due to involved integrals. Alternately Gunn diodes can also be simulated using complimentary JFETs and a PN junction diode [11]. Figure 27 shows a spice model of Gunn diode using the same approach.

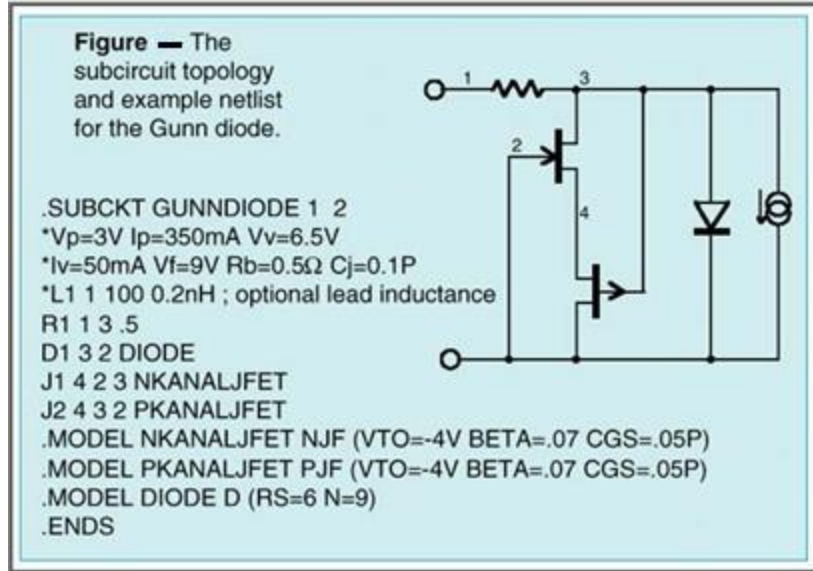


Fig 27. Spice Model of Gunn Diode using JFETs

We used ADS to construct a JFET based model of Gunn diode. Figure 28 shows the designed model. The IV characteristics obtained by DC analysis is shown in figure 29. The IV curve shows negative resistance for applied DC voltage between 3-6 V.

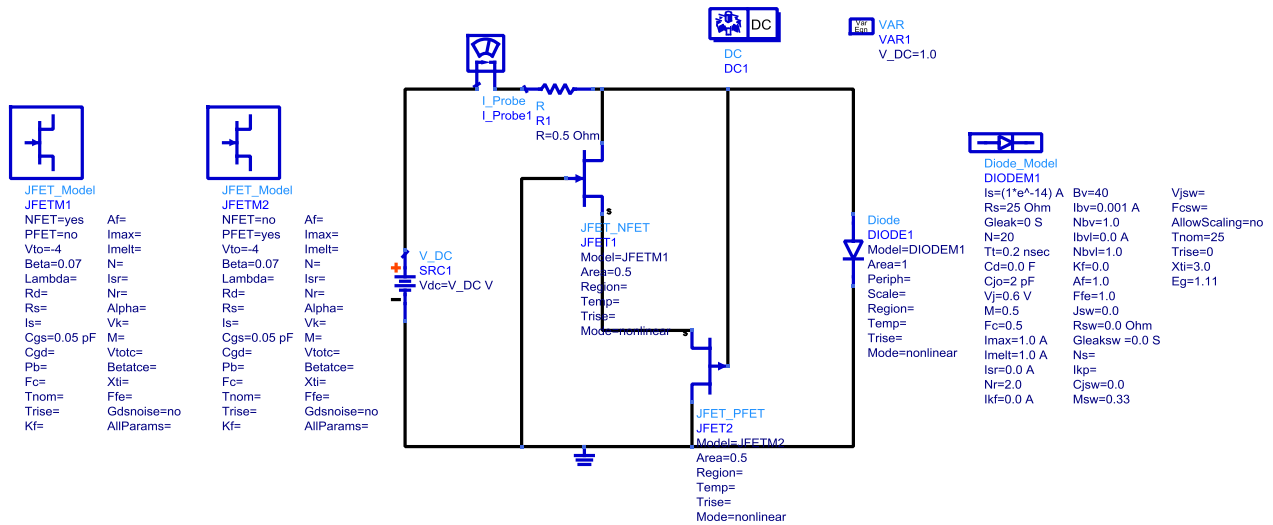


Fig 28. Schematic of Gunn Diode model designed in ADS

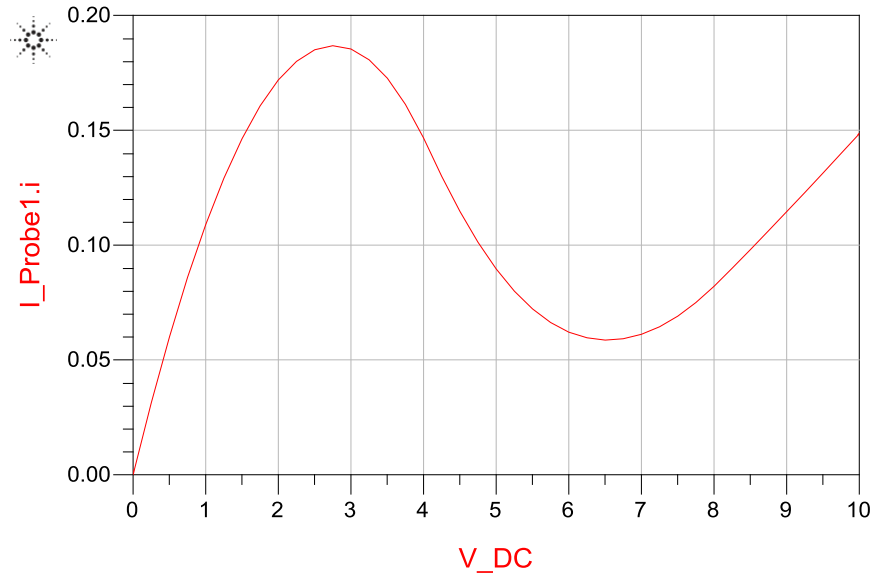


Fig 29. I-V characteristics of the Gunn Diode model

5.2.3 Simulation of Gunn Diode with Semi-lumped filter

Models of both Gunn diode and filter have been realized in ADS. In this section we integrate them to observe above 0 dB insertion loss. The Gunn diode is biased at 5V corresponding to its negative resistance region. In figure 30 a DC block and an AC short is placed to ensure the DC signal only goes through the Gunn diode and to block any DC signal going to the filter.

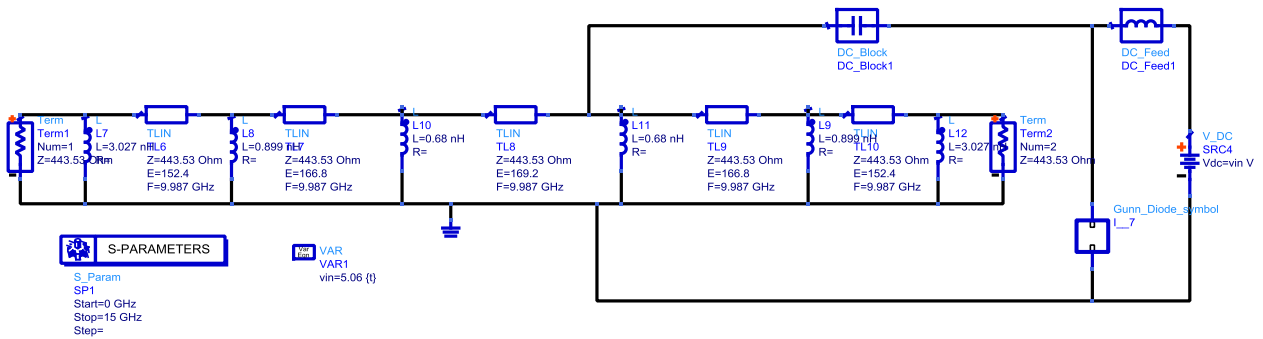


Fig 30. ADS Schematic of Gunn Diode simulated with semi-lumped model of SIW Filter

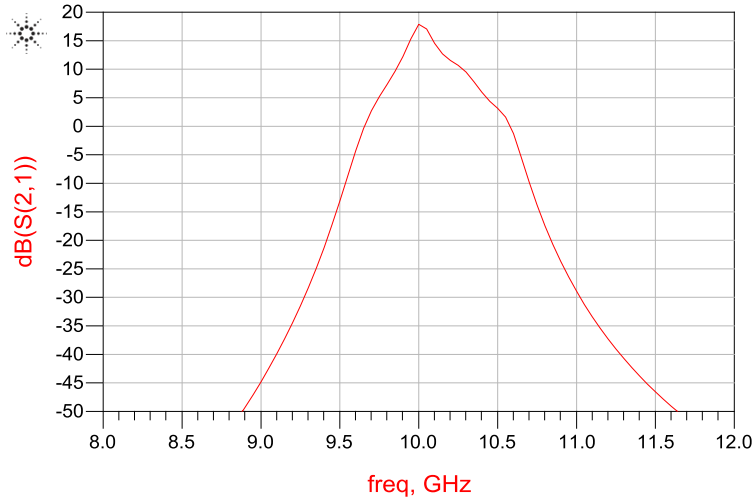


Fig 31. S Parameter response of the Active Filter at 5V bias

The result obtained by the small signal analysis shows above 0 dB insertion loss. We can achieve the desired level of active filtering by tweaking JFET models and PN junction diode models. In this simulation these models were constructed based on parameters provided by Keysight on their website.

5.3 Alternative approach using PHEMTs

This approach uses a common gate stage at the input and common drain stage at the output of the filter. The first and last sections act respectively as input and output matching networks. P-HEMT active devices in common gate and common drain configurations have been used to achieve wide-band matching, gain performance and improve selectivity [12].

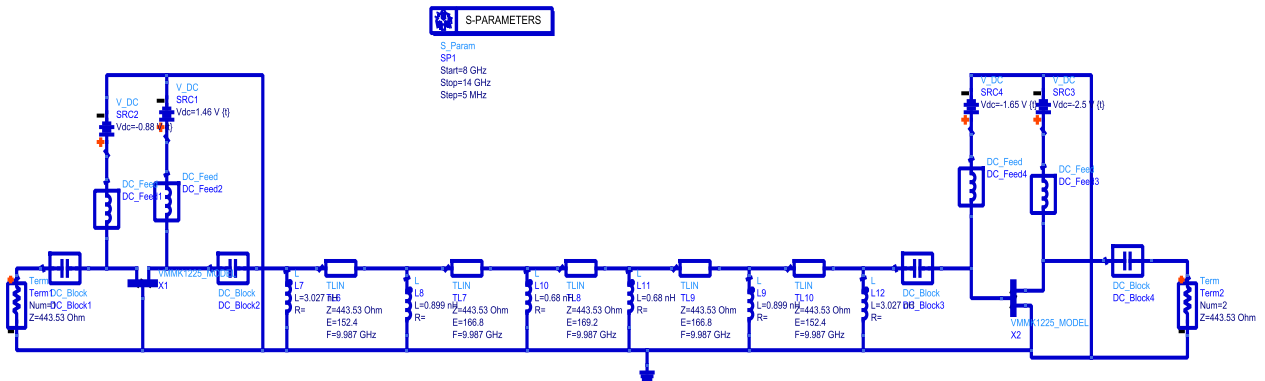


Fig 32. ADS schematic of PHEMTs incorporated at the input and output of SIW filter model

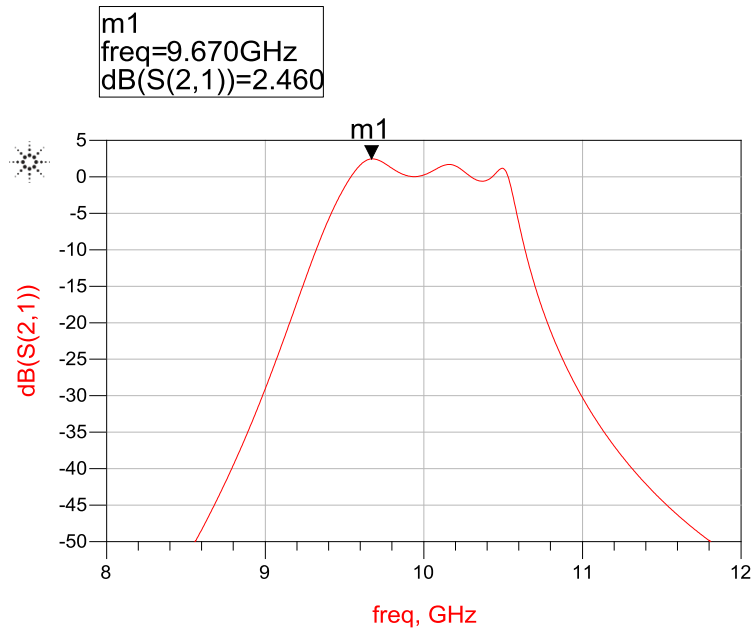


Fig 33. S parameter response of the SIW filter with PHEMTs

The filter is realized using P HEMT VMMK 1225 from Avago Technologies. Both the transistors are identically biased at $V_{gs} = 0.85$ V and $V_{ds} = 2.4$ V. Figure shows about +2dB insertion loss in this case. This simulation has been done as a proof of concept and both the transistors used have the same size. If we choose transistor with different sizes at the input and the output we can achieve better S21 response.

CHAPTER 6

FABRICATION AND MEASUREMENT

Using the extracted design parameters shown in Table 2 SIW filter was fabricated in the lab. The design was exported from CST in gerber format and printed on transparencies which served as a mask for photolithography. Photolithography was carried out on the top metal layer using a positive photoresist.

6.1 Fabrication

Following are the steps involved:

- Cut out Rogers 5880 substrate with dimensions slightly bigger than the filter
- Place the substrate on the spinner
- Using a pipette pour small amount of photoresist (PR) on the substrate
- Spin at 2000 rpm for 40 seconds
- Soft bake at 110 °C for 30 seconds
- Using the printed transparencies as a mask expose the photoresist side for 80 seconds
- Hard bake at 110 °C for 60 seconds
- Develop in AZ 300 MIF for 30 seconds
- Rinse with deionized water (DI)
- Place in ferric chloride solution for 30 mins
- Rinse with DI and strip PR using acetone



Fig 34. Photograph of the Rogers substrate with patterned top metal layer

The patterned top metal layer of Rogers 5880 is shown in figure 34. Next step was to add metallized vias. The gerber files generated from CST were used to create drill file in ADS. The drill file was then loaded into LPKF tool which was used to drill holes in the substrate. The major challenge here was to get the perfect alignment since the tool has no built in alignment method. Once the alignment is complete the tool reads the drill file to drill holes in an automated fashion.

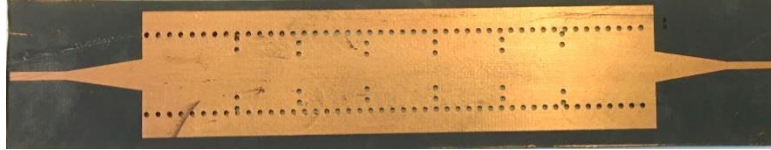


Fig 35. Photograph of the structure with drilled via holes using LPKF tool

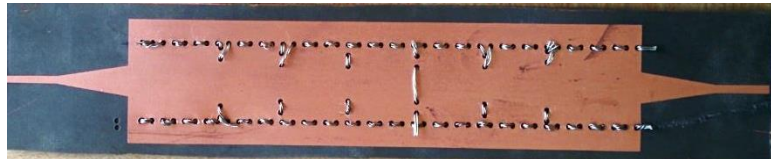


Fig 36. Photograph of the structure with braided wire threaded through the vias

The drilled holes needed to be metallized in the next step. Several methods were tried to achieve this. The method that worked the best was to thread the vias with braided metal wire and then add solder to the remaining air gaps. After all the vias are filled, the structure needs to be cleaned using isopropyl alcohol to get rid of the flux. SMA connectors are soldered at the ends for doing measurements.



Fig 37. Photograph of the fabricated SIW filter

6.2 Measurements

S parameter measurements were done on the fabricated filter using Vector Network Analyzer. Figure 38 shows the measured result. There are ripples in the return loss which are caused by connectors and cable lengths. Insertion loss is a lot higher than expected due to fabrication tolerances. Also, the in-house method of metallizing vias isn't ideal.

An alternative approach could be to use rods instead of braided wire to fill the vias. Since the chosen substrate was really thin (0.508 mm) doing this was challenging. In future designs thicker version of Rogers 5880 could be used.

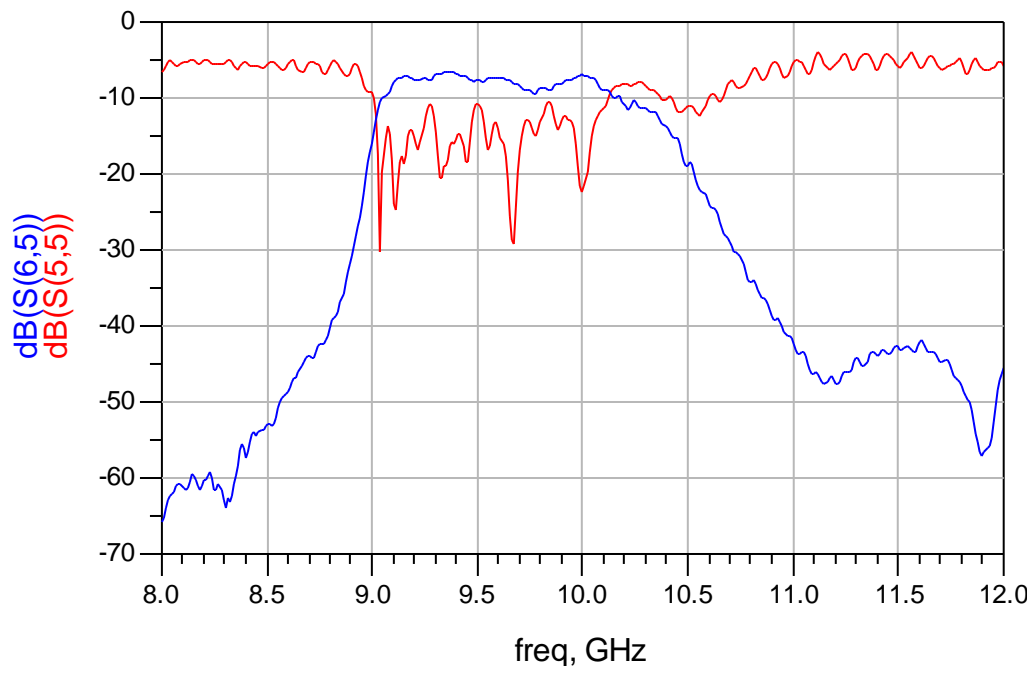


Fig 38. S parameter response of the fabricated SIW filter

CHAPTER 7

SIW CAVITY DESIGN

High Q resonant cavities can be built using SIW. These high Q cavities can be exploited for building oscillators with low phase noise. The cavity topology shown in figure 39 has two functions, one of a frequency selector and the other of a coupling device for positive feedback. The diameter and pitch of the vias are such that no radiation loss happens at the desired frequency. The following equations provide a good approximate of the length and width of the cavity [13].

$$F_{R(TE_{m0q})} = \frac{c_o}{2\sqrt{\epsilon_r}} \sqrt{\left(\frac{m}{W_{eff}}\right)^2 + \left(\frac{q}{L_{eff}}\right)^2}$$

where

$$L_{eff} = L - \frac{d_v^2}{0.95 \cdot p_v}, \quad W_{eff} = W - \frac{d_v^2}{0.95 \cdot p_v}$$

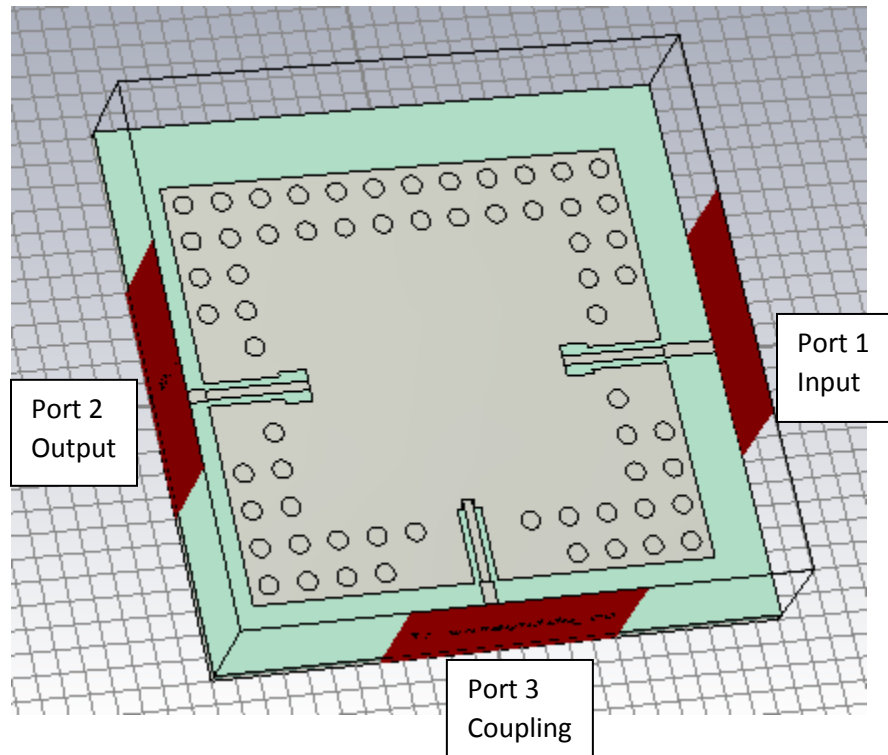


Fig 39. SIW cavity designed to resonate at 10 GHz

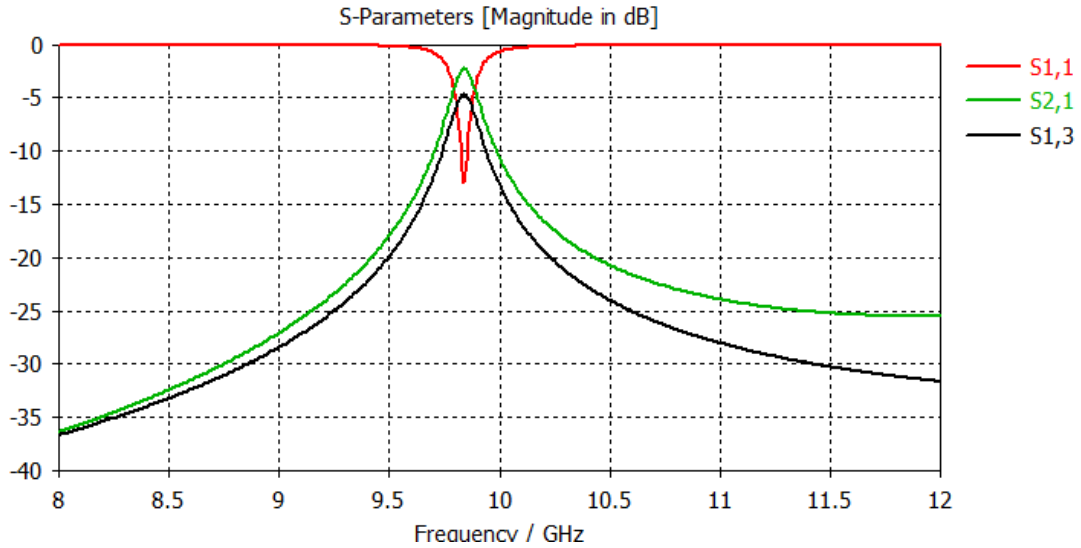


Fig 40. S parameter response of the SIW cavity

As shown in figure 41 current probes are used to connect cavity to microstrip lines. These are short circuited sections of coplanar waveguides. The length and width of the ends determine the level of coupling. The three probes are namely Input port, Output port and Coupling port.

If the designed cavity is combined with a small signal amplifier in a feedback fashion we can achieve oscillations. The coupling level of feedback port needs to be adjusted such that the loop gain is slightly higher than 1 dB to take into account the losses in the amplifier. The loop length needs to be adjusted such that there is a total 0 degree phase shift in the entire loop [13].

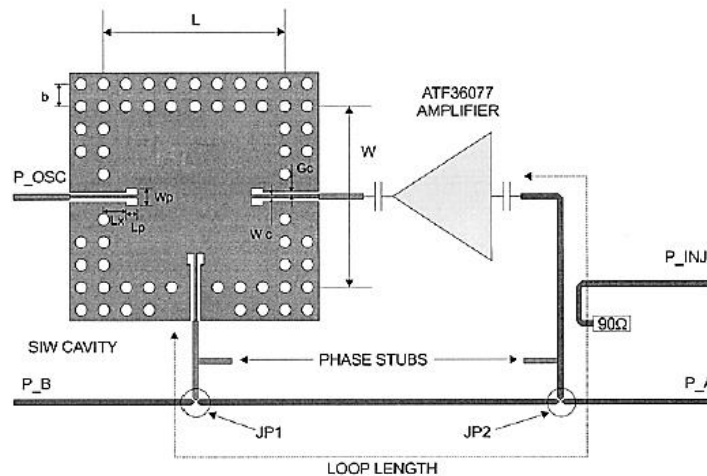


Fig 41. Topology of the SIW feedback oscillator [13]

CHAPTER 8

CONCLUSION AND FUTURE DIRECTION

8.1 Results

In this work we have successfully designed filter models using two different approaches. One with classical lumped elements and another using a more realistic transmission line based model. These models were then used to build a 3D model in CST.

In the second half of the project two different ways of doing active filtering were explored. Above 0 dB loss was observed in both cases. The first case uses a basic Gunn diode which is relatively inexpensive. The other approach uses two PHEMTS which could be more expensive and difficult to bias. In conclusion both the demonstrated approaches are practical but using Gunn diode might be a more viable option.

8.2 Future Direction

The next steps would be to improve the fabrication technique to achieve filtering with less insertion loss. Also, there are readily available Gunn diodes in the market which can be used to demonstrate the active filtering idea experimentally. Lab equipments required to perform this measurement are Vector Network Analyzer, DC source, bias T and circulator.

In future this SIW filter can be integrated with oscillator to get better phase noise performance without any loss. An entire system can also be built using SIW approach. There are a number of papers on SIW cavity oscillators, SIW antennas etc. Such a system can be very efficient at mm wave frequencies and their planarity would be great for integration.

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