

Performance of the New Vertex Detector at SLD¹

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Abstract

During the past year, the SLD collaboration completed the construction and began the operation of a new vertex detector (VXD3) employing 307 million pixels. This detector, based on 96 CCDs of 13 cm² area each, is an upgrade of the original vertex detector of SLD (VXD2), made possible by advances in the technology of CCD detectors. Its improved impact parameter resolution, larger solid angle coverage and virtually error-free track linking will enhance the SLD measurement of the polarization-enhanced forward-backward asymmetry for b- and c- quarks, increase the precision of the measurement of the b-fraction in hadronic Z decays, and open the possibility to observe B_s^0 -mixing. Full separation of primary, secondary and tertiary vertices is accessible. A description of the mechanics and electronics of VXD3 are presented along with results from the first data.

I. INTRODUCTION

The SLD (SLC Large Detector) experiment studies the nature of elementary particles using highly polarized weak neutral bosons, Z^0 s, which are produced by SLC (SLAC Linear Collider). The original SLD pixel vertex detector VXD2[1], placed close to the e^+e^- intersection point (IP), in conjunction with small and stable SLC beam spots, has provided SLD with excellent flavor-tagging for three years, and validated the suitability of a CCD-based pixel vertex detector.

The upgrade to the 307 Mpixel VXD3[2], completed in December 1995, has significantly improved performance, and opened new, exciting possibilities for physics at SLD. Improved impact parameter resolution, increased solid angle coverage and reliable track linking will boost the SLD ability to make a world-class measurement of the forward-backward asymmetry (A_{FB}) for the b- and c- quarks, and will improve the precision in the measurement of the b-fraction in hadronic Z decays. A wide range of measurements can be made which will make use of full separation of the primary, secondary and tertiary vertices. One of the most exciting possibilities is

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the search for B_s^0 mixing, leading to the measurement of the mixing parameter, x_s .

These improvements have been achieved by the changes in the detector design discussed below. The first SLD run with VXD3 ended in July 1996. Final understanding of the performance of the vertex detector may be achieved only after completion of a comprehensive data analysis, which we expect by the spring of 1997. However, we already can see that the operational parameters of VXD3 are close to the expected values. This first run revealed a few unanticipated problems, which were either corrected before the run, or are being corrected for the next run. Physics quality data were obtained and represent an improvement over VXD2.

II. VXD3 DETECTOR DESIGN AND COMPARISON WITH VXD2

A. Geometry and Material

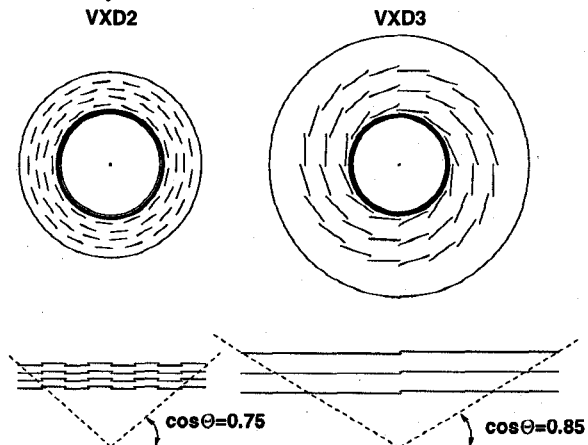


Fig. 1 Comparison of VXD2 and VXD3 geometries.

Figure 1 shows the difference in the geometries of VXD2 and VXD3. The inner beampipe radius of VXD2 (25 mm) is reduced to 23.2 mm to achieve better impact parameter resolution and polar angle coverage. VXD2 provided only 2-hit coverage for most of the azimuth, with only 30% of tracks having 3 or more hits, and polar angle coverage only up to

$|\cos\theta| = 0.75$ (ladder active length 92.3 mm).

The development of large area CCDs[3], allows a simplified ladder design, with only 2 CCDs covering the entire 159 mm length of the ladder. Polar angle coverage for 3 hits matches the central drift chamber (CDC) coverage of $|\cos\theta|_{max} = 0.85$. Deterioration of spatial resolution at small polar angles is not an issue thanks to very thin active EPI silicon layer of $20\mu\text{m}$ on CCDs.

The beryllium motherboard stiffener and thinned CCDs, to $150\mu\text{m}$, reduce the radiation length thickness for a VXD3 ladder to 0.4% (compare to 1.15% for VXD2 ladder). The thickness of the titanium liner ($100\mu\text{m}$ for VXD2) was reduced by a factor of 2, since the very soft photons do not make a large contribution to the background. The reduction in the beryllium beampipe thickness from 1.0 mm to 0.75 mm is mechanically acceptable, and further reduces the multiple scattering. These changes improved the impact parameter resolutions as shown in figure 2.

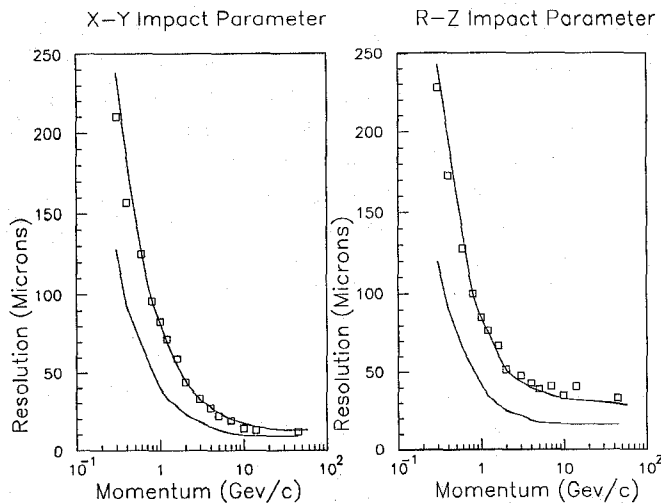


Fig. 2 Comparison of VXD2 and VXD3 impact parameter resolutions. The boxes are from data with VXD2. The lower curves are the expected improvement with VXD3.

The "shingled" structure between ladders in all 3 layers of VXD3 gives uniform 3-hit coverage for full azimuth range, reduces the average inner hit radii and corrects the problem of large lever-arm variation with azimuth in VXD2. The VXD3 layout is such that in case one hit is lost, the resulting lever-arm is still better than that achievable with fully efficient VXD2. These improvements result in an expected VXD3 impact parameter resolution parametrized in equation 1.

$$\sigma_{xy}(\mu\text{m}) = 9\oplus \frac{29}{p \sin^{3/2} \theta}; \quad \sigma_{rz}(\mu\text{m}) = 14\oplus \frac{29}{p \sin^{3/2} \theta} \quad (1)$$

B. Mechanical Structure

The physical dimension of a CCD is $82.4 \times 16.6 \times 0.15 \text{mm}^3$. Two CCDs are assembled onto a polyimide/beryllium sandwich to form a ladder; one CCD is mounted on the inner side of the ladder, and one on the outer side. CCDs have about 1mm of overlap, forming an active area of $159 \text{mm} \times 16 \text{mm}$. 48

ladders are arranged in three coaxial cylindrical layers, located at nominal radii of 28.0mm, 38.1mm and 48.3mm around the beam pipe.

The vertex detector is supported by a structure made from instrument grade beryllium. The beryllium components are match pinned and doweled to achieve the stable environment. Mating surfaces are lapped with $1\mu\text{m}$ precision. The CCD ladders are supported at each end via beryllium rings mounted to the inner faces of endplates. All joints between dissimilar materials are designed to allow for thermal contraction variation during cool-down. This support structure follows the previous VXD2 design, with some improvements.

The vertex detector operates at cryogenic temperature (-50°C to -90°C) in order to completely suppress any loss of charge transfer inefficiency from radiation damage. Liquid nitrogen boiloff gas is piped through a beryllium jacket surrounding the beryllium beampipe. Fine holes allow gas to flow out through the outer jacket into the detector cryostat, creating a uniform flow of gas from the innermost to outermost barrel of the detector.

The vertex detector was surveyed with the OMIS II coordinate measuring machine. Every ladder was surveyed individually before assembly, and each barrel was surveyed following assembly to a few micron precision. After installation, the vertex detector position with respect to the central drift chamber is monitored by a system employing a capacitive readout.

C. Electronics and Readout

The CCDs are n-buried channel devices fabricated on ptype epitaxial layer and having a p+ substrate. They have an active area $80 \text{mm} \times 16 \text{mm}$. They are operated in fullframe readout mode. The substrate resistivity is specified to be less than $20 \times 10^3 \text{ohm} \times \text{cm}$ to maintain short carrier lifetimes. The epitaxial layer is 18-22 microns thick with a resistivity of $20 \text{ohm} \times \text{cm}$ for adequate diffusion length, optimal diffusion/drift ratio, and clean high rate clocking. The pixel sizes are $20\mu\text{m} \times 20\mu\text{m}$. The readout register operates on two-phase clocking, and the imaging area on three-phase. There are 4 readout nodes, one on each corner of the device, with 800,000 pixels (2000 rows of 400 pixels) per node.

The readout system for VXD3 represents a significant advance over that of VXD2. The pixel readout rate is 5MHz (cf. 2MHz for VXD2), so despite the increased pixel quantity, no degradation in system readout time has been necessary. Advances in electronics permit much more compact drive and readout circuitry. Most control and signal processing circuitry has been moved inside the SLD detector, eliminating most of the cable plant and simplifying commissioning and operation. The readout electronics consist of 16 analog-to-digital (A/D) boards, placed close to the CCDs, and connected with high speed optical links to FASTBUS data acquisition modules. These modules are modifications of Vertex Data Acquisition modules (VDA), used in VXD2. These new modules have been named by their designer Last Fastbus Modules (LFM).

A/D boards also have all necessary circuitry to generate CCD clocks and biases. Every A/D board has 24 channels of

amplifiers with a gain of 100 and 24 8-bit flash ADCs, serving 6 CCDs. Digitized signals are organized into serial data stream using multiplexers based on XILINX programmable gate arrays[4], and are transmitted via 1.2GHz optical data link, using the Hewlett-Packard gigabit rate transmitter chip and Finisar optical transmitter[5]. Every board also contains a Motorola M68HC11 microcontroller, which is used to download the XILINX code, CCD image clocks waveforms, DC offsets for amplifiers, ADC gate delay and CCD enable-disable signals (to be able to disconnect defective CCDs from bias and clock sources). The A/D board has 3 modes of operation - initialization, run and calibration, which are also controlled by this microcontroller. In the calibration mode pulses of known amplitudes are generated on the A/D board and are fed to the CCD outputs through node reset circuits, so the entire signal path may be checked and calibrated. The microcontrollers on A/D boards are functional only during initialization mode, which is automatically entered after power-on, or on demand to change any settings. During data readout microcontrollers clocks are off, to reduce the possibility of noise increase due to crosstalk to amplifier inputs. During readout all functionality of the A/D board is provided by the fast logic sequencer, a device based on the AMD fast programmable logic MACH220 chip[6].

The main function of LFM modules is to reduce the 307 Mbytes of raw data to a manageable size (about 100 Kbytes), and transfer this data to data acquisition system. The data size reduction is achieved by hardware reconstructing 2-d clusters of charge deposition and imposing a threshold, which gives > 99% efficiency for minimum ionizing particles traversing 20 μ m of silicon. This hardware (cluster processor) is based on XILINX programmable gate arrays. The cluster processor generates accept signals, which cause recording of current raw memory address to special "accept memory". These stored addresses are used then by LFM CPU (Motorola 68LC040) to extract regions of interest from the raw data memory and transfer it to the data acquisition system.

III. CCD ACCEPTANCE TESTS

The CCD manufacturing proceeded in two phases: the design and production of a few CCDs, and then production of the bulk of the CCDs. The phase 1 CCDs were tested at low temperature at SLAC, where they were methodically evaluated to verify that all specifications were met. After positive results of this test, phase 2 production of the bulk of CCDs was started. Phase 1 tests were used also to choose between a few different options available for production. First, there were two possible designs of the output node source followers. Each output node had two followers: a low power, high impedance first stage follower and a more powerful, low impedance second stage follower. For the first stage it was possible to use either a buried channel FET, or a surface channel FET. The buried channel has a lower noise level (27 e.r.m.s. according to our measurement with 10 MHz readout speed vs 45 e.r.m.s for surface channel); however, a larger supply voltage is required (22V vs. 17V). Though the lower noise is very attractive,

concerns about power dissipation in the cryostat, the potentially lower yield and reliability of CCDs with a buried channel, and the determination that the surface channel output node FET met our specifications very well, led us to proceed with the surface channel option. First phase tests also demonstrated that for such large area CCDs, the probability of defects ("charge traps" or potential pockets affecting charge transfer) is considerable. Some defects absorb so much charge that the entire signal from a minimum ionizing particle is lost. Though the level of charge traps in phase 1 CCDs was acceptable (average inefficient area was less than 1% of the total CCD area), steps were taken to reduce them. We eliminated the "supplementary" channels, as it was suspected that the variation in the width of these channels could create potential pockets. The supplementary channel is the specially doped narrow region (about 5 μ m wide), which runs in the center of CCD channel (20 μ m wide), employed to increase radiation hardness. Our phase 1 radiation hardness tests demonstrated very satisfactory performance for the VXD3 environment, and it was decided that the supplementary channel was not needed. The phase 2 CCD evaluation demonstrated that elimination of the supplementary channels did not reduce "charge traps", but the faulty processing procedures responsible for creation of these traps were finally identified.

Before assembling the CCDs into VXD3, all CCDs (already mounted on the ladders) were required to pass acceptance test procedures at SLAC. The results of these acceptance tests are summarized in table 1.

Table 1
Acceptance Test Results

Parameter	Acceptance criteria	Average measured value
Noise (e.r.m.s)	<63	52.2
Responsivity (μ V/e)	>2.8	2.94
Charge transfer inefficiency in I ($\times 10^5$)	<5	0.8
Charge transfer inefficiency in R ($\times 10^5$)	<25	0.9
Number of blocked columns per CCD	< 2	1.7
Number of "hot" pixels per CCD	< 4	2.3

IV. VXD3 ELECTRONICS COMMISSIONING AND PERFORMANCE

During the detector electronics commissioning some problems arose which complicated the data acquisition system operation. One of the unexpected problems was the interference from the beam passing through the detector. When the beam current reached a certain threshold, the PLL chips on the A/D boards (which provide the local clock) lost synchronization with the external clocks, supplied through optical fibers from one common source. Fortunately,

synchronization was recovered in a very short time ($< 10\mu\text{sec}$), and we did not need these clocks during beam collision time. We disconnected the "synchronisation lost" signal from the general board reset circuitry and blocked signal decoding around beam collision time ($\sim 100\mu\text{sec}$). Another problem was caused by a sharp increase in the power consumption by the LFMs at the time of data recording in the front end memory. Because it happened synchronously in all 16 LFMs, residing in one FASTBUS crate, it was difficult to keep the resulting "glitch" on the power bus within the specification necessary for reliable operation of gigabit data link. Increased bypass capacitance on the LFM boards cured the problem.

After these initial problems were solved, the electronics performed well during 3 months of running without any access to the A/D boards. However, the A/D cooling was inadequate. The hottest region on the boards reached about 60°C , which we did not consider as very safe. The cooling system is being redesigned and will be rebuilt before the next run. During the run one FINISAR optical transmitter failed, and one of the output buffers for the CCD image clocks failed. We are inclined to attribute this to high ambient temperature.

V. FIRST RESULTS FROM RUN DATA ANALYSIS

A. Spatial Resolution

The use of large area CCDs simplified the mechanical design, and allowed the ladder length increase. However, the size of the CCDs created some additional complications for hit reconstruction. Unlike VXD2, VXD3 CCDs cannot be treated as planes; their shapes have considerable deviations from a flat surface. All ladders were surveyed after assembly. Since the resolution of the coordinate measuring machine is worst for the "depth" coordinate, only sideview measurement of CCD edges had sufficient accuracy, dominating the fitting of CCD shapes to Chebyshev polynomials.

The positions of all CCDs were derived from the barrel survey data. The survey was performed at room temperature, and correction for thermal contractions were calculated. The orientation of the ladders during the survey with respect to gravity was different from the orientation in the final detector, necessitating gravity sag corrections. The final determination of the CCD positions on the detector will be based on charged particle track reconstruction. This procedure was well established for VXD2 where tracking data from about 50,000 Z events achieved sufficient accuracy. With about 50,000 events recorded during the first run with VXD3, work on the final alignment is now in progress. Although the final alignment has not converged, we can make some estimates of our coordinate measurement accuracy from distributions such as the residuals in barrel 2 CCDs relative to the expected track positions, based on barrel 1 and 3 measurements. The global alignment is not yet completed so we expect the residuals to be polar and azimuthal angle dependent, but for restricted regions the width of such distributions should be limited only by the measurement errors and multiple scattering. Figures 3 and 4 illustrate this. The scale of current misalignment may be seen from comparison of the width of distributions 4a and 4b. The

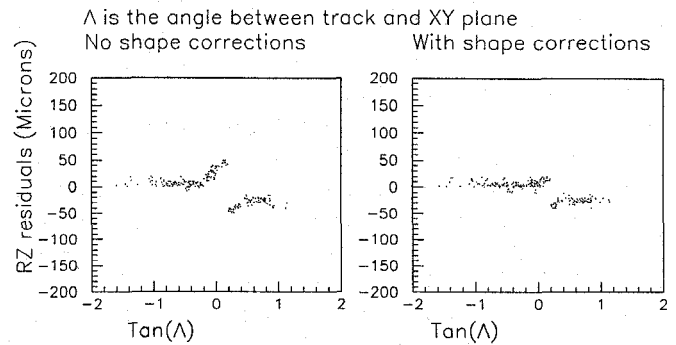


Fig. 3 Residuals for a specific triplet of CCDs vs. dip angle Λ . Effect of the CCDs shape correction is seen.

distribution of residuals summed over all regions of VXD3 (labelled global) has a sigma of $21.0\mu\text{m}$, while the residual for a restricted region is only $6.0\mu\text{m}$.

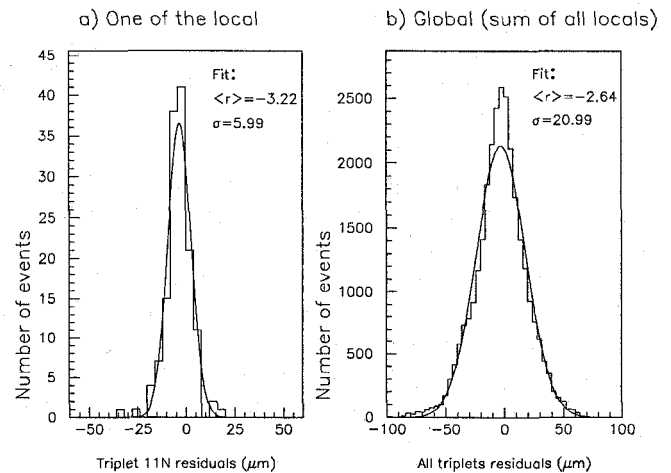


Fig. 4 Distributions of residuals in one VXD3 layer relative to the extrapolation from the two other layers presented for a restricted region of VXD3 (a) and for the entire detector (b).

B. Detector Efficiency

The single-layer efficiency can be estimated from the observed amplitude distribution for minimum ionizing particles and the cluster processor threshold (12 ADC counts) and is $> 99\%$. We can also estimate this efficiency by extrapolating tracks from the drift chamber back to the vertex detector and checking if a hit in a VXD3 layer is seen when the other two layers are hit. This procedure gives an efficiency close to 99%. Based on this, the 2-hit efficiency of VXD3 (i.e. the probability of observing the signals from a track in at least 2 of 3 layers) should be much greater than 99% if the hit inefficiencies in different CCDs are not correlated. However, the 2-hit efficiency found directly from data (figure 5) is about 98%. This implies there are correlations in the missing signals. The natural sources of such correlations are fake tracks in the drift chamber (due to noise there), or tracks that begin in the drift chamber (for example, from γ -conversion).

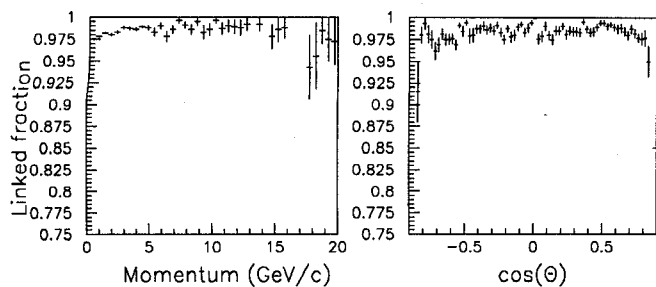


Fig. 5 Linking efficiency for 2(or more) hits as a function of particle momentum and $\cos\theta$.

Having a 99% one-layer efficiency, we can expect 97% 3-hit efficiency. As is seen from figure 6, the average 3-hit efficiency is again lower than expected (about 93% instead of 97%). Even adding 2% to correct for our presumed non-existent tracks deduced from the 2-hit analysis, we still have a deficit. The situation is clearer in figure 6b, which shows the 3-hit

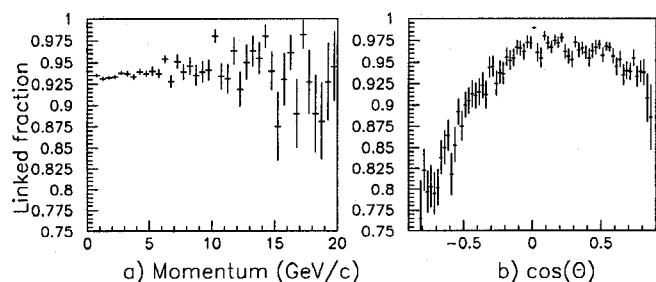


Fig. 6 Linking efficiency for 3(or more) hits as a function of particle momentum and $\cos\theta$.

efficiency vs. $\cos\theta$. At large negative $\cos\theta$ the 3-hit efficiency drops to 80% and there is also a fall-off in efficiency at large positive $\cos\theta$. This inefficiency results from the drop in signal amplitude as the charge is transferred across the CCD. This amplitude drop was investigated with a radioactive source following the run. Table 2 shows the size of the amplitude drop for each layer on the north and the south end of the detector. The amplitude drop's dependence on the detector operating temperature convinced us that it results from radiation damage to the CCDs in the inner layer of the detector (see figure 7).

Table 2
Average Signal Amplitude Loss

	South	North
Layer 1	29.1%	26.1%
Layer 2	12.1%	9.7%
Layer 3	7.6%	6.8%

During accelerator tune-up, before fully damped beams were established, the SLC electron beam was brought through the SLD detector, exposing VXD3 to considerably larger

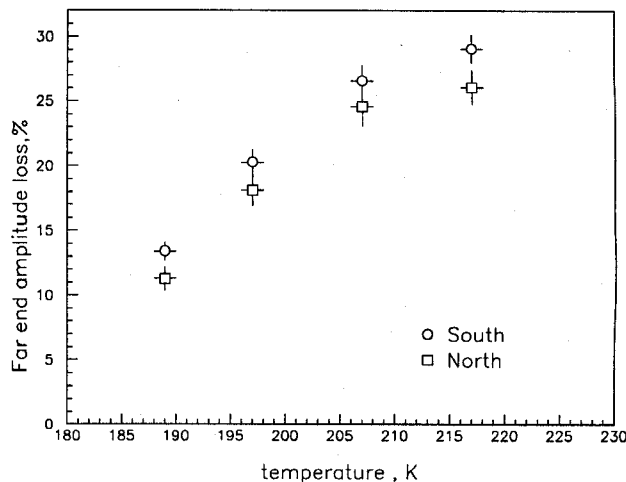


Fig. 7 Temperature dependence of the amplitude drop in the inner layer of CCDs

radiation dosage than normal running conditions. Because inefficiency at large negative $\cos\theta$ is observed in data from the very beginning of the run, and does not change during the run, we conclude that the bulk of the radiation damage happened at this period of accelerator tune-up. In general, this damage does not compromise the potential for high-efficiency tracking. We can't improve the 1996 run data, though even with this observed inefficiency it is still much better than with VXD2 (where we had majority of the tracks with only 2-hits in the vertex detector). However, for the next run we will lower the operational temperature from -50°C to -90°C . At this temperature (as we have observed with the radioactive source) the effect of radiation damage may be nullified (see [7] for details on mechanism).

VI. CONCLUSION

The SLD collaboration has constructed and successfully commissioned the new vertex detector VXD3 during 1996. Preliminary results from the first run confirmed its potential for improved resolution. Further improvements in the VXD3 operation are expected for the next run.

VII. REFERENCES

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