# Relationship between the charging damage of test structures and the deposited charge on unpatterned wafers exposed to an electron cyclotron resonance plasma

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The correlation between the nonuniformities of plasma parameters (i.e., floating potential) and the induced charging onto the surface of oxide-covered unpatterned 4 in. Si wafers exposed to $O_2$ electron cyclotron resonance (ECR) plasma is investigated. Wafers covered with a 1000 Å oxide layer were exposed to the ECR plasma under nonuniform conditions, and the induced surface charge was mapped on the wafers using contact potential difference technique. Floating potential profiles were monitored using a Langmuir probe. Experimental data indicate that the magnitude of the surface charge is proportional to the deviation of the floating potential from its surface-averaged potential. These results were compared to location of the damage of metal-oxide-semiconductor capacitor test structures exposed to same plasmas. © *1998 American Institute of Physics.* [S0003-6951(98)03310-5]

In metal-oxide-semiconductor (MOS) device fabrication, plasma processing plays an important role since it has many advantages in terms of process convenience, directionality, and high resolution. However, because of the existence of charged particles, plasma processing enhances the damage potential due to charging of the processed surfaces.

Previous studies clearly indicate that gate-oxide charge damage can be a severe problem in electron cyclotron resonance (ECR) systems. It is becoming apparent that plasma nonuniformities which occur across the surface of the wafer during processing are a major factor in this issue.[1–3] Namura *et al.*,[4] concluded that plasma-potential variations were responsible for the oxide-degrading charge buildup, while Samukawa's studies[5,6] show that ion current-density nonuniformity was the primary cause of the damage. A strong correlation between the early breakdown percentage of MOS capacitor test structures and the nonuniformity of the floating potential and plasma potential profiles measured above the wafer stage has also been reported.[7] A method for online monitoring of oxide surface charge accumulation has been developed using contact potential difference (CPD),[8] a material analytical technique. In previous studies,[9] CPD maps of oxide-covered wafers subjected to plasma processing were related to the corresponding capacitor-leakage test maps. However, CPD results have not yet been correlated to the plasma parameter profiles as well as the damage produced in processing tools.

The goals of this work are: (i) investigate the charging phenomena on oxide-covered Si wafers upon $O_2$-ECR plasma exposure using the CPD technique; (ii) demonstrate the relationship between the plasma floating potential recorded above the wafer and the magnitude of the oxide surface charging; and (iii) to find a correlation between the nonuniformities in floating potential, the process-induced surface charge distribution on unpatterned oxide-coated wafers and the damage locations in MOS capacitor test structures. We demonstrate that Langmuir probe-based measurements of the floating potential can be used to monitor the potential for charging damage in an ECR. We also demonstrate that CPD correlates well with Langmuir probe measurements in characterizing plasma nonuniformities during semiconductor processing. The latter provides a simple, rapid, and cost-effective method for determining whether damage to a patterned wafer is likely to occur.

The ECR plasma-etching system employed in this study consists of a source region where a high-density ECR plasma is produced, and a downstream region where the wafer is located. The plasma source incorporates a 1.5 kW microwave power supply, vacuum chamber, waveguide, microwave mode converter, magnet power supplies, and a pair of magnets arranged in a magnetic-mirror configuration. The wafer stage is located 19 cm below the resonance region, and it is provided with a rf connection, electrostatic clamping, and helium backside cooling. In order to create local, ''artificial'' nonuniformities, a special electrode assembly[7] was mounted on the stage, above the wafer. It consists of a stainless steel ring and a circular grid electrode that are independently biased relative to the chamber ground. During the experiments, the ring voltage was set to $-20$ V and the grid voltage to $+30$ V. Figure 1 displays a comparison between floating potential profiles for a uniform and a nonuniform case, for a 2 mTorr, 1000 w microwave power, $O_2$ plasma.

The floating potential was monitored using a Langmuir probe[10] diagnostic. The probe scans the plasma radially 1 cm

 

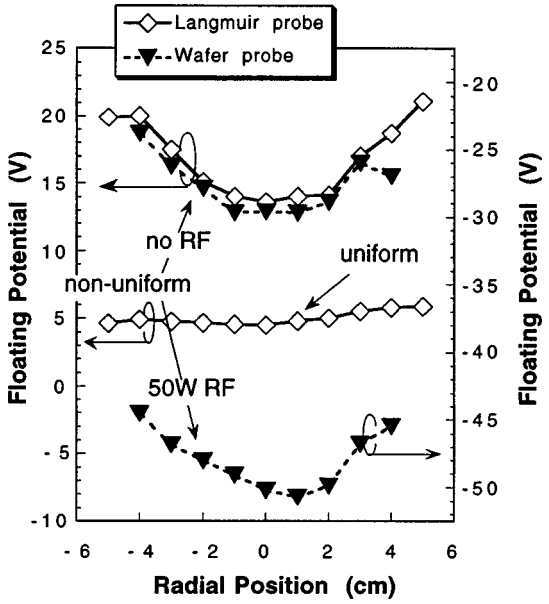


FIG. 1. Floating potential measurements were performed for uniform and nonuniform plasmas, on the surface of the wafer and 1 cm above it.

above the surface of the wafer. The connection between the wafer map and the region of the probe measurements is shown in Fig. 2. Plasma potentials, floating potentials, ion saturation currents, plasma densities, and electron temperatures were monitored. Floating potential profiles were also recorded using a high impedance voltmeter.

To make sure that the profile of the Langmuir probe-based floating potential across the stage is similar to that from the surface of the wafer, a specially designed wafer was employed, similar to the SPORT wafer.[11] It is an oxide covered wafer, with metallic pads on its surface, and with electrical connections coupled to a high-impedance voltmeter through a low-pass filter. The positioning of the pads on the wafer corresponds to the Langmuir probe measurement locations (see Fig. 2). Figure 1 exhibits measured floating potentials from the surface of the wafer recorded at the pad locations, along with Langmuir probe measurements above the stage, in the presence and absence of rf biasing, versus radial position. In the absence of rf power, the two measurements result in almost identical values for the floating potential, while for 50 W rf power, the average potential value on the surface becomes more negative, and the Langmuir probe measurements do not indicate significant changes. However, both measurements show similar shapes.

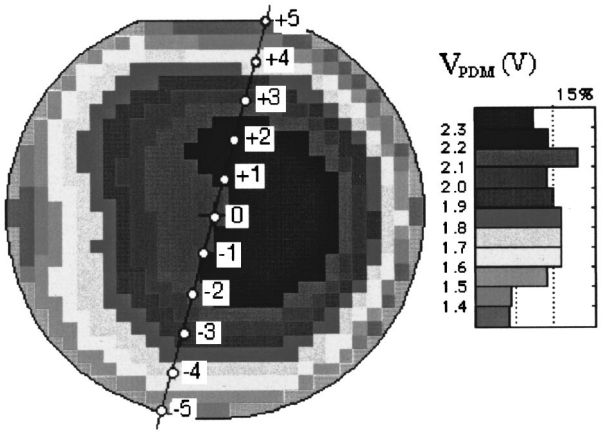


FIG. 2. Map of the oxide surface charge on a wafer exposed to a 1000 W microwave power, 2 mTorr, 50 W rf power, nonuniform plasma. Different shades reflect different amount of charge stored on the wafer surface. The highest magnitude of the charge is found on the center of the wafer. The dots located along the line rotated 75° counterclockwise with respect to the major flat of the wafer represent the location of the measurements of the floating potential.

Test wafers (blank Si wafers, $p$ type, 10–20 $\Omega$ cm, with thermally grown, 1000 Å thick oxide) were processed in $O_2$ plasma. The processing conditions were similar to those employed in the previous work[7] on MOS test structures. The structures were fabricated on 4 in. $n$-type Si wafers, with 5 $\Omega$ cm resistivity. Each wafer consisted of 84 dies, 220 capacitors/die, with two different gate areas of $6\times6$ $\mu m^2$ and $20\times20$ $\mu m^2$, and antenna ratios varied between 178–11 111 and 16–1000, respectively. The gate oxide thickness was 10 nm. The control wafer showed no incidence of early breakdown, and the intrinsic breakdown-voltage range was from 13 to 18 V. Whole-wafer maps of the breakdown-voltage data for the structures with the largest antenna ratio were made.[7]

Shortly after the processing, the induced charge on the surface of the wafer was mapped using the CPD technique. CPD measures an ac voltage $V_{PDM}$ induced on a reference electrode, located in the wafer's vicinity, by an oscillating shutter placed between the electrode and the wafer. It has been shown[9] that, in the case of a wafer covered by a thick oxide (1000 Å), $V_{PDM}$ is the change of the oxide surface barrier, a direct function of the charge placed on the oxide's surface by plasma processing. Therefore, plasma-induced oxide surface charge can be expressed as $V_{PDM}{}^{*}\epsilon_{ox}/d_{ox}$, where $\epsilon_{ox}$ is the oxide permittivity, and $d_{ox}$ is the oxide thickness. CPD permits fast, noncontact measurements without need for any wafer processing.[8] An example of a CPD wafer map is displayed in Fig. 2.

In the case of MOS capacitors, the charging induces potential differences across the gate-oxide that cause the generation of Fowler–Nordheim tunneling currents,[12,13] leading as a result to dielectric breakdown. Such charging occurs from local differences in the ion and electron current fluxes reaching the individual gate antennas of the test structure. Unpatterned oxide-covered wafers undergo a similar phenomenon. Due to the insulator nature of the oxide-covered wafers, ion and electron fluxes must balance locally. In the absence of the rf bias, the surface potential will exhibit a value very close to the Langmuir probe floating potential. Depending on the amplitude of the floating potential and on the thickness of the oxide and its quality, the Si substrate potential will change toward an average of the surface potential. In the case of the 50 W rf bias, a self-bias will develop to balance the electron and ion flow per cycle. Considering quasineutrality and provided $\omega_{pi}^2 < \omega_{rf}^2$, the dc voltage drop across the sheath is given by the following relation:[14]

$$V_{sh} \cong V_{RF} + \frac{T_e}{2}\left[\ln\frac{M}{2\pi m} - \ln\left(2\pi\frac{V_{rf}}{T_e}\right)\right], \tag{1}$$

where $V_{sh}=V_p-V_{fox}$, $V_p$ is the plasma potential, $V_{fox}$ is the floating potential on the surface of the oxide, and $T_e$ is the electron temperature. $V_{rf}$ (the rf voltage across the plasma sheath) is developed as a result of the voltage divider action

between the sheath capacitance and the oxide capacitance. Since the latter is much larger than the sheath capacitance, and the ECR plasma is an equipotential, $V_{\mathrm{rf}}$ remains relatively constant across the wafer, even if the sheath capacitance is nonuniform.

The Langmuir probe floating potential can be expressed as[14]

$$V_{\mathrm{fp}} \cong V_p - \frac{T_e}{2} \ln\left( \frac{M}{2\pi m} \right). \tag{2}$$

Thus, we find the relationship between the wafer surface potential and the probe floating potential:

$$V_{\mathrm{fox}} \cong V_{\mathrm{fp}} - V_{\mathrm{rf}} + \frac{T_e}{2} \ln\left( 2\pi \frac{V_{\mathrm{rf}}}{T_e} \right). \tag{3}$$

The wafer surface potential does not align exactly with the probe floating potential due to the last term in Eq. (3), which is dependent on the local electron temperature. Under the condition of this experiment, $M/2\pi m \gg 2\pi V_{\mathrm{rf}}/T_e$ and the last term in Eq. (3) is no more than 10% of $V_{\mathrm{rf}}$. Consequently, the effects of $T_e$ on the relationship between the wafer surface potential and the probe floating potential can be represented linearly by neglecting the third term in Eq. (3). Thus, the wafer surface potential will have a similar profile to the probe floating potential. As a result, we conclude that Langmuir probes can be successfully employed to monitor variations of the wafer surface potential in the ECR plasma system, irrespective of the rf bias.

Figure 2 shows the map of the surface charge distribution on a wafer subjected to processing under nonuniform plasma conditions similar to those displayed in Fig. 1. Both the floating potential and surface charge profiles show a more intense nonuniformity at lower pressures (0.5 mTorr) due to a higher $T_e$. It is noteworthy that the floating potential profiles recorded with the Langmuir probe are smoother when a rf bias is applied, and that the average surface charging was found to be less intense in comparison to no-bias conditions. This effect can be explained in our case considering Eq. (3), by noting that floating potential variations are smaller with the addition of rf bias. In all nonuniform plasma cases, the difference between the local floating potential and the surface average potential is peaked in the center of the wafer. Accordingly, the CPD extracted charge magnitude also is peaked in the center of the wafer. This indicates that a very good correlation exists between the CPD measurements and the corresponding contours of the floating potential deviation from the average.

Figure 3 shows the radial profile of the plasma induced surface charge on unpatterned wafers and the breakdown voltages of MOS capacitor test structures exposed to the same plasma conditions: 1000 W microwave power, nonuniform, 2 mTorr, 50 W rf bias plasma. Taking into account the damage threshold of the MOS capacitors, caused by the exponential dependence of the Fowler–Nordheim currents on the oxide electric field and dependent on area ratio, oxide thickness, oxide quality, and exposure time, the charge and breakdown voltage profiles show a very good correlation.

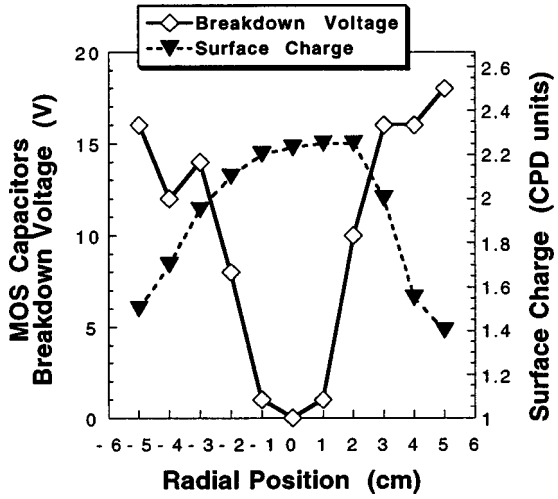


FIG. 3. Surface-induced charge on unpatterned oxide-coated wafers and breakdown voltages on MOS capacitor test structures profiles extracted from the whole-wafer maps for a wafer subjected to exposure to a 2 mTorr, 50 W rf bias plasma. The lowest breakdown voltage, between 0 and 1 V was found on the center of the wafer, and corresponds to the highest induced surface charge.

In summary, the process-induced surface charging of oxide-coated Si wafers is closely related to the nonuniformity of the floating potential profiles above the wafer surface during processing. The amount of surface charge has been found to be proportional to the deviation of the floating potential from the average value across the wafer surface. A very good correlation has been identified between the surface-induced charge maps and the maps of the breakdown voltage of the MOS capacitor test structures.

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