

MODULATION AND CONTROL TECHNIQUES FOR PERFORMANCE
IMPROVEMENT OF MICRO GRID TIE INVERTERS

by

Zeljko Jankovic

A Dissertation Submitted in
Partial Fulfillment of the
Requirements for the Degree of

Doctor of Philosophy

in Engineering

at

The University of Wisconsin-Milwaukee

August 2020

ABSTRACT
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Zeljko Jankovic

The University of Wisconsin-Milwaukee, 2020
Under the Supervision of Professor Dr. Adel Nasiri

The concept of microgrids is a new building block of smart grid that acts as a single controllable entity which allows reliable interconnection of distributed energy resources and loads and provides alternative way of their integration into power system. Due to its specifics, microgrids require different control strategies and dynamics of regulation as compared to ones used in conventional utility grids. All types of power converters used in microgrid share commonalities which potentially affect high frequency modes of microgrid in same manner. There are numerous unique design requirements imposed on microgrid tie inverters, which are dictated by the nature of the microgrid system and bring major challenges that are reviewed and further analyzed in this work. This work introduces, performs a detailed study on, and implements nonconventional control and modulation techniques leading to performance improvement of microgrid tie inverters in respect to aforementioned challenges.

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ACKNOWLEDGMENTS

First and foremost, I would like to thank to my doctoral thesis advisor, Dr. Adel Nasiri, for his academic advising, guidance, support, and understanding without which this dissertation would have never been produced. I would also like to thank Dr. Lixiang Wei for guidance during the research process that resulted in this dissertation. I thank to the members of my dissertation committee: Dr. Robert Cuzner, Dr. Lingfeng Wang and Dr. Brian Armstrong for willingness to serve as members of my dissertation committee and courses they taught which all found application in this dissertation. I thank to Puneeth Srikanta Murthy, my colleague from Rockwell Automation, for his invaluable help in obtaining experimental test data. I also thank to all my colleagues from the laboratory at the University of Wisconsin Milwaukee, for their assistance on various issues and companionship throughout my Ph.D studies. Finally, I thank to my spouse Dejana and my mother Nada for their endless support, understanding, and tolerance during the course of my studies.

1. Introduction and Literature Review

1.1. Introduction to Microgrids

The MICROGRID is defined as “a group of interconnected loads and distributed energy resources (DERs) with clearly defined electrical boundaries that acts as a single controllable entity with respect to the grid and can connect and disconnect from the grid to enable it to operate in both grid-connected or island modes” by the United States Department of Energy [1].

An installation is considered a microgrid if it has clearly defined electrical boundaries, if it can be managed as a single controllable entity, and if its installed generation capacity is sufficiently high to supply local critical loads while operated disconnected from the utility grid, in what is called the islanded mode.

This makes microgrids a small, local and independent electrical power systems made possible mostly due to advancements in power electronics technologies.

Microgrid concept [2] has been introduced as a building block of the smart grid to provide a reliable solution for interconnection of distributed generation units. Microgrid provides an alternative concept for integration of renewable energy sources as well as other distributed energy resources into power system [3]–[8]. Distributed energy resources are very versatile [9] and comprise various different technologies. In [10] and [11] current practices in integration of distributed energy resources into microgrids including the mutual interaction problems have been reviewed.

Main drivers behind Microgrid concept development is the need for higher reliability and power quality [12] while study in [13] expands by adding energy arbitrage factor to the list.

Additional objectives are reduction in transmission system losses, increased electricity availability, improved resiliency, reduction of power system expansion cost and overall environmental impact.

A microgrid can either operate in the utility grid-connected mode or in islanded mode [14], [15].

In the utility grid-connected mode of operation, energy can be freely exchanged between the main grid and microgrid based on the ratio between generation and loading within the microgrid. On the contrary, in the islanded mode of operation, overall power balance between generation units and loads has to be satisfied in order to guarantee reliable operation of microgrid. Islanding can be divided into intentional, which usually occurs as a planned event, and unintentional, which can occur due to unscheduled events. Some Microgrids can only operate in islanded mode since they do not have a point of connection to the utility grid, and those are called isolated microgrids.

The hierarchical control structure for microgrids has been proposed in [16], [17] in order to provide standardization for microgrid operation and functionality. Hierarchical control is the most common control structure used in microgrids due to multiple controllable resources and strict performance requirements [15][18]–[20]. Hierarchical control structure for a microgrid typically consists of primary, secondary and tertiary control levels [16][21]-[22], as shown in Figure 1.1. These three levels differ mostly in overall speed of response and communication requirements.

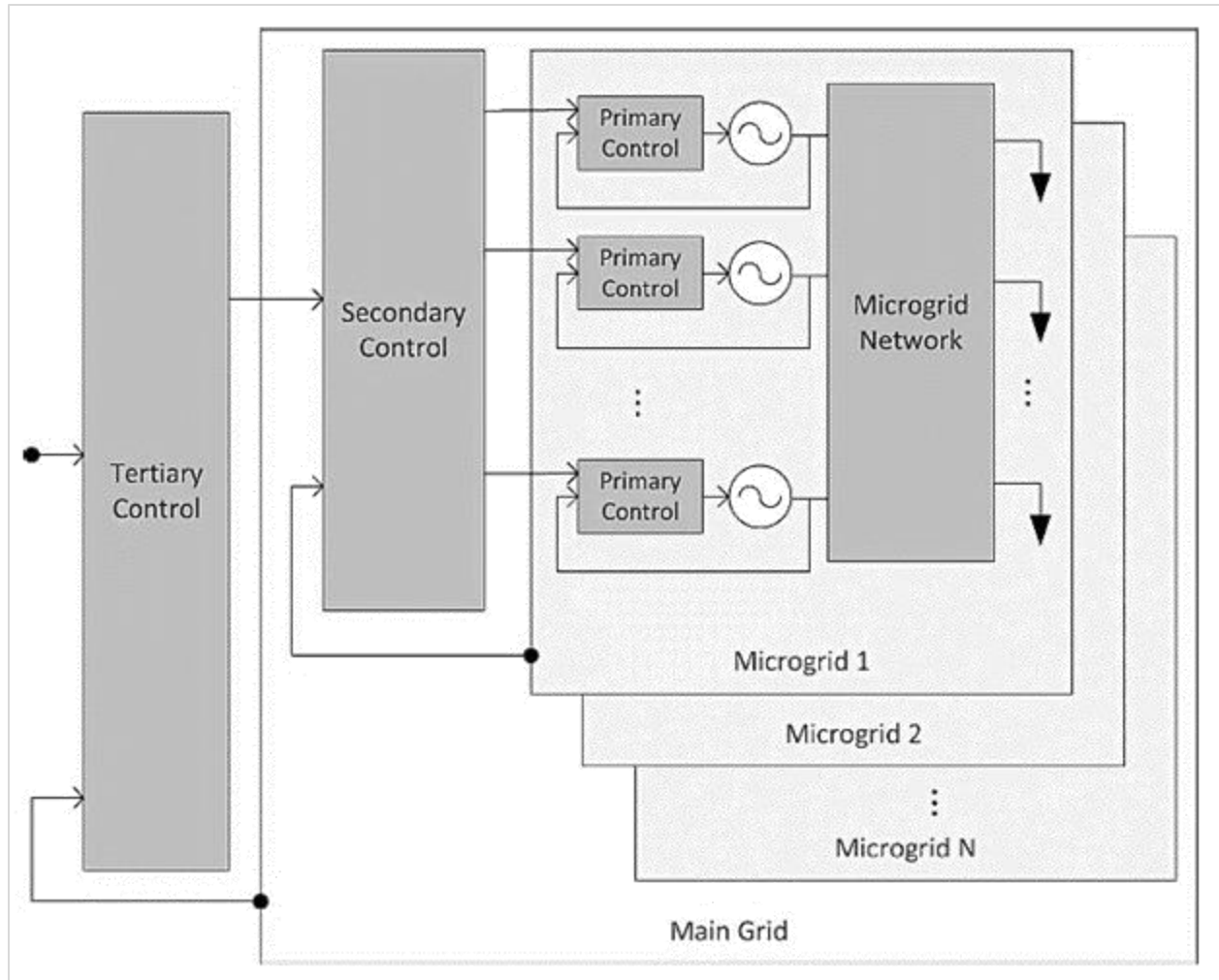


Figure 1. 1. Hierarchical control levels: primary control, secondary control, and tertiary control. [67]

The primary controller is the first level in the control hierarchy, and it is responsible for the local voltage and frequency control, ensuring a proper power sharing between multiple DG units, islanding detection and a stable microgrid operation [14], [15], and [23]. The primary control is an independent local control strategy that is based exclusively on local measurements for reliability reasons, Primary microgrid control does not require any communication and it allows each DG unit to operate autonomously. Taking into account the lack of rotating inertia in the microgrid system, the primary controller is the fastest controller in microgrid, usually operating in millisecond range time periods.

In order to achieve overall controllability of microgrid, secondary control has to be used. Secondary control is there to ensure a secure, reliable and economical operation of a microgrid. Secondary controller consists of significantly slower control loops as well as communication systems capable of gathering key measurements in different microgrid nodes, and sending various control commands to each generation unit [16], [17]. Secondary control is capable of rectifying voltage and frequency deviations produced by the primary control. Voltage unbalance and harmonic compensation using the secondary controller [24] are some of the other objectives.

Tertiary control is the highest level of control which is the slowest one in terms of control loop bandwidth. It typically operates in a minute range time periods, providing signals to secondary level controls. It is related to economic optimization algorithms based on the electricity market trends [16]. Tertiary controller typically targets microgrid long term set points depending on the host power system. It should coordinate the operation of multiple microgrids interacting in the system, and provide support for the host grid in terms of voltage, frequency etc.

Furthermore, it should communicate thru the information with the distribution system operator to ensure optimal microgrid operation inside the power utility grid. Finally, Tertiary controller is responsible for power flow and overall power quality at the point of common coupling (PCC) between microgrid and a utility grid.

The main power components in a microgrid are distributed generation units, distributed energy storage systems, various types of microgrid loads and distribution network equipment which are connected to the host grid through a point of common coupling.

Distributed generation units can be either dispatchable or non-dispatchable in terms of active power control. Dispatchable units can be fully controlled in terms of active and reactive power and typically those are diesel or natural gas generators. On the other hand, non-dispatchable

units, cannot be externally controlled in terms of active power due to intermittency in the generation. Therefore, they can only be controlled in terms of reactive power, which is typical behavior for solar and wind generation units.

Energy storage system primary role is to balance the difference between the active and reactive power generation and distribution in the microgrid due to renewable energy generation intermittency.

Microgrid loads can be either fixed or flexible from both active and reactive load standpoint. Fixed loads have to be supplied all the time, while flexible loads can be either curtailed or deferred based on the conditions.

There are several major challenges in having multiple distributed energy resources in a microgrid system. Due to a lack of dominant source of active energy, common control strategies utilized in utility grid system are not applicable to microgrid system [25]–[27]. Additionally, Islanded mode of operation requires completely different dynamic of regulation comparing to grid-connected mode, with significant engagement of reactive power control [25].

1.2. Power Converters in Microgrid Applications

Power converters in a microgrid, commonly named microgrid tie inverters, are primarily used as part of either non-dispatchable or dispatchable distributed generation units, energy storage systems and variable frequency motor loads. According to the primary microgrid control structure, microgrid tie inverters can be sorted into grid-feeding, grid-supporting, and grid-forming power converters [28], [29] as represented in Figure 1.2.

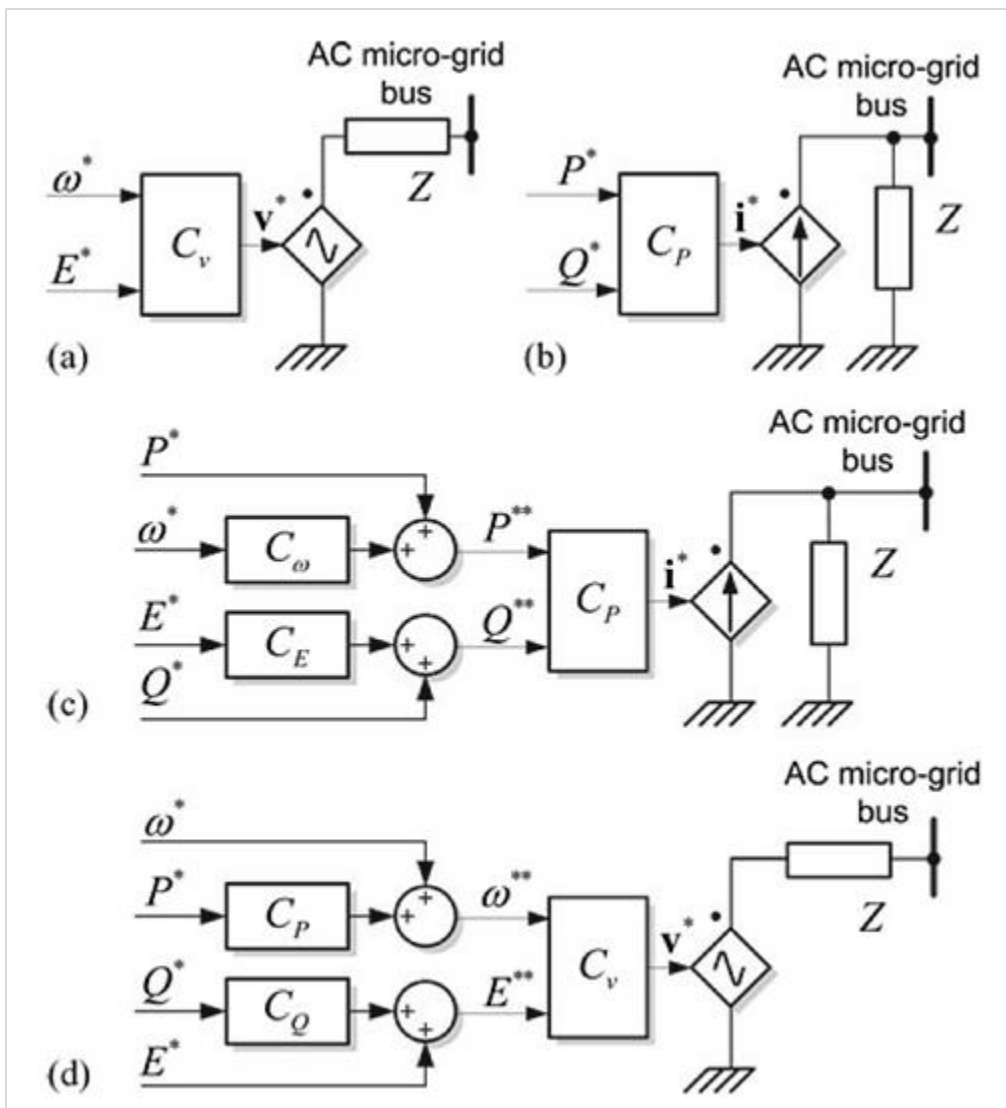


Figure 1. 2. Simplified representation of grid-connected power converters. (a) grid-forming, (b) grid-feeding, (c) current-source-based grid-supporting, and (d) voltage-source-based grid-supporting. [68]

Grid-feeding power converters are controlled as current sources, with the simplified Norton model representation of an ideal grid connected current source and high impedance connected in parallel. Majority of the power converters in microgrid systems operate as grid-feeding converters, with the primary role of injecting active and reactive power to an energized grid. The most common examples of grid feeding converters are PV and wind turbine systems [30] which are controlled by a maximum power point tracking controller. Maximum power point tracking controller sets reference active and reactive power values for P and Q, and it is not part of the basic control structure of a grid-feeding power converter. When microgrid operates in an island mode, grid feeding converters cannot operate without the grid-forming converter, synchronous generator units or grid-supporting power converters to set the reference voltage and frequency values for a microgrid system. In a grid tied operation mode, grid feeding converters can only impact microgrid voltage and frequency at a higher level control by adjusting the active and reactive power references P and Q as explained in [31], [32]. The inner controller of grid-feeding power converters regulates the current injected into the grid [33]. The reference for this inner loop current controller is set by outer loop power references P and Q [34] and [35]. Grid-feeding power converters can locally control active and reactive power references P and Q according to a predefined maximum power point algorithm [36], both in grid-connected and islanded microgrid condition. Secondary control in a microgrid can set power references for grid feeding converters in order to minimize the voltage and the frequency deviations in the power system. In island operation, the secondary controller provides different set of power references in order to equalize generation sharing in the microgrid. The tertiary microgrid level controller indirectly controls grid-feeding power converters in order to ensure economically optimal operation of the system.

The grid-forming converters are controlled as voltage sources, with the simplified Thevenin model representation of an ideal grid connected ac voltage source and low impedance connected in series. Series impedance value is crucial for power sharing capability between multiple grid forming converters in a microgrid. A good example of a grid forming converters is an energy storage system, which is typically disconnected in a grid tied mode. However, in islanded microgrid mode, energy storage system forms the microgrid voltage by controlling the voltage magnitude E and frequency ω , which will be used as a reference for the rest of grid-feeding power converters connected to it [37]. The external control loop of the grid forming converters controls Voltage Magnitude E^* and the frequency ω at the point of common coupling while the internal control loop regulates the current supplied by the converter in the same manner as in grid feeding power converters [26], [38]. Voltage control loop of the grid-forming power converter is typically disabled when the microgrid operates in a grid tied mode. Secondary control in a microgrid can set voltage and frequency references for grid forming converters during the transition between grid tied and islanded mode in order to ensure proper microgrid synchronization and reconnection to the utility grid.

Grid-supporting converters are either represented as a simplified Thevenin model of an ideal grid connected ac voltage source and low impedance connected in series or a simplified Norton model of an ideal grid connected current source and high impedance connected in parallel. A grid-supporting power converter is tasked to contribute to the regulation of the grid frequency and the voltage by controlling the active and reactive power delivered to the grid [39]. Regulation of either output current or voltage places grid supporting converters in between grid-feeding and a grid-forming power converters in terms of functionality. While current source grid supporting

converter needs a grid forming unit to operate, voltage source version can operate in both grid-connected and island mode regardless of the presence of other units.

Current source grid supporting converter has the objective to supply the active and reactive power to the microgrid, with online adjustments necessary to contribute to regulation of the voltage amplitude and frequency of the microgrid. Current source grid supporting inverters are very similar in behavior to utility Grid connected wind turbines in terms of grid power supporting capabilities [40]. Voltage source grid supporting converter has the objective to regulate the amplitude and the frequency of the output voltage of the converter at the PCC in both grid-connected and island modes, with limited contribution to the overall power sharing between generation units in the microgrid. Voltage source grid supporting converters do not require any grid-forming converter for operation in the microgrid. A good example of the voltage source grid supporting converter would be an uninterruptible power supply which controls the output voltage and frequency while regulating output power sharing between multiple units in system [41]. In order to ensure proportional power sharing between multiple generation units in a microgrid, droop control is implemented as part of the grid supporting control algorithm. Droop control has shown to be the most practical algorithm for communication less power sharing in a microgrid [42], as it mimics the familiar self-correcting electromechanical behavior of synchronous generators in utility power system. The droop regulation technique regulates the exchange of active and reactive power within the microgrid, by increasing the injected active power when the grid frequency decreases and increasing the delivered reactive power when the grid voltage amplitude decreases in order to keep the microgrid voltage and frequency under control. The voltage and current Controllers are designed to reject high frequency disturbances and provide sufficient damping for the output LCL filter [43], [44]. This primary control level in grid-supporting power converters establishes voltage

and frequency stability in the microgrid by ensuring proper power sharing between units. The secondary control level sets the droop characteristic coefficients of multiple generation units depending on the voltage and frequency deviation in the microgrid. The tertiary control establishes the secondary control reserve in the microgrid.

For investigation of the dynamic behavior of the microgrid system eigen value study needs to be performed. Small-signal modeling and steady-state analysis of an autonomous microgrid was investigated in [35],[45] – [50].

In [27] a systematic methodology for development of a small-signal dynamic model of a microgrid under varying parameter condition is proposed.

Similar modeling study of an inverter based microgrid is presented in [35]. The small-signal state-space model of a microgrid was constructed and modes (eigenvalues) with corresponding frequencies and damping values were identified. The relation between system stability and system parameters was established and sensitivity analysis was conducted. The complete set of eigenvalues of the system has shown existence of a large range of frequency components which fall into three different clusters. High frequency modes in cluster 3 were shown to be sensitive to the state variables of LCL low pass filter and the corresponding line currents. Medium frequency modes in cluster 2 were dominantly affected by state variables of voltage and current controller, and output filter. State variables of the power controller were impacting low frequency dominant modes in cluster 1.

Another small-signal dynamic model of the microgrid was constructed as part of study on the power sharing dynamics in a microgrid system [49]. Linearized model of a microgrid system with inverter, line and load states was given in the standard form. Complete set of modes (eigenvalues) of the microgrid study system, indicates a wide band of dynamic modes similar as

in [35]. Power sharing controllers and corresponding low bandwidth loop filters dominantly dictate the low-frequency modes. Medium frequency modes are sensitive to medium bandwidth voltage control loops. LCL filters and the current control loops mainly affect high frequency modes. Aforementioned separation in a frequency domain is intentionally targeted as part of the overall design of a microgrid tie inverter system. Typically starting from a given switching frequency bandwidth of the inner current control loop is determined. LCL filter resonance frequency is designed low so to avoid any switching harmonic resonance, but not very low to avoid any low-order harmonic resonance. Under practical design constraints, a typical microgrid tie inverter is designed with a current control loop bandwidth of about 800Hz– 2 kHz, voltage control loop 3-10 times slower, and power control loop 1–20 Hz, Therefore, the frequency separation is a salient feature that inherently exists in a different inverter systems [27].

Microgrids with inverters controlled by droop controllers are known to have stability issues that have been widely covered in literature [35],[48],[51]–[58]. The eigenvalue analysis confirms that the dominant low frequency modes are mainly dictated by the droop controller [12]. Instability issues are likely to happen as a consequence of poorly damped low-frequency modes in the presence of parameter changes. Multiple strategies have been reported to increase the damping of the low-frequency modes [27],[39],[51][52]-[54], [55]-[56]. Constant power loads tend to decrease damping in a power system [57] since they often present type of loads connected to a network [58]. In both dc [59]–[61] and ac [62] microgrids constant power loads have shown to have destabilizing effect on low frequency modes and solutions have been discussed in [63] and [64]. Basically, all the low frequency focused stability studies of microgrid systems assumes that the system is not sensitive to the mid-frequency or high-frequency dynamics, and therefore microgrid

model can be simplified to represent the inverters only by their low-frequency dynamics as in [65] and [66].

To the best of author's knowledge, there has been no published work analyzing high frequency modes in details as part of the small signal analysis of the microgrid. Primary reason for lack of published work analyzing high frequency modes is related to the fact that from microgrid standpoint of view, inverter is considered an "ideal" component from the dynamics and control standpoint. From the single microgrid tie inverter analysis standpoint, LCL filter parameters, current control loop parameters and microgrid equivalent impedance mainly affect high frequency modes.

1.3. Microgrid Tie Inverter – Performance Challenges

As discussed above, regardless of the primary control operating mode, all three types of converters (feeding, forming and supporting) share commonalities in terms of utilization of common power circuit topology, modulation technique and internal current control loop, thus affecting high frequency modes of a microgrid in a same manner. However, there is a lot of unique design requirements imposed on microgrid tie inverters, which are dictated by the nature of the microgrid system. To the best of author's knowledge, there has been no published work analyzing impact of microgrid performance requirements on microgrid tie inverter design as a whole. Some of the major challenges that microgrid tie inverter application brings are:

- Nature of the microgrid induces a necessity for full rated reactive power support capability of inverters, thus challenging conventional power structure design and switching modulation techniques.
- Reduced power quality of microgrid systems affects current harmonic performance of microgrid tie inverters.
- Decoupled control over active and reactive power represents another necessary requirement for stable microgrid operation free of power oscillations
- From the single inverter standpoint, microgrid equivalent input impedance varies in time based on the microgrid ever-changing operating conditions, which affects dynamics.
- Inverter closed loop system stability and LCL filter resonance represent major challenges for microgrid tie inverter current controller design.

Following work provides a full state of the art review and detailed analysis of the listed challenges related to the behavior of the microgrid tie inverters. In addition to that, following nonconventional control and modulation techniques that provide performance improvements in respect to challenges listed above are also introduced as part of the work:

- 1) Dynamic Discontinuous Pulse Width Modulation (DDPWM) as a primary inverter modulation technique used for more efficient inverter operation under full power factor range
- 2) Grid Voltage Feedforward control for improved harmonic performance of inverter under distorted microgrid voltage condition
- 3) Decoupled Power Control for independent active and reactive power control of the inverter, free of mutual coupling.

Work is presented in seven distinct chapters, with first and last one being Introduction and literature review and Conclusions and Future work respectively.

As part of DDPWM introduced in second chapter, simple implementation algorithm with specific adjustments to MTI application is proposed. Derivation of semiconductor loss expressions along with full thermal study is performed. Complete harmonics study with major parameter impact analysis is considered.

In third chapter, low pass filter design guidelines along with parameter influence is introduced. Impedance and circuit-based analysis of the filter is performed. State space models of various filter types is derived for both reference frames.

Chapter four considers various specifics of digital control system modeling and implementation. Closed loop system performance and stability is analyzed for various control

topologies. Universal current controller parameter selection guideline is presented. Input impedance expression of a closed loop system is included.

Chapter five is solely devoted to newly proposed grid voltage feedforward and decoupled power control techniques. Derivation of controller parameters and performance of each technique is fully evaluated.

As part of proof of concept, experimental test setup and results are presented in chapter six.

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2. MTI Modulation Technique

2.1. Dynamic Discontinuous PWM

Energy efficiency is of greatest importance for power electronics systems. As part of same directive, reduction of switching losses of three phase voltage source inverter (VSI) is of primary importance. In order to clarify different switching loss reduction possibilities, simplified VSI open loop control block diagram shown in Figure 2.1. will be considered.

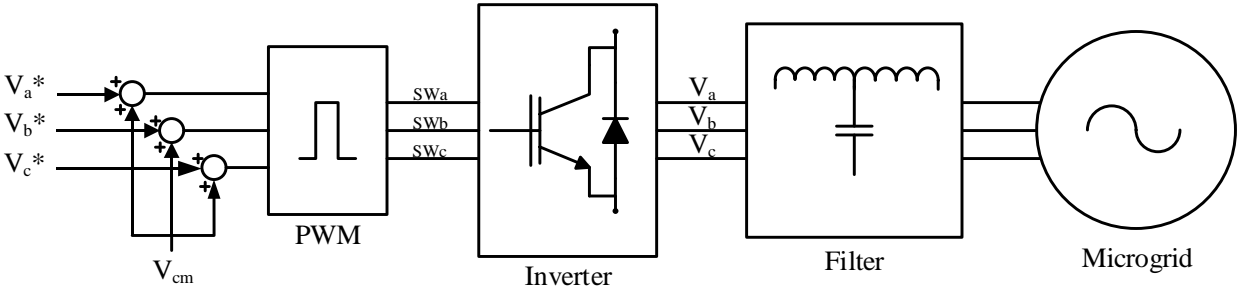


Figure 2. 1. VSI – Simplified Open Loop Control Block Diagram

As demonstrated thru derivation of (2.38.), (2.39.) and (2.40.) addition of zero sequence voltage, alternately called common mode voltage, V_{cm} to each of the fundamental output phase voltage signals does not affect the phase to phase voltages on the output of the inverter. Therefore, by variation of V_{cm} , modulation strategies can be classified into two categories, which are continuous (CPWM) [1-3] and discontinuous (DPWM) [4-7]. In CPWM strategies, normalized modulating signal is never clamped to its maximum values (-1 or 1), while operating in linear range. On the other hand, for DPWM strategies, modulating signals are intentionally clamped for duration of one third of the fundamental period (120°). During periods of intentional clamping, switching action is skipped in that phase, thus effectively leading to reduction in switching

frequency. Based on position of the clamping action within fundamental period, numerous DPWM strategies exist. The four DPWM strategies of primary interest for this work are DPWM0 [6], DPWM1 [5], DPWM2 [6] and DPWM3 [7], with clamping period positioned such that it is optimized for different power factor (PF) operation of the inverter. Therefore, different combinations of DPWM strategies called generalized DPWM (GDPWM) have been proposed in literature to minimize the switching losses of inverter at different power factor operation [8],[9]. However, the major drawback of GDPWM is the requirement for computation of the phase angle difference between voltage and current in each of the phases, which makes it very challenging for practical implementation. In order to address that drawback, [10] has presented a new direct digital implementation of GDPWM called DDT-GDPWM. DDT-GDPWM does not require knowledge of the power factor angle, but only instantaneous values of phase currents. While usage of current measurements may be a solution for certain applications, DDT-GDPWM is particularly sensitive to high harmonic content and dynamic transient behavior. That requires further computational processing and manipulation of sensing signals for applications that are particularly sensitive. Also, DDT-GDPWM is not implementable for applications that do not provide direct current measurements.

This work presents a new technique of implementing GDPWM called Dynamic DPWM (DDPWM). DDPWM automatically implements optimal DPWM strategy by means of minimal switching losses without power factor angle calculation or utilization of current measurements. Flowchart of a proposed algorithm for DDPWM is shown in Figure 2.2.

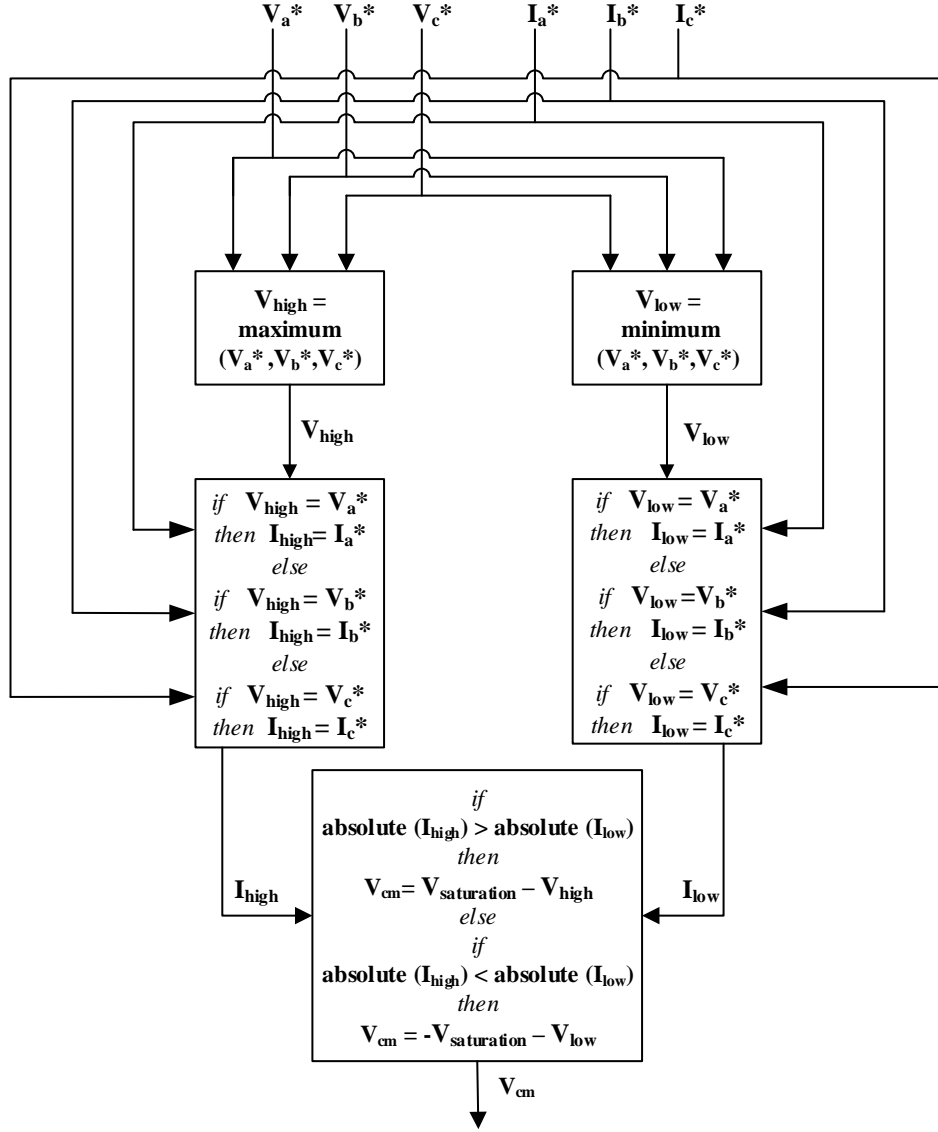


Figure 2. 2. Flowchart of the DDPWM algorithm

Algorithm uses three phase current and voltage reference signals at the inverter output. The algorithm is performed during each sampling period. Firstly, the determination of the maximum and minimum voltage reference signals between phases is made as V_{high} and V_{low} . Then, the current reference signals of corresponding phases is assigned as I_{high} and I_{low} . After that the absolute values of I_{high} and I_{low} values are compared, and the zero sequence signal V_{cm} is determined based on the clamped voltage value $V_{saturation}$ and V_{high} / V_{low} values.

In order to illustrate the functionality of DDPWM, it is first simulated at full range of phase angle differences between reference voltage and current. The voltage reference vector is fixed, while current reference vector varies per $I_{Ref} = I_m \sin(\omega_f t + \theta)$, where I_m is the magnitude of the output current, ω_f is the fundamental frequency and phase angle θ varies between $[-180^\circ, 180^\circ]$. Simulation results for all three phases are shown in Figure 2.3.

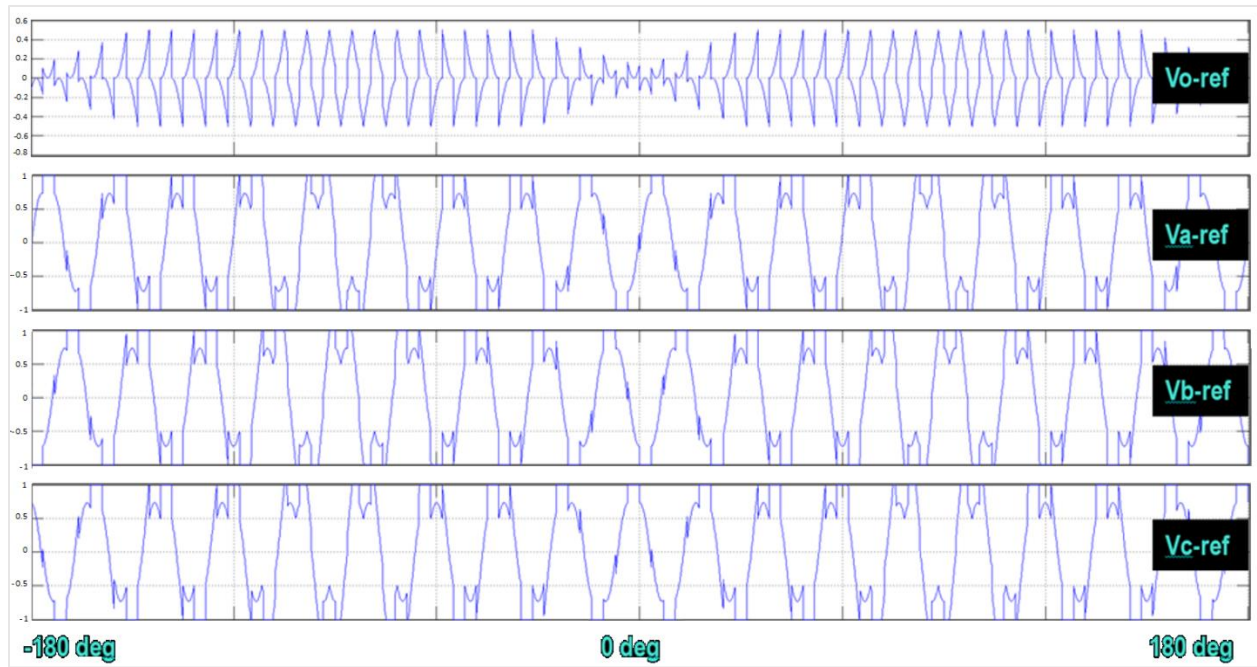


Figure 2. 3. Simulation of DDPWM algorithm for range of phase angle values $-180^\circ < \theta < 180^\circ$

The changes of the phase angle induce changes of the location of the clamped voltage location in respect to input reference voltage. The proposed modulation basically follows the maximum current, such that it minimizes switching losses. DDPWM generates following twelve patterns based on the values of phase angle θ :

Phase Angle θ Value	Pattern Description
$-180^\circ < \theta < -150^\circ$	Linear Sliding Transition from DPWM1 to DPWM2
$-150^\circ < \theta < -120^\circ$	Constant DPWM2
$-120^\circ < \theta < -90^\circ$	Linear Sliding Transition from DPWM2 to DPWM3
$-90^\circ < \theta < -60^\circ$	Linear Sliding Transition from DPWM3 to DPWM0
$-60^\circ < \theta < -30^\circ$	Constant DPWM0
$-30^\circ < \theta < 0^\circ$	Linear Sliding Transition from DPWM0 to DPWM1
$0^\circ < \theta < 30^\circ$	Linear Sliding Transition from DPWM1 to DPWM2
$30^\circ < \theta < 60^\circ$	Constant DPWM2
$60^\circ < \theta < 90^\circ$	Linear Sliding Transition from DPWM2 to DPWM3
$90^\circ < \theta < 120^\circ$	Linear Sliding Transition from DPWM3 to DPWM0
$120^\circ < \theta < 150^\circ$	Constant DPWM0
$150^\circ < \theta < 180^\circ$	Linear Sliding Transition from DPWM0 to DPWM1

Table 2. 1: DDPWM Patterns based on the values of phase angle θ

Therefore, it can be concluded that DDPWM represents a combination of four distinct DPWM methods (DPWM0, DPWM1, DPWM2, DPWM3) along with the linear sliding transition between mentioned ones.

As already described, DDPWM avoids usage of measurement signals by utilizing inverter current reference values as part of the algorithm. However, in cases like MTI shown in Fig. 2.4, where higher order filters are used as interconnection between inverter and grid, grid current reference i_2 is the only reference value available.

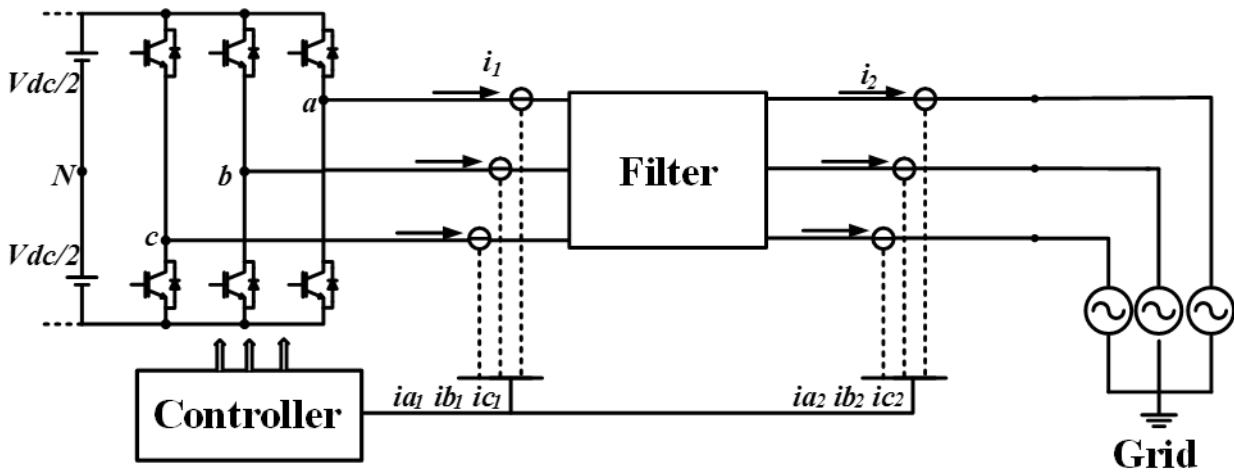


Figure 2. 4. MTI Generalized Topology

Therefore, a new reference i_1 needs to be created in order to implement DDPWM algorithm properly. Inverter side current reference i_1 can be derived by using a set of state space equations for LCL filter in synchronous reference frame, which is further explained in chapter 3.3.3:

$$\frac{di_{d1}}{dt} = -\frac{R_1 + R_c}{L_1}i_{d1} - \omega i_{q1} + \frac{R_c}{L_1}i_{d2} - \frac{V_{fd}}{L_1} + \frac{E_{id}}{L_1} \quad (2.1.)$$

$$\frac{di_{q1}}{dt} = \omega i_{d1} - \frac{R_1 + R_c}{L_1}i_{q1} + \frac{R_c}{L_1}i_{q2} - \frac{V_{fq}}{L_1} + \frac{E_{iq}}{L_1} \quad (2.2.)$$

$$\frac{dV_{fd}}{dt} = \frac{1}{C}i_{d1} - \frac{1}{C}i_{d2} - \omega V_{fq} \quad (2.3.)$$

$$\frac{dV_{fq}}{dt} = \frac{1}{C}i_{q1} - \frac{1}{C}i_{q2} + \omega V_{fd} \quad (2.4.)$$

At steady state condition, all the derivative terms can be ignored, and i_1 and i_2 can be treated as reference values i_1^* and i_2^* . Also, inverter input voltage E_i is to become voltage reference V^* , used as an input to DDPWM algorithm. After some mathematical manipulation of equations (2.1.)-(2.4.), the final expression for current reference i_1 for d and q axis becomes:

$$i_{d1}^* = \frac{\left(1 - \frac{x_L}{x_c}\right) + \frac{R_c(R_1+R_c)}{x_c^2}}{\left(\frac{x_L}{x_c} - 1\right)^2 + \frac{(R_1+R_c)^2}{x_c^2}} i_{d2} + \frac{-\frac{R_1}{x_c} - \frac{x_L R_c}{x_c^2}}{\left(\frac{x_L}{x_c} - 1\right)^2 + \frac{(R_1+R_c)^2}{x_c^2}} i_{q2} + \frac{\frac{(R_1+R_c)}{x_c^2}}{\left(\frac{x_L}{x_c} - 1\right)^2 + \frac{(R_1+R_c)^2}{x_c^2}} E_{id} + \frac{\frac{\left(1 - \frac{x_L}{x_c}\right)}{x_c}}{\left(\frac{x_L}{x_c} - 1\right)^2 + \frac{(R_1+R_c)^2}{x_c^2}} E_{iq} \quad (2.5.)$$

$$i_{q1}^* = \frac{\frac{R_1}{x_c} + \frac{x_L R_c}{x_c^2}}{\left(\frac{x_L}{x_c} - 1\right)^2 + \frac{(R_1+R_c)^2}{x_c^2}} i_{d2} + \frac{\frac{R_c(R_1+R_c)}{x_c^2} - \frac{\left(x_L - 1\right)}{x_c}}{\left(\frac{x_L}{x_c} - 1\right)^2 + \frac{(R_1+R_c)^2}{x_c^2}} i_{q2} + \frac{\frac{\left(x_L - 1\right)}{x_c}}{\left(\frac{x_L}{x_c} - 1\right)^2 + \frac{(R_1+R_c)^2}{x_c^2}} E_{id} + \frac{\frac{(R_1+R_c)}{x_c^2}}{\left(\frac{x_L}{x_c} - 1\right)^2 + \frac{(R_1+R_c)^2}{x_c^2}} E_{iq} \quad (2.6.)$$

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i_{d1}^* and i_{q1}^* values can be easily transformed back to stationary abc frame reference values i_{a1}^* , i_{b1}^* and i_{c1}^* and used as inputs to

DDPWM algorithm.

2.2. Switching Losses

For the calculation of the switching losses for DDPWM, a linear dependence of the switching energy loss on the current amplitude is assumed [11]. The average switching power loss value for a generic device is defined over a fundamental period as:

$$P_{sw} = \frac{1}{2\pi} \int_0^{2\pi} P(\theta) d\theta \quad (2.7.)$$

Where $P(\theta)$ represents switching power loss function related to a position of the switching pulse interval. It is important to point out that in two level voltage source inverter applications, single switch in a leg conducts only during half fundamental period. Therefore, in cases where turn on and turn off energy losses per commutation are provided, the average switching energy loss per switch becomes:

$$P_{Tsw} = \frac{1}{T} \int_{-\frac{\pi}{2\omega}}^{\frac{\pi}{2\omega}} \frac{(E_{on} + E_{off})}{V_{dcnom} I_{dcnom}} f_{sw} V_{dc} I_m \cos(\omega t) dt = \frac{1}{\pi} \frac{(E_{on} + E_{off})}{V_{dcnom} I_{dcnom}} f_{sw} V_{dc} I_m K_{sw} \quad (2.8.)$$

Where E_{on} and E_{off} represent a turn on and turn off energy loss per commutation for specified dc bus voltage V_{dcnom} and current I_{dcnom} . V_{dc} and I_m represents inverter dc bus voltage and output current magnitude, f_{sw} represents carrier frequency and coefficient K_{sw} represents a switching loss factor. For CPWM strategies, value of K_{sw} is equal to 1. For DPWM techniques, that factor varies based on the particular technique used and on the resulting power factor. DDPWM represents a unique case because its non-switching intervals adapt with current peaks.

For unity power factor operation DDPWM applies DPWM1 as per Figure 2.5., for which switching loss factor for a single switch can be calculated as:

$$K_{sw} = \frac{\omega}{2} \left(\int_{-\frac{\pi}{2\omega}}^{-\frac{\pi}{6\omega}} \cos(\omega t) dt + \int_{\frac{\pi}{6\omega}}^{\frac{\pi}{2\omega}} \cos(\omega t) dt \right) = 0.5 \quad (2.9.)$$

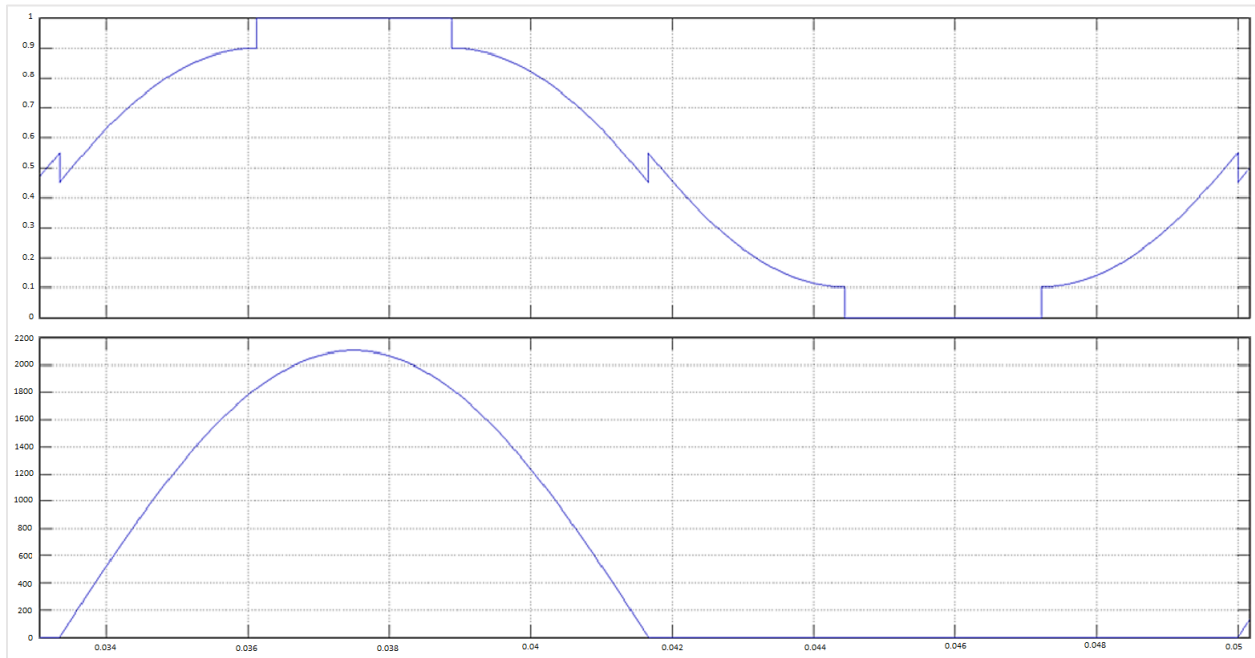


Figure 2. 5. Duty cycle and current of a single switch for DDPWM at PF=1

For pure reactive power operation at power factor zero, DDPWM uses DPWM3 as per Figure 2.6., for which switching loss factor for a single switch can be calculated as:

$$K_{sw} = \frac{\omega}{2} \left(\int_{-\frac{\pi}{2\omega}}^{-\frac{\pi}{3\omega}} \cos(\omega t) dt + \int_{\frac{\pi}{6\omega}}^{\frac{\pi}{6\omega}} \cos(\omega t) dt + \int_{\frac{\pi}{3\omega}}^{\frac{\pi}{2\omega}} \cos(\omega t) dt \right) = \frac{3 - \sqrt{3}}{2} \quad (2.10.)$$

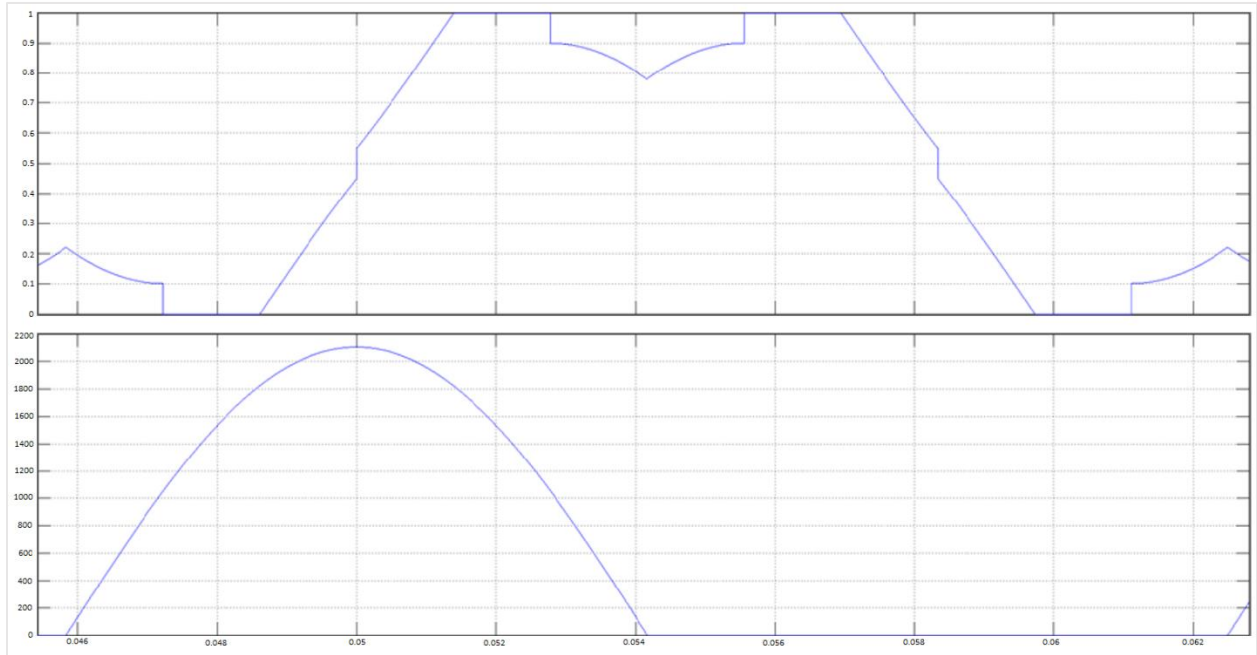


Figure 2. 6. Duty cycle and current of a single switch for DDPWM at PF=0

In order to completely evaluate switching loss performance of DDPWM, switching loss factor comparison with CPWM for a full range of phase angle values is presented in Figure 2.7.

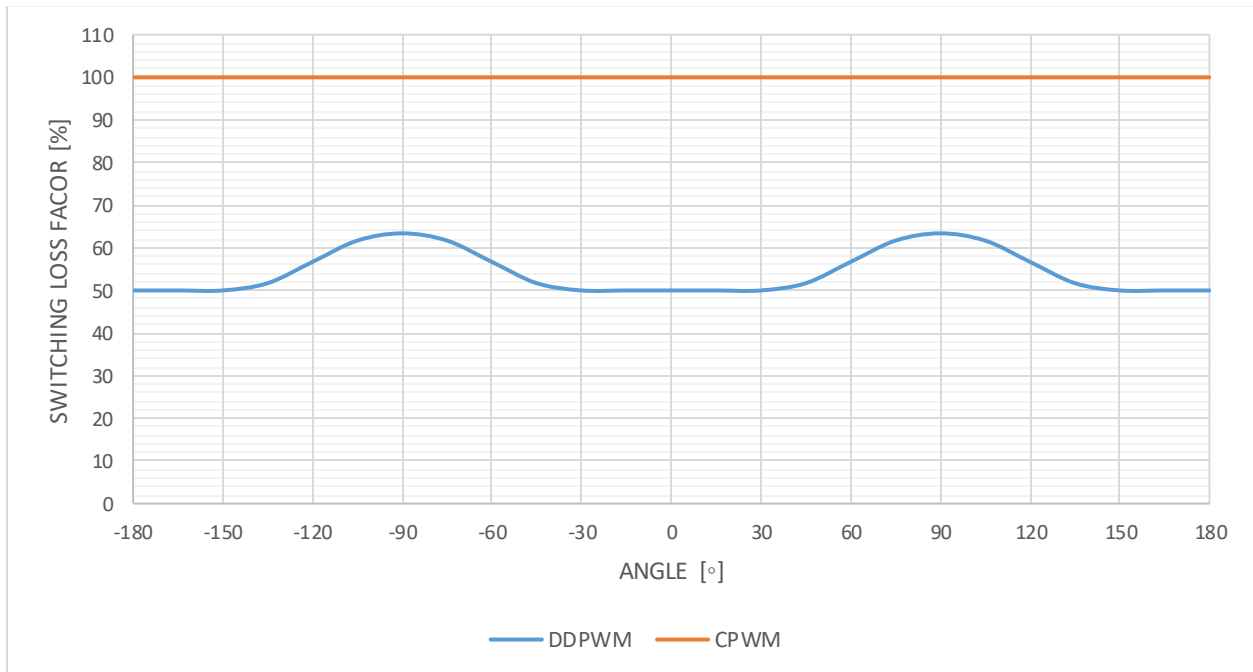


Figure 2. 7. Switching Loss factor for CPWM and DDPWM as a function of phase angle θ

Based on Figure 2.7., it is clear that DDPWM as compared to CPWM strategies provides significant switching loss reduction throughout the full range of phase angle θ values. Also, $PF = 0$ operation represents the worst case scenario for DDPWM from the switching loss standpoint.

Switching losses have been presented for generic switching device based on the turn on and turn off energy E_{on} and E_{off} , which will work for hard switched devices like transistors and mosfets. On the other hand, freewheeling diode, which is placed antiparallel with switches, produces losses once every carrier cycle due to reverse recovery phenomena. Therefore, for a given reverse recovery energy loss per commutation E_{rr} , the average switching energy loss per diode becomes:

$$P_{Dsw} = \frac{1}{T} \int_{\frac{\pi}{2\omega}}^{\frac{\pi}{2\omega}} \frac{E_{rr}}{V_{dcnom} I_{dcnom}} f_{sw} V_{dc} I_m \cos(\omega t) dt = \frac{1}{\pi} \frac{E_{rr}}{V_{dcnom} I_{dcnom}} f_{sw} V_{dc} I_m K_{sw} \quad (2.11.)$$

In order to evaluate the derived formulas for switching losses of transistors and diodes, MTI system with previously defined parameters has been simulated. System has been simulated at unity power factor condition and rated output power. Turn on/off and reverse recovery energy losses have been extracted from the datasheet of the comparative IGBT module as $E_{on} = 195 mJ$, $E_{off} = 260mJ$ and $E_{rr} = 145mJ$. Figure 2.8. shows the resulting switching loss of a single transistor and diode within inverter phase leg.

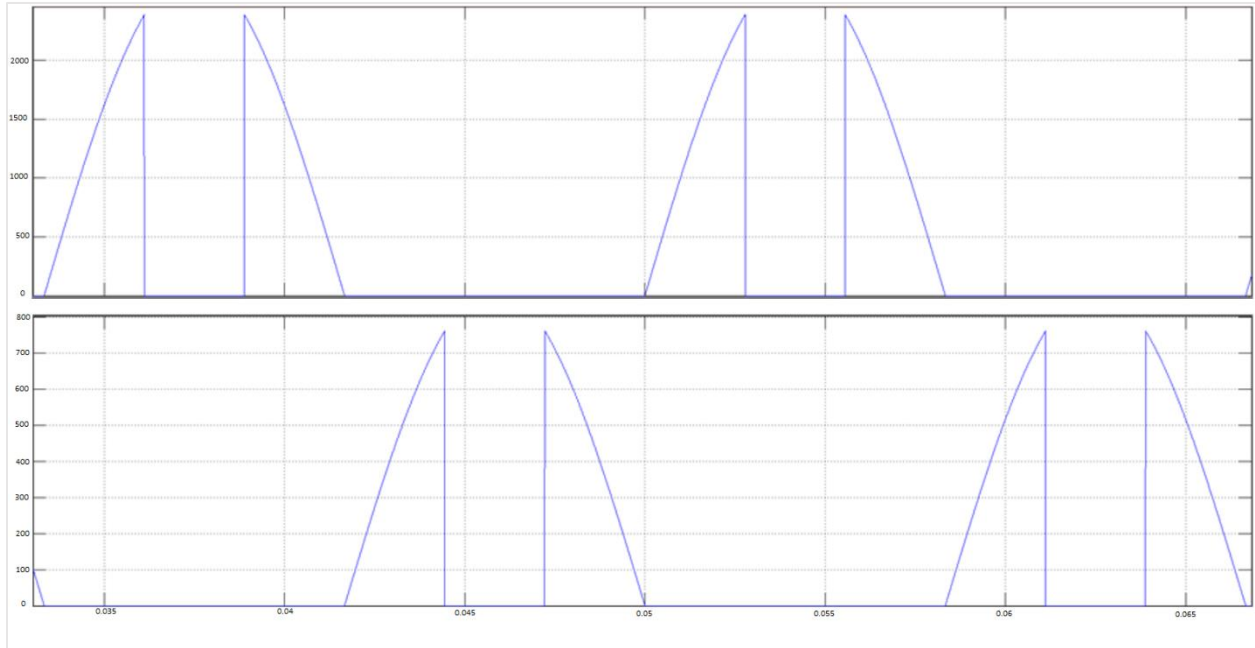


Figure 2. 8. Transistor and Diode Switching Loss within single Inverter Phase leg

As discussed previously, DDPWM clamps inverter output voltage such that, depending on the current peak position, it always guarantees minimal switching losses. Since switching losses are proportional to the value of the output current, it is clear from Figure 2.8 that for unity power factor operation clamping occurs around the peak current, thus leading to reduced losses. The average switching loss for transistor and diode can be calculated using previously derived formulas as 657.75W and 279.4W, respectively.

2.3. Conduction Losses

For the calculation of the conduction losses for DDPWM, a relative conduction period of the transistor and diode in each bridge leg is defined within a pulse half period as:

$$d_t = \frac{1}{2} \left(1 + \frac{2}{\sqrt{3}} m \cos(\omega t) + m_0 \right) \quad (2.12.)$$

$$d_d = \frac{1}{2} \left(1 - \frac{2}{\sqrt{3}} m \cos(\omega t) - m_0 \right) \quad (2.13.)$$

Where m is a modulation index defined later in (2.21.) and m_0 represents a zero sequence modulation function. Zero sequence modulation function m_0 is a characteristic of a modulator and is unique for different power factor operation as well as different modulation index m values. Forward voltage drop characteristic of switches and diodes is represented as a combination of constant voltage drop and resistive voltage drop as:

$$V_{t,d} = V_{fw} + R_{fw} I_{fw} \quad (2.14.)$$

Where $I_{fw} = I_m \cos(\omega t + \theta)$ is the device current during positive half period of conduction. Same as with switching loss evaluation, transistor in one leg and diode in opposite leg of the same phase will conduct during one half period, based on the phase current polarity, as per figure 2.9.

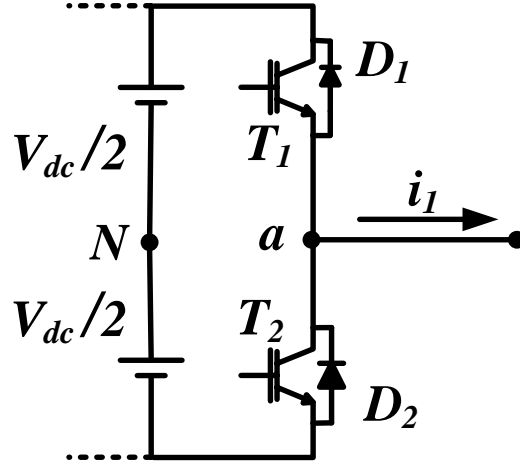


Figure 2. 9. Conduction Path for transistor and diode in a single phase for positive current orientation

The average conduction power loss value for a generic device is defined over a fundamental period as:

$$P_c = V_{fw} I_m \frac{1}{T} \int_{-\frac{\pi}{2\omega} - \frac{\theta}{\omega}}^{\frac{\pi}{2\omega} - \frac{\theta}{\omega}} d \cos(\omega t + \theta) dt + R_{fw} I_m^2 \frac{1}{T} \int_{-\frac{\pi}{2\omega} - \frac{\theta}{\omega}}^{\frac{\pi}{2\omega} - \frac{\theta}{\omega}} d \cos^2(\omega t + \theta) dt \quad (2.15.)$$

The average conduction loss formula presented above is unique for all continuous and discontinuous PWM techniques, but will produce different results based on different zero sequence modulation function m_0 , and different power factor angle θ .

Since DDPWM adapts to the position of the phase current, it basically represents a combination of different DPWM techniques at different power factor angles. Therefore, it is rather complicated to provide a final conduction loss solution that covers full range of power factor angles for DDPWM. In order to quantify the conduction losses, a solution will be provided for conditions where the transistor/ diode losses are the highest. For transistors, maximum conduction losses with DDPWM were found to occur at $\theta = 0^\circ$, leading to unity power factor operation with active power

flow direction into the grid. For diodes, maximum conduction losses occur at $\theta = 180^\circ$, also leading to unity power factor operation, but with the opposite active power flow direction towards inverter. In both cases, unity power factor operation leads to DPWM1 operation, for which zero sequence modulation function m_0 becomes:

Integration Angle φ	m_0
$-\frac{\pi}{2} - \theta < \varphi < -\frac{\pi}{6} - \theta$	$-1 - \frac{2}{\sqrt{3}}m\cos(\omega t - \frac{2\pi}{3})$
$-\frac{\pi}{6} - \theta < \varphi < \frac{\pi}{6} - \theta$	$1 - \frac{2}{\sqrt{3}}m\cos(\omega t)$
$\frac{\pi}{6} - \theta < \varphi < \frac{\pi}{2} - \theta$	$-1 - \frac{2}{\sqrt{3}}m\cos(\omega t - \frac{4\pi}{3})$

Table 2. 2.: m_0 as function of integration angle φ

Based on zero sequence modulation function expression, the average conduction loss formula for single transistor and diode becomes:

$$P_t = \frac{V_{fwt}I_m}{2} \left(\frac{1}{\pi} + \frac{2}{\sqrt{3}} \frac{m}{4} \cos \theta \right) + R_{fwt}I_m^2 m \frac{\sqrt{3}}{4\pi} \cos \theta \quad (2.16.)$$

$$P_d = \frac{V_{fwd}I_m}{2} \left(\frac{1}{\pi} - \frac{2}{\sqrt{3}} \frac{m}{4} \cos \theta \right) - R_{fwd}I_m^2 m \frac{\sqrt{3}}{4\pi} \cos \theta \quad (2.17.)$$

The maximum average conduction loss for transistors and diodes occurs at $m = 1$ and $\theta = 0^\circ$ and $\theta = 180^\circ$ respectively:

$$P_{tmax} = \frac{V_{fwt}I_m}{4\pi\sqrt{3}} (2\sqrt{3} + \pi) + R_{fwt}I_m^2 m \frac{\sqrt{3}}{4\pi} \quad (2.18.)$$

$$P_{dmax} = \frac{V_{fwd}I_m}{4\pi\sqrt{3}} (2\sqrt{3} + \pi) + R_{fwd}I_m^2 m \frac{\sqrt{3}}{4\pi} \quad (2.19.)$$

In order to evaluate the derived conduction loss formula, MTI system with previously defined parameters has been simulated. Forward voltage characteristic parameters for transistor and diode have been extracted from the datasheet of the comparative IGBT module as $V_{fwt} = 0.8\text{ V}$, $R_{fwt} = 0.73\text{ m}\Omega$ and $V_{fwd} = 0.8\text{ V}$, $R_{fwd} = 0.46\text{ m}\Omega$. Figure 2.10 shows the resulting conduction loss of a single transistor and diode at unity power factor operation, with active power injection at $m=1$.

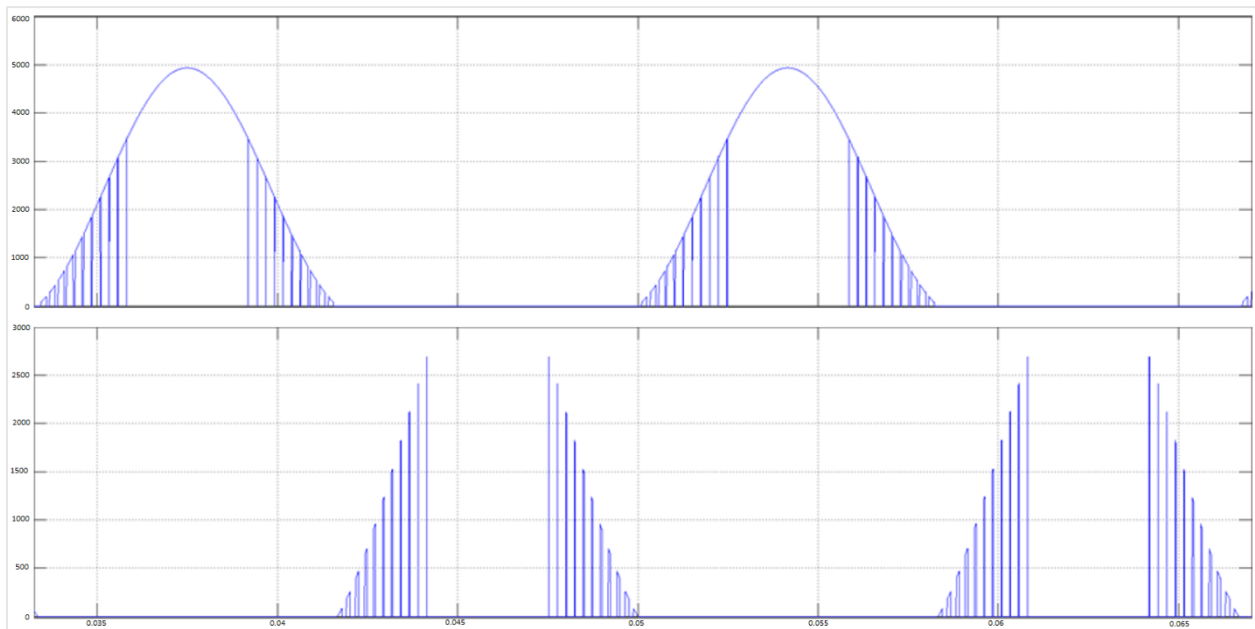


Figure 2. 10. Transistor and Diode Conduction Loss within single Inverter Phase leg

As opposed to switching losses that are not present during clamping period for both diode and IGBT, conduction losses are always present for either of the two devices. Figure 2.10 shows full conduction of transistor during clamping period, which is a consequence of power flow direction towards the grid. If the power factor flow direction was to change, full conduction of the diode would occur during same clamping period. The average conduction loss for transistor and diode can be calculated using previously derived formulas as 1305.4W and 37W, respectively.

In order to evaluate the conduction losses at other operating conditions, MTI system has been simulated for a full range of power factor angles as well as full range of modulation index values. Transistor and diode conduction losses are shown in Figures 2.11 and 2.12 respectively.

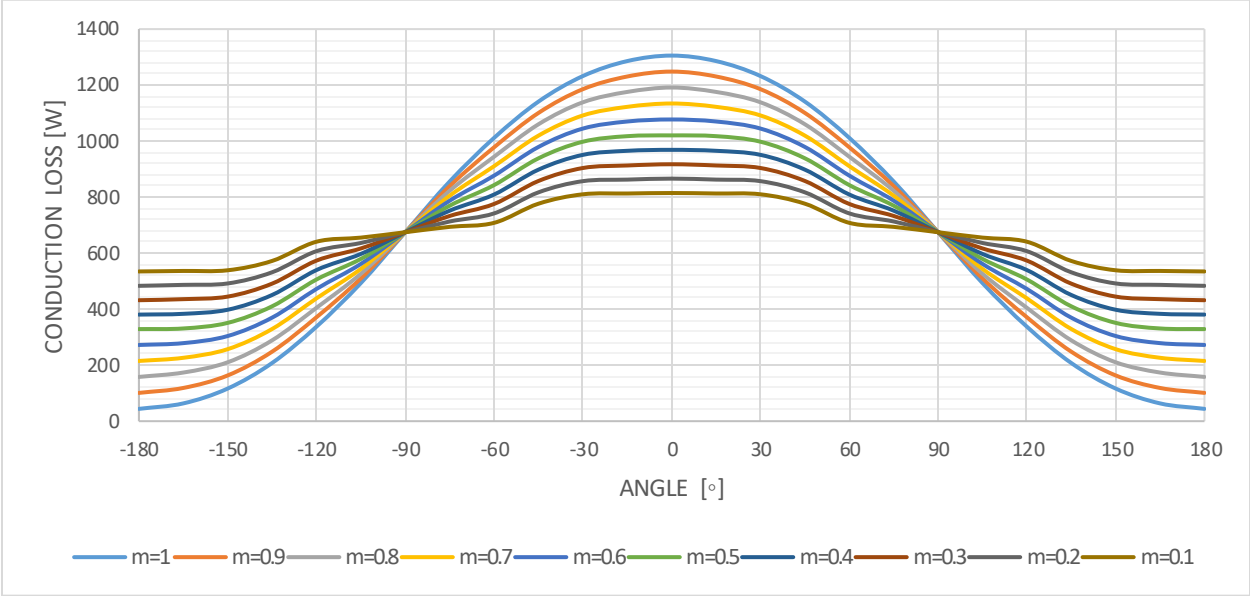


Figure 2. 11. Transistor Conduction Losses for range of θ and m values

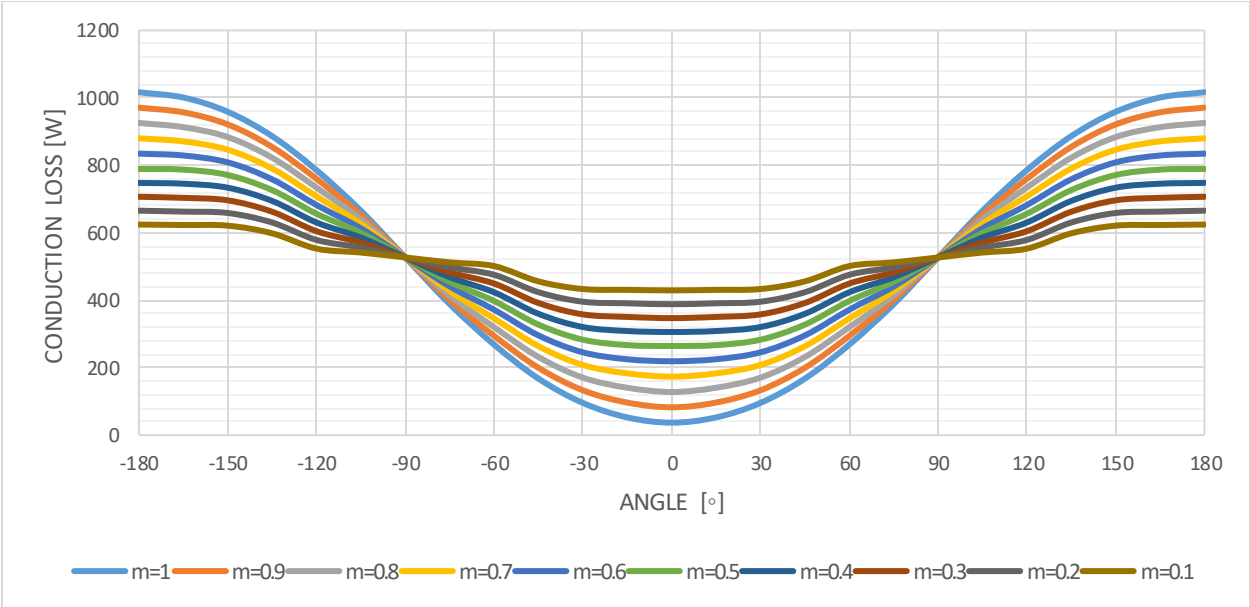


Figure 2. 12. Diode Conduction Losses for range of θ and m values

Results from figures show that higher modulation index values produce higher conduction losses of transistor for active power flow towards the grid, and lower losses for active power flow condition towards the inverter. Opposite is true for diodes. Also it is noticeable that conduction losses are independent of modulation index value, for pure reactive power operation.

2.4. Thermal Modeling and Calculation

Losses in a semiconductor devices used for microgrid tie inverter application consists of conduction and switching losses. Each one of those has been covered in details in previous sections. Total energy lost exits the semiconductor as heat, which is almost entirely dissipated thru conduction mechanism. The most precise thermal modeling method for thermal calculations is based on the finite element analysis. However, FEA is most often impractical to use due lack of design parameters exclusively known to semiconductor manufacturer. Therefore, in order to perform successful study for optimized thermal design, partial fraction thermal layer model for one dimensional heat flow (also called Foster model) is typically used. In order to perform thermal calculations using Foster model, it is important to know some important thermal parameters, such as thermal resistances and thermal capacitances, which are dependent on the semiconductor material parameters and dimensions, but are readily available thru manufacturer datasheets. An example of the Foster thermal model for half H bridge module consisting of two transistors and antiparallel diodes is presented in Figure 2.13. P, R, C and T represent power dissipation, thermal resistance, capacitance, and temperature rise of each segment respectively.

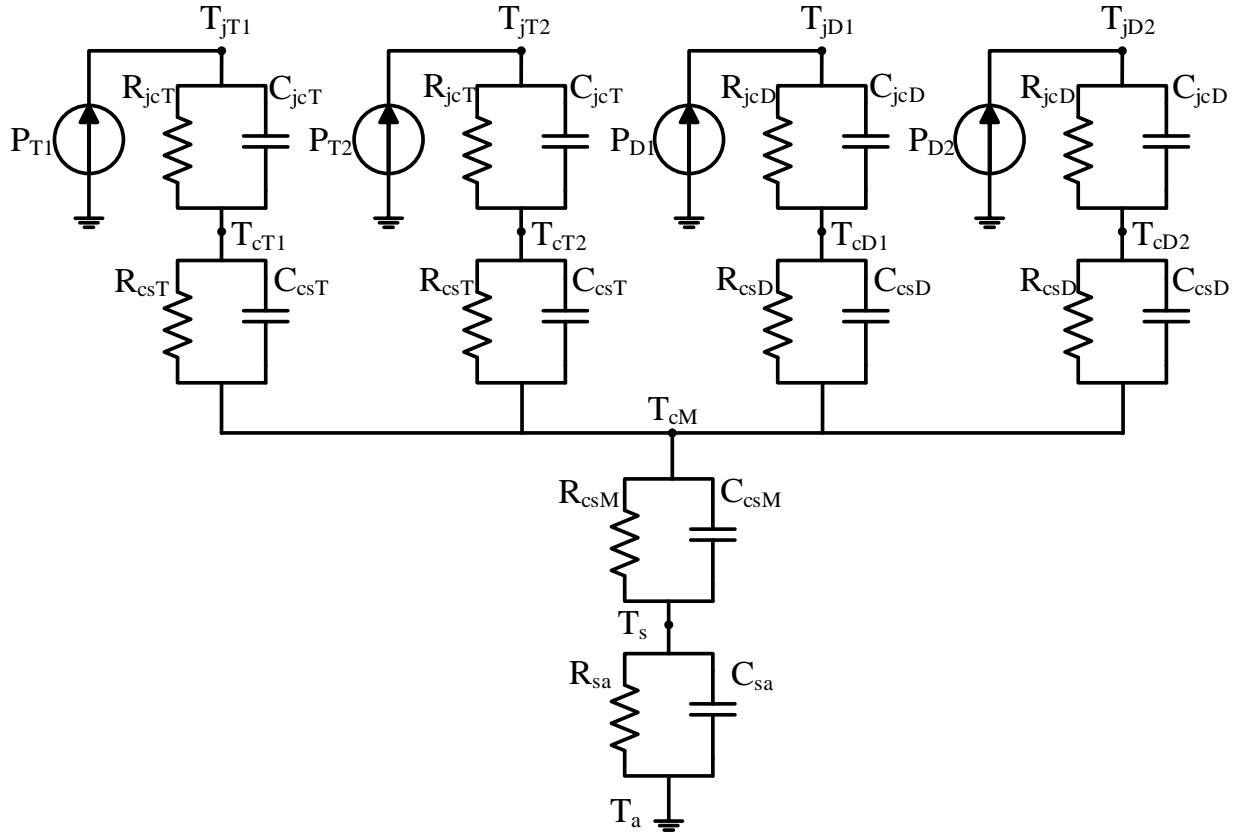


Figure 2. 13. Example of Foster thermal model of half H bridge module

Each transistor and diode in a module contains multiple parallel chips with same functionality, which are electrically isolated from the cooling surface called case. Electrical isolation is typically achieved via usage of substrates, which are thermally very conductive. Subscript $j-c$ represents equivalent thermal impedance in between individual switch junction and module case temperature. Despite the fact that there is only one case per module, each switch contains individual case temperature point, reflected thru individual case to heatsink thermal impedances shown in Figure 2.13 with subscript $c-s$. The reason for this is that only partial temperature coupling between switches exists, thus leading to uneven case temperature distribution across the case surface. The amount of thermal coupling between individual switches is reflected thru common thermal impedance between case and heatsink, using added subscript M .

Finally, at the very end of the model is the thermal impedance between heatsink and ambient, marked with subscript *s-a*. Thermal impedance between heatsink and ambient is independent of the module and is solely dependent on the heatsink design. The design of the heatsink is dependent on many application parameters, such as number of devices being cooled, ambient temperature, cooling medium selection, flow rates etc., and will not be further investigated as part of this work. For the purpose of thermal calculations, both thermal resistance and capacitance play a role in establishing a thermal impedance value, which is typically defined thru a thermal transient impedance value as:

$$Z_{th}(t) = \frac{T - T(t)}{P} \quad (2.20.)$$

Where *P* and *T* represent power dissipation and stationary temperature. Transient thermal impedance provides a dynamic thermal response of a system under step change in the power dissipation, and is important for thermal performance in applications with dynamic load changes and transient conditions. However, for MTI, which is not considered a dynamic load application, steady state thermal performance is of primary interest. Consequently, thermal capacitances can be neglected, and knowledge of thermal resistances becomes sufficient for thermal calculations.

In order to completely evaluate thermal performance of DDPWM, simulation model with previously defined parameters has been used. Total average power losses per transistor and diode for a full range of phase angle values is presented in Figure 2.14 and 2.15 respectively.

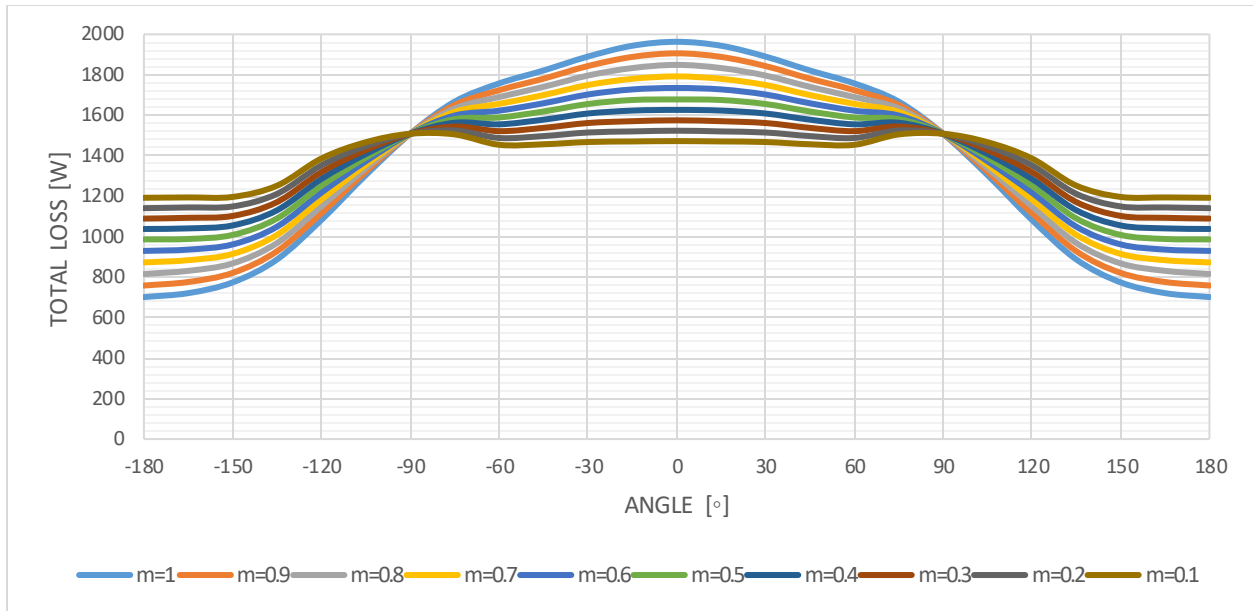


Figure 2. 14. Transistor TotalLosses for range of θ and m values

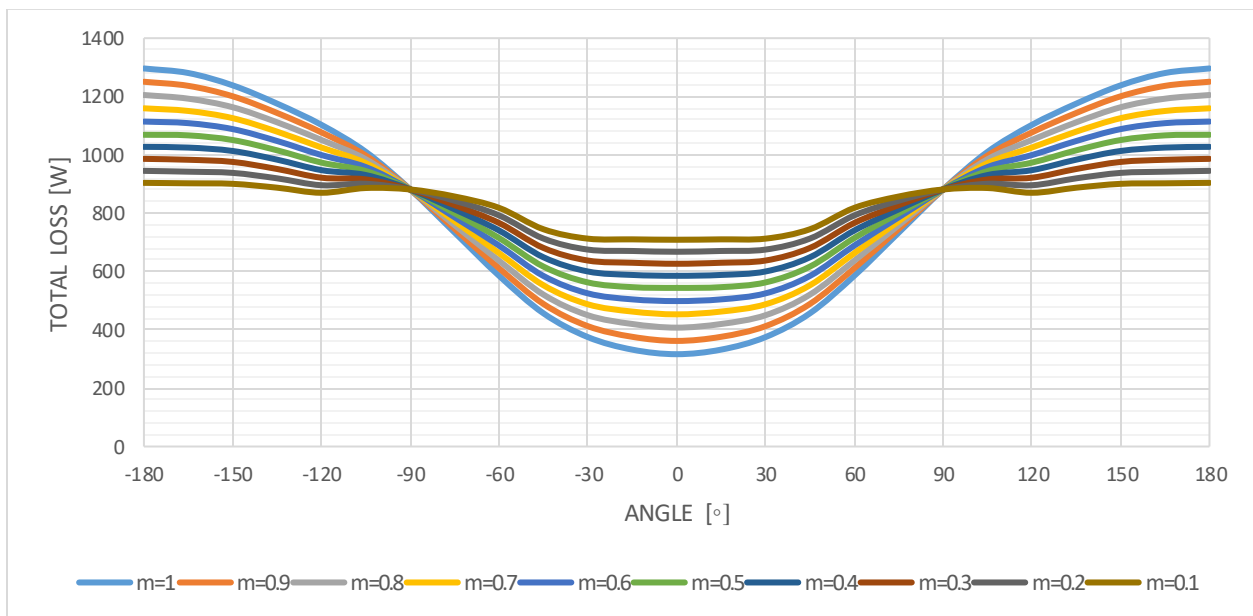


Figure 2. 15. Diode Total Losses for range of θ and m values

Similar to conduction losses, total average power losses per individual switch reach maximum value at unity power factor operation and modulation index $m=1$. Transistor peak average losses occur at active power flow directed towards grid, while diode peak losses occur at opposite power flow towards inverter. Peak power losses of individual switches are important for

maximum junction temperature estimation due to temperature rise over resistances R_{jc} and individual R_{cs} . On the other hand, common thermal resistance R_{csm} and R_{sa} do not form temperature rise based on the power losses of individual switches, but based on the summarized losses of all the switches inside the module, and all the modules mounted onto the heatsink. For the exemplary case of the Half H Bridge module with thermal model shown in Figure 2.13, temperature rise across the common thermal resistances is dictated by the total power loss of pair of transistors and diodes. Total average power loss per module for a full range of phase angle and modulation index values is presented in Figure 2.16.

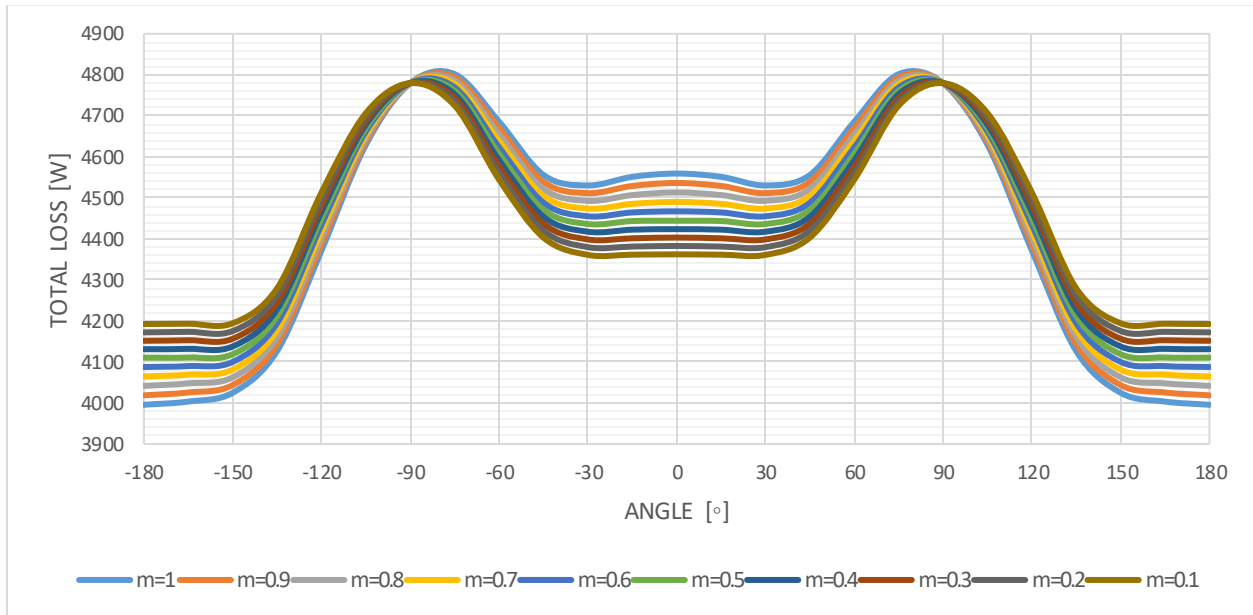


Figure 2. 16. Module Total Losses for range of θ and m values

Module power losses show a drastically different power loss distribution as opposed to individual switches. Firstly, module level power losses show very low dependence on the modulation index value across all the phase angle values. Secondly, peak power losses occur around PF=0 condition, depending on the actual module parameters. That basically means that reactive power operating condition of MTI dictates the maximum power loss condition for power modules operating under DDPWM. The reason for such kind of distribution lies in the fact that at

PF=0 condition switching losses are maximized and conduction losses show solid values for both transistor and diode. Finally, with the actual distribution of power losses per switch as well as on the module level, it is possible to calculate the junction temperatures of individual switches. In order to obtain steady state transistor and diode temperature rise over ambient, all thermal resistance parameter values from Figure 2.13 are required. For the exemplary case, parameters have been extracted based on the state of the art design as follows:

Thermal Resistance	Value
R_{jci}	17.3 K/kW
R_{csi}	5.4 K/kW
R_{jcd}	28.3 K/kW
R_{csd}	7.2 K/kW
R_{cSM}	6 K/kW
R_{sa}	10 K/kW

Table 2. 3.: Thermal Resistance Values

Based on thermal resistances and individual and total power loss distribution per module, transistor and diode junction temperature rise over ambient is shown if Figure 2.17 and 2.18 respectively.

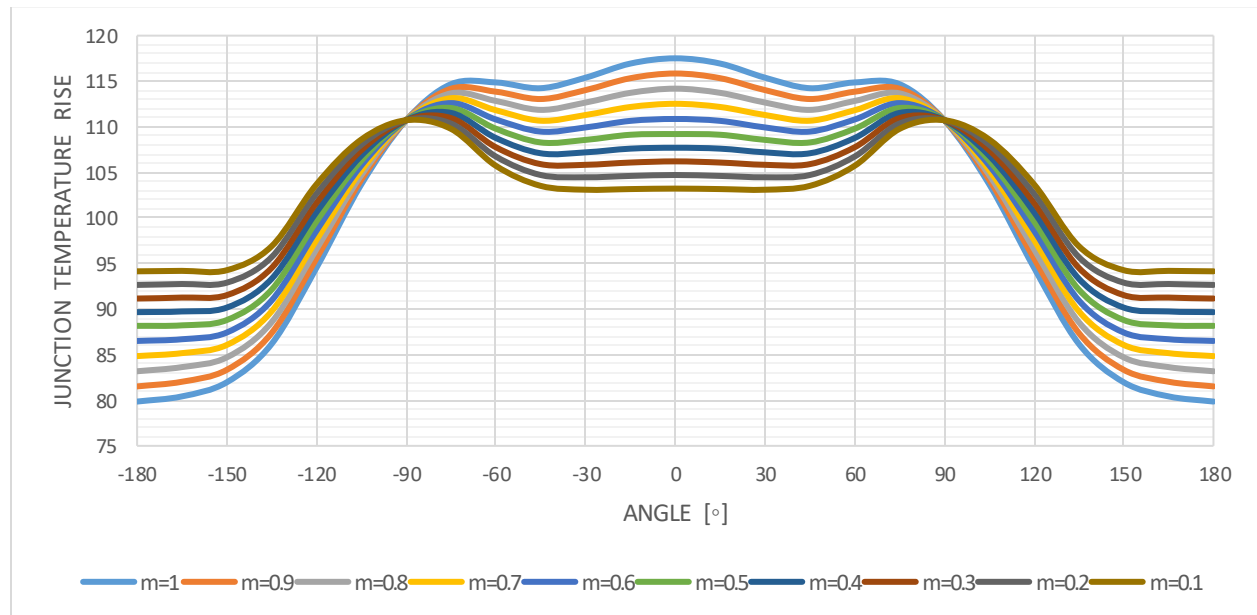


Figure 2. 17. Transistor Junction Temperature Rise for range of θ and m values

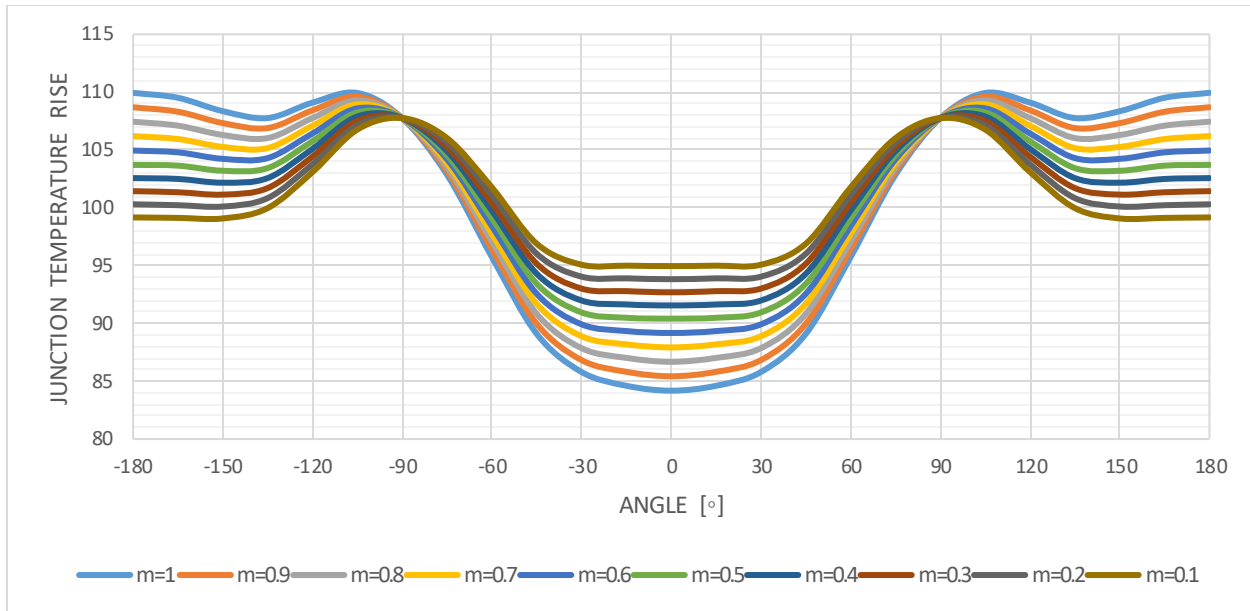


Figure 2.18. Diode Junction Temperature Rise for range of θ and m values

Figure 2.17 shows that the highest junction temperature rise for transistor occurs at unity power factor operation and maximum modulation index, which is in accordance with individual transistor loss distribution shown in Figure 16. However, the temperature rise distribution remains high as the angles value is moving towards reactive power operation, which is a consequence of the highest total module loss distribution around $\pm 90^\circ$ operation. Therefore, for design cases where common thermal resistances R_{cSM} and R_{sa} have relatively high values in respect to R_{jc} and R_{cs} , and where switching losses are increased, transistor temperature rise may occur around reactive power support conditions of MTI. As per Figure 2.18, that is exactly the case with diode, where the maximum junction temperature rise occurs at power factor values close to zero. It is also important to point out that in this particular case, maximum junction temperature rise occurs with transistors, as oppose to diodes. However, that is very much dependent on the given set of parameter values, which in certain design cases can result in higher junction temperature rise in diodes.

2.5. Harmonics Performance of PWM Modulator

2.5.1. Linear Region Operation of PWM Modulator

Due to the reactive power support and operation under soft line impedance requirements, MTI needs to operate at higher dc voltage levels than standard active front end rectifier, as per (3.5.) and (3.6.). Higher DC bus requirements dictate higher switching losses of the power module along with the higher filter inductor and DC bus capacitor losses under certain operating conditions. In order to keep thermal stress on power structure components down, it is desired to operate with a minimal dc-link voltage level that will allow operation at required power levels. DC link voltage levels are limited by operation of the MTI within the linear region of the modulator which depends on the voltage utilization level of the inverter defined thru modulation index m . For simplification purposes, modulation index presented in this work is defined differently than what can be found in common literature, where six pulse inverter waveforms are used as a reference [12]. Modulation index m is defined in this work as the ratio of the magnitude of fundamental component of the line to line inverter output voltage V_{fu} to given DC bus voltage V_{dc} :

$$m = \frac{V_{fu}}{V_{dc}} \quad (2.21.)$$

Linear region limit for triangle carrier based family of PWM techniques, is defined as the point where magnitude of the modulation signal becomes greater than the carrier peak value. Passing the linear region results in a nonlinear relation between modulation signal and actual output voltage. For Sine - Triangle PWM modulation, linear range ends at $m = 0.865$. For third harmonic injection PWM, linear region limit occurs at 0.971. For Space vector modulation and all

the discontinuous PWM modulation techniques, linear range is extended to $m = 1$, based on [2], [13].

$m = 1$ represents a theoretical limit for the linear region of the modulator, but it may be practically reduced as a consequence of dead time and minimum pulse width time implemented as part of the PWM technique, as well as due to rise and fall time and voltage drops across semiconductor switches, as per equations (2.50.) and (2.51.). From (2.50.) and (2.51.) it can be concluded that DPWM methods have superior voltage linearity characteristics for applications that operate at or around $PF = 1$. However, voltage linearity limitation is defined under $PF = 0$ condition when inverter is supplying reactive power, since that requires highest modulation index m value. This operating condition is shown in figure 2.66. and it results in the actual voltage fundamental increase on the output, thus effectively extending the linear region.

For MTI utilizing DPWM or SVPWM modulation technique, minimum theoretical DC bus voltage $V_{dc\ min}$ level required for operation within linear region of the modulator needs to be kept below the level of magnitude of output AC line - line voltage.

$$V_{dc\ min} = V_{ln}\sqrt{2}\sqrt{3} \quad (2.22.)$$

$V_{dc\ min}$ represents the highest DC bus voltage output of a 3 phase full bridge rectifier at no load condition.

For Example, if the phase to neutral inverter output voltage *RMS* value is 220V, the following numbers are calculated:

$$V_{dc\ min} (DPWM) = 220V\sqrt{2}\sqrt{3} = 537V \quad (2.23.)$$

$$V_{dc\ min} (SPWM) = 620V \quad (2.24.)$$

2.5.2. Low Order Harmonics of PWM Modulator

Power converters convert electrical energy from one parametric level to another by switching two state semiconductor-based electronic switches in a predefined manner. This switching process called modulation has an aim to optimize operation of the converter based on target criteria. Considered Microgrid Tie Inverter uses three phase two level VSI in order to produce target output voltage for given operating point. It uses pulse width modulation (PWM) for controlling the AC output, which varies the duty cycle of the converter at high frequency to achieve a target average low-frequency output voltage. Unfortunately, output voltage control is accompanied by undesirable harmonics that come as a result of switching process. Various modulation techniques create trains of switched pulses that have the same fundamental volt-second average, but they also contain unwanted harmonic components. Harmonic analysis is necessary in order to quantify the amount of undesirable harmonics created during modulation process. A useful and well established method for comparing effectiveness of modulation process is by comparing the distortion of output voltage in terms of unwanted harmonic components in respect to ideal sine waveform. Given the output voltage of an inverter $v(t)$ as a periodic function with period T , the root-mean-square (RMS) value of the function is:

$$V_{rms} = \sqrt{\frac{1}{T} \int_0^T v(t)^2 dt} \quad (2.25.)$$

$v(t)$ can be represented by the Fourier series since it is a periodic function:

$$v(t) = V_0 + V_1 \cos(\omega_1 t) + V_2 \cos(2\omega_1 t) + V_3 \cos(3\omega_1 t) + \dots \quad (2.26.)$$

By combining (2.25.) and (2.26.) with some rearrangement and manipulation, leads to the definition of the total harmonic distortion (THD) of the output voltage:

$$THD = \sqrt{\left(\frac{V_0}{V_{1,rms}}\right)^2 + \sum_{n=2,3,\dots}^{\infty} \left(\frac{V_{n,rms}}{V_{1,rms}}\right)^2} \quad (2.27.)$$

For low order harmonic study it is useful to analyze performance of only a certain set of harmonics, as oppose to a full spectrum. Also, in order to provide fair comparison across full modulation range, it useful to always use rated fundamental voltage as a reference. Normalized selective total harmonic distortion (NSTHD) is a measure that considers both requirements, and is defined for first i harmonics as:

$$NSTHD50 = \sqrt{\left(\frac{V_0}{V_{1f,rms}}\right)^2 + \sum_{n=2,3,\dots}^{50} \left(\frac{V_{n,rms}}{V_{1f,rms}}\right)^2} \quad (2.28.)$$

In a voltage source inverter system, output voltage is always a controlled variable. However, output current is typically of more interest for the application due to its relation to the output power control. Total harmonic distortion (THD) of the output current is defined in a similar fashion to output voltage as:

$$THD = \sqrt{\left(\frac{I_0}{I_{1,rms}}\right)^2 + \sum_{n=2,3,\dots}^{\infty} \left(\frac{I_{n,rms}}{I_{1,rms}}\right)^2} \quad (2.29.)$$

Since the current waveform is dependent on the load impedance it is hard to characterize it in advance. In many applications load can be approximated by an inductance, which leads to a weighted total harmonic distortion (WTHD) definition:

$$WTHD = \frac{\sqrt{\sum_{n=2}^{\infty} \left(\frac{V_n}{n}\right)^2}}{V_1} \quad (2.30.)$$

WTHD basically represents a normalized value of the THD of the output current based on the load inductance, and is a very elegant way of making a quantifiable connection between voltage and current harmonics in an application. However, WTHD cannot be used in MTI analysis due to the fact that the inverter is connected to the microgrid thru a third order LCL low pass filter which does not have a linear impedance characteristic throughout the frequency range. Also, due to a resonant impedance characteristic, equivalent impedance values become very low around resonance frequencies, thus creating an even more complex impedance characteristic.

In order to evaluate THD for a certain type of PWM, determination of the harmonic frequency components of a PWM switched phase leg output is necessary. Analytical solution that is most often used in literature for identifying harmonic component in PWM was first developed in [14] based on previous work in [15] and [16]. The analysis process assumes the existence of two time variables $C(t)$ and $R(t)$ representing high frequency carrier waveform and low frequency reference signal waveform.

$$C(t) = \omega_c t + \rho_c \text{ and } R(t) = \omega_r t + \rho_r$$

where

$$\omega_c = \frac{2\pi}{T_c} = \text{carrier angular frequency}$$

$$\rho_c = \text{carrier phase angle}$$

$$\omega_r = \frac{2\pi}{T_r} = \text{reference angular frequency}$$

$$\rho_r = \text{reference phase angle}$$

From Fourier transform theory [17], any time-varying function can be expressed as a summation of harmonic components. Modulated voltage waveform $F(t)$, which is double time variable controlled waveform, can be expressed as:

$$\begin{aligned}
F(t) = & \frac{A_{00}}{2} + \sum_{q=1}^{\infty} [A_{0q} \cos(q[\omega_r t + \rho_r]) + B_{0q} \sin(q[\omega_r t + \rho_r])] \\
& + \sum_{p=1}^{\infty} [A_{p0} \cos(p[\omega_c t + \rho_c]) + B_{p0} \sin(p[\omega_c t + \rho_c])] \\
& + \sum_{p=1}^{\infty} \sum_{\substack{q=-\infty \\ (q \neq 0)}}^{\infty} [A_{pq} \cos(p[\omega_c t + \rho_c] + q[\omega_r t + \rho_r]) \\
& + B_{pq} \sin(p[\omega_c t + \rho_c] + q[\omega_r t + \rho_r])] \quad (2.31.)
\end{aligned}$$

Where each of additive terms represent DC Offset, Fundamental Components and Baseband Harmonics, Carrier Harmonics and Sideband Harmonics respectively, p represents the carrier index variable and q represents the baseband index variable. Therefore, the h -th harmonic component is defined as $h = p \frac{\omega_c}{\omega_r} + q$.

Values p and q define the q -th sideband harmonic in the group of harmonics that are located around the p -th carrier harmonic. Special group of harmonics called baseband harmonics occur for $p = 0$, where the harmonic frequencies are defined by q alone. Another special group called carrier harmonics occur for $q = 0$, where the harmonic frequencies are defined by p alone. The magnitudes of the harmonic components are represented by A_{pq} and the B_{pq} coefficients, which must be calculated for each set of values of p and q for each PWM scheme under consideration.

Equations:

$$A_{pq} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x, y) \cos(px + qy) dx dy \quad (2.32.)$$

$$B_{pq} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x,y) \sin(px + qy) dx dy \quad (2.33.)$$

Represent a general Fourier integral that has to be adapted for particular PWM pattern and solved in order to determine A_{pq} and B_{pq} values.

In general, if ω_r and ω_c are not an integer ratio, the resulting switched pulse train waveform will not be periodic within single fundamental period cycle, but it will be over a certain number of periodic cycles of the fundamental reference waveform.

Determination of the harmonic frequency components of a PWM switched output waveform using double Fourier Integral Analysis is quite complex and time demanding task. A derivation process for A_{pq} and B_{pq} for basic PWM techniques is presented in [18], from which a general analytical solution can be derived for particular DPWM of interest. Later in this chapter it is shown that DDPWM at $\theta = 0^\circ$ represents the worst case modulation from harmonics magnitude perspective, so a general analytical solution is derived using same principles from [18] as:

$$\begin{aligned}
A_{pq} = \frac{4V_{dc}\omega_c}{h\omega_r\pi^2} & \left(\frac{\pi}{3} J_q \left(h \frac{\omega_r}{\omega_c} \pi m \right) \cos \left(\frac{q\pi}{6} \right) \sin \left[\left(p \right. \right. \right. \\
& + q \left. \left. \left. \frac{\pi}{2} \right] \cos \left(h \frac{\omega_r}{\omega_c} \frac{\pi}{2} \right) + \frac{1}{2q} \sin \left(\frac{q\pi}{6} \right) \left(\sin \left[\left[\left(h \frac{\omega_r}{\omega_c} + p \right) \frac{\pi}{2} \right] \right] - \cos(q\pi) \sin \left[\left(h \frac{\omega_r}{\omega_c} - p \right) \frac{\pi}{2} \right] \right) \right) \\
& + \frac{1}{q} \sin \left(\frac{q\pi}{6} \right) \cos \left(\frac{q\pi}{3} \right) J_0 \left(h \frac{\omega_r}{\omega_c} \pi m \right) \left(\sin \left[\left(h \frac{\omega_r}{\omega_c} + p \right) \frac{\pi}{2} \right] \cos(q\pi) - \sin \left[\left(h \frac{\omega_r}{\omega_c} - p \right) \frac{\pi}{2} \right] \right) |_{q \neq 0} \\
& + \sum_{\substack{k=1 \\ k \neq -q}}^{\infty} \frac{1}{q+k} J_k \left(h \frac{\omega_r}{\omega_c} \pi m \right) \sin \left[\left(q+k \right) \frac{\pi}{6} \right] \cos \left[\left(2q+k \right) \frac{\pi}{6} \right] \left(\cos[(q+k)\pi] \sin \left[\left(k+h \frac{\omega_r}{\omega_c} \right. \right. \right. \\
& + p \left. \left. \left. \frac{\pi}{2} \right] + \sin \left[\left(k-h \frac{\omega_r}{\omega_c} + p \right) \frac{\pi}{2} \right] \right) \\
& + \sum_{\substack{k=1 \\ k \neq q}}^{\infty} \frac{1}{q-k} J_k \left(h \frac{\omega_r}{\omega_c} \pi m \right) \sin \left[\left(q-k \right) \frac{\pi}{6} \right] \cos \left[\left(2q-k \right) \frac{\pi}{6} \right] \left(\cos[(q-k)\pi] \sin \left[\left(k+h \frac{\omega_r}{\omega_c} \right. \right. \right. \\
& + p \left. \left. \left. \frac{\pi}{2} \right] + \sin \left[\left(k-h \frac{\omega_r}{\omega_c} + p \right) \frac{\pi}{2} \right] \right) \right) \quad (2.34.)
\end{aligned}$$

Where $J_y(z)$ is Bessel functions of the first kind with order y and argument z . Due to obvious complexity and lack of intuitiveness in usage of general analytical solution for harmonic coefficient A_{pq} , it will not be further considered in this work.

Alternative method for determining harmonic values of a PWM switched waveform is using a Fast Fourier Transform analysis of a simulated time-varying switched waveform. FFT is an algorithm developed for computing discrete Fourier transformation on discrete signals by using factorization into sparse matrices [19][20]. Using FFT over classical Fourier Transformation offers the benefits of expediency and reduced mathematical effort. Fast Fourier Transform (FFT) method is very sensitive to periodicity of the overall waveform and the resolution step time of the simulation program. Therefore, harmonic investigations of various PWM strategies using FFT

analysis are only effective for integer carrier to fundamental ratios, particularly in cases where the small magnitude baseband and sideband harmonics are the primary focus [18]. Due to the fact that harmonic distortion limits defined in IEEE-519-2014 standard define harmonic limits in the current waveform at PCC up to 50th harmonic only, the primary focus of the harmonics study would be on the first 50 harmonics. Another good reason is that these low order harmonics (<50) potentially all fall within the current controller frequency bandwidth as well as filter resonance frequency range, thus being very important to quantify for performance reasons.

As described previously, PWM is achieved by switching at the intersection of a reference signal waveform and high frequency carrier by comparing a low-frequency target reference waveform against a high-frequency carrier waveform. Two major carrier waveform signal types used are the sawtooth and triangle, with modulation termed trailing edge and double edge, respectively. Double edge modulation has shown to have an intrinsic advantage over trailing edge modulation by eliminating odd harmonic sideband components around odd multiples of the carrier fundamental, and even harmonic sideband components around even multiples of the carrier fundamental [18]. Since MTI is to be implemented with minimal unwanted harmonic impact, double edge modulation will be considered.

It is important to point out that, even though possible, non-integer frequency ratios between carrier and fundamental are highly undesirable to use because they introduce subharmonics below the fundamental frequency. Any harmonics that exist in the subharmonic region of non-integer ratio modulators represent low order carrier sideband components, that may, depending on the roll off characteristic of sideband harmonics of certain modulator type, represent a highly unwanted component.

In general, three phase PWM modulator for VSI uses naturally or regular sampled PWM process applied to a three-phase VSI, with the three sinusoidal references displaced in time by 120 with addition of common mode voltage waveform V_{cm} .

$$v_a^* = \frac{V_{dc}}{2} \left[\frac{2}{\sqrt{3}} m \cos (\omega_0 t) + V_{cm} \right] \quad (2.35)$$

$$v_b^* = \frac{V_{dc}}{2} \left[\frac{2}{\sqrt{3}} m \cos (\omega_0 t - 2\frac{\pi}{3}) + V_{cm} \right] \quad (2.36.)$$

$$v_c^* = \frac{V_{dc}}{2} \left[\frac{2}{\sqrt{3}} m \cos (\omega_0 t + 2\frac{\pi}{3}) + V_{cm} \right] \quad (2.37.)$$

where m represents modulation index and the reference waveforms are defined with respect to the DC bus mid-point. The fundamental target three-phase line-line output voltages are given by the differences between the phase leg voltages.

$$v_a^* = v_a^* - v_b^* = m \cos \left(\omega_0 t + \frac{\pi}{6} \right) \quad (2.38.)$$

$$v_b^* = v_b^* - v_c^* = m \cos \left(\omega_0 t - \frac{\pi}{2} \right) \quad (2.39.)$$

$$v_c^* = v_c^* - v_a^* = m \cos \left(\omega_0 t + \frac{5\pi}{6} \right) \quad (2.40.)$$

Common mode components added to the fundamental voltages reduce the peak size of envelope of each phase voltage, but they do not affect the line to line fundamental output voltage, since the common mode voltages cancel between the phase legs.

Most basic three phase modulation called SPWM does not use common mode waveform, but only fundamental references. Lack of common mode signal in the reference limits the linear range of modulator operation to $m = 0.865$. Other PWM techniques can increase modulation index to $m = 1$ and still maintain linear operation of modulator, which is achieved by adding

appropriate common mode reference signal to the fundamental reference waveform. Despite superior low order harmonic performance [21], limited linear range of operation represents a major constraint for using SPWM in MTI, and therefore it will not be further investigated.

Modulation index m is very practical to use for harmonic analysis, since it represents a per unit value of fundamental line to line voltage harmonic, which becomes known and does not need to be presented in the spectra anymore.

The first modulation strategy to perform low order harmonic analysis on is called third harmonic injection (THI) modulation. It uses most simple common mode signal added to the fundamental voltage waveforms, which is basically a 3rd harmonic in phase with one of the 3 phase reference fundamentals. Common mode signal magnitude of $1/6^{\text{th}}$ of the fundamental has shown to cover the full linear range up to $m = 1$, thus providing optimal DC bus utilization [22, 23]. The expression for common mode signal is

$$V_{cm} = \frac{m}{3\sqrt{3}} \cos(\omega_0 t) \quad (2.41.)$$

Extended linear range puts THI in the same rank as space vector modulation and all the discontinuous PWM techniques in terms of DC bus utilization. Reference phase fundamental waveform, common mode waveform and resulting reference signal for THI are shown in figure 2.19.

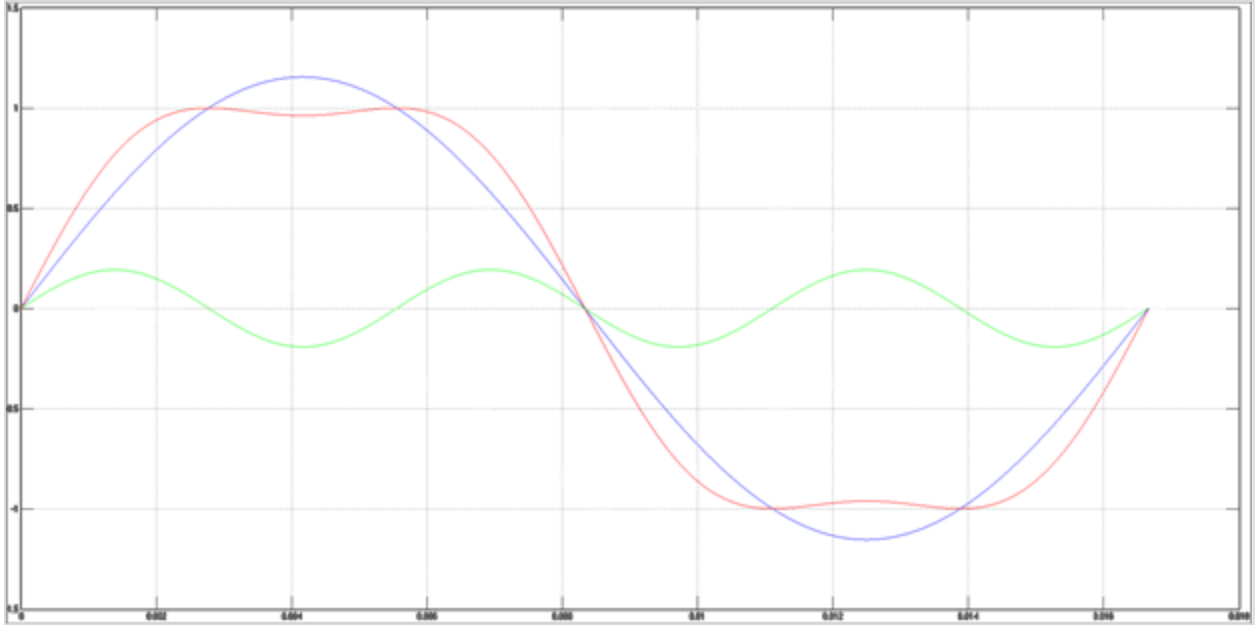


Figure 2. 19. THI Modulation – fundamental, common mode and resulting reference signal

As previously explained, in order to obtain magnitudes for each of the first 50 harmonics in PWM waveform, Fast Fourier Transform analysis has to be performed on a simulated time-varying switched waveform. A carrier to fundamental ratio of $cf=69$ was selected based on the MTI design example, and a full harmonic spectrum for various modulation indexes values is shown in Figure 2.20.

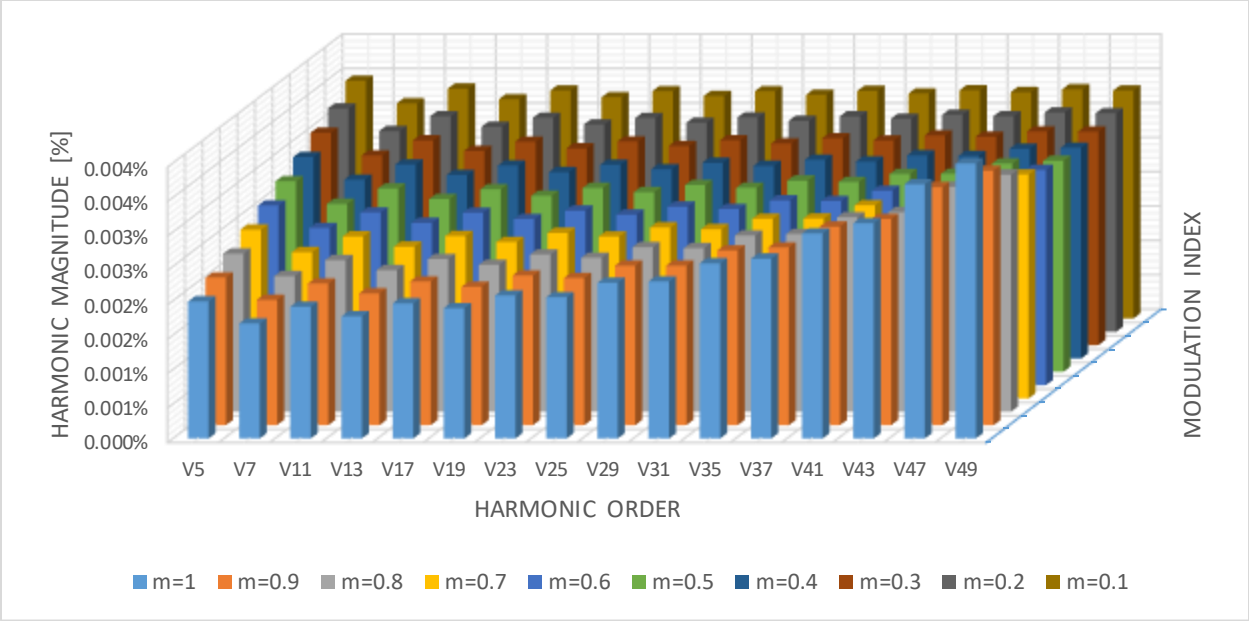


Figure 2. 20. THI Modulation – Voltage Harmonic spectrum for various m values

It is obvious that all 50 harmonics have very low magnitude, and can practically be even completely neglected. Another thing to notice is that harmonic magnitudes are very weakly dependent on the modulation index value. This makes THI a modulation of choice for applications that require good low order harmonic performance and use low cf ratio.

Next PWM modulation for consideration is space vector modulation (SVM). SVM is based on eight possible switch combinations creating 8 output voltage space vectors as per Figure 2.21.

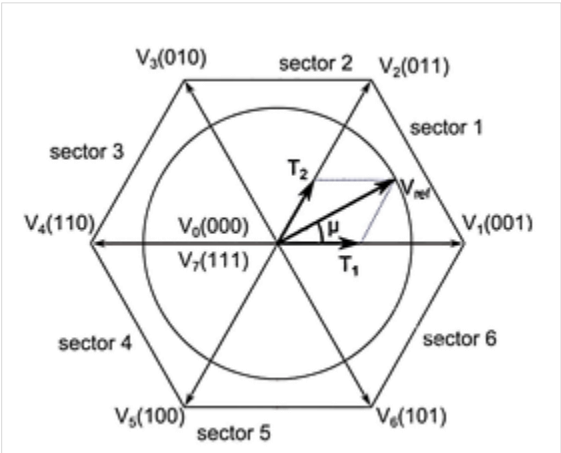


Figure 2. 21. Vector allocations for SVM.

Vectors V_0 and V_7 correspond to a shorted negative (000) and positive (111) output respectively, thus forming so called zero vectors. On the other hand, other six vectors $V_1 - V_6$ form stationary vectors called active vectors. Output voltage is formed by the summation of space vectors within one half switching period, where opportunity exists to manipulate the zero vector. The most conventional SVM implementation [24] centers the active space vectors in each half carrier period, and divides the remaining time equally between zero vectors V_0 and V_7 , which was shown to be a harmonically superior SVM variation. This SVM can be realized in equivalent SPWM implementation called Space Vector PWM (SVPWM). Figure 2.22 shows the correlation between vector times in SVM and switching pattern of SVPWM for first sector.

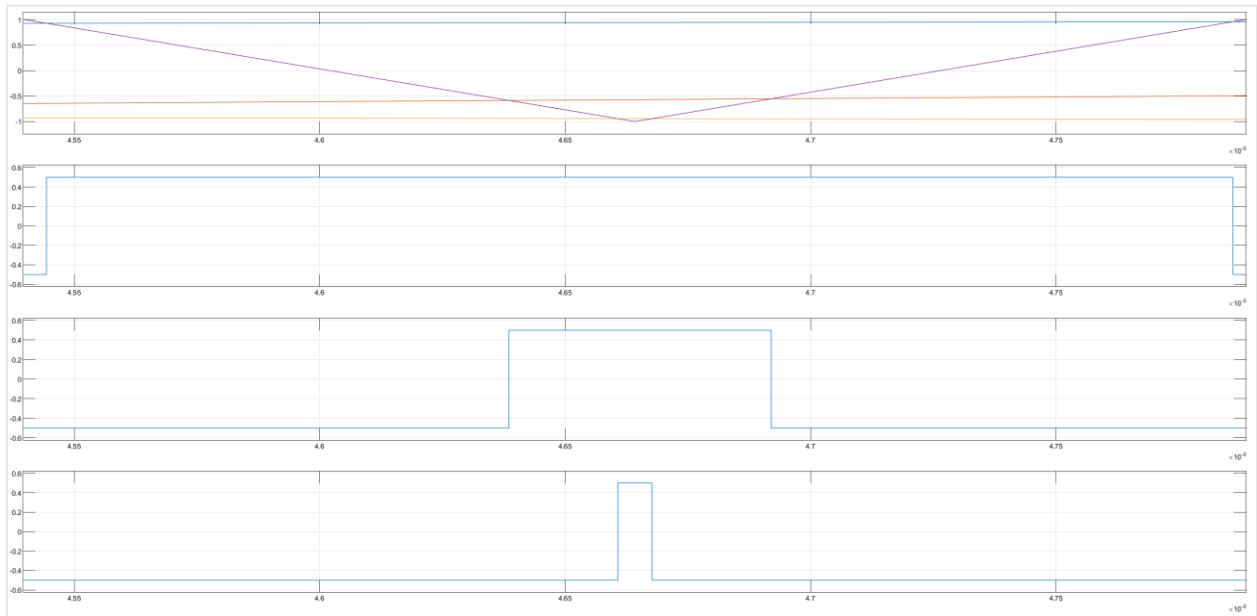


Figure 2. 22. Correlation of switching times between SVM and SVPWM.

Common mode voltage signal expression for this implementation is

$$v_{cm} = v_a^* - \frac{\max(v_a^* v_b^* v_c^*) + \min(v_a^* v_b^* v_c^*)}{2} \quad (2.42.)$$

Reference phase fundamental waveform, common mode waveform and resulting reference signal for SVPWM are shown in figure 2.23.

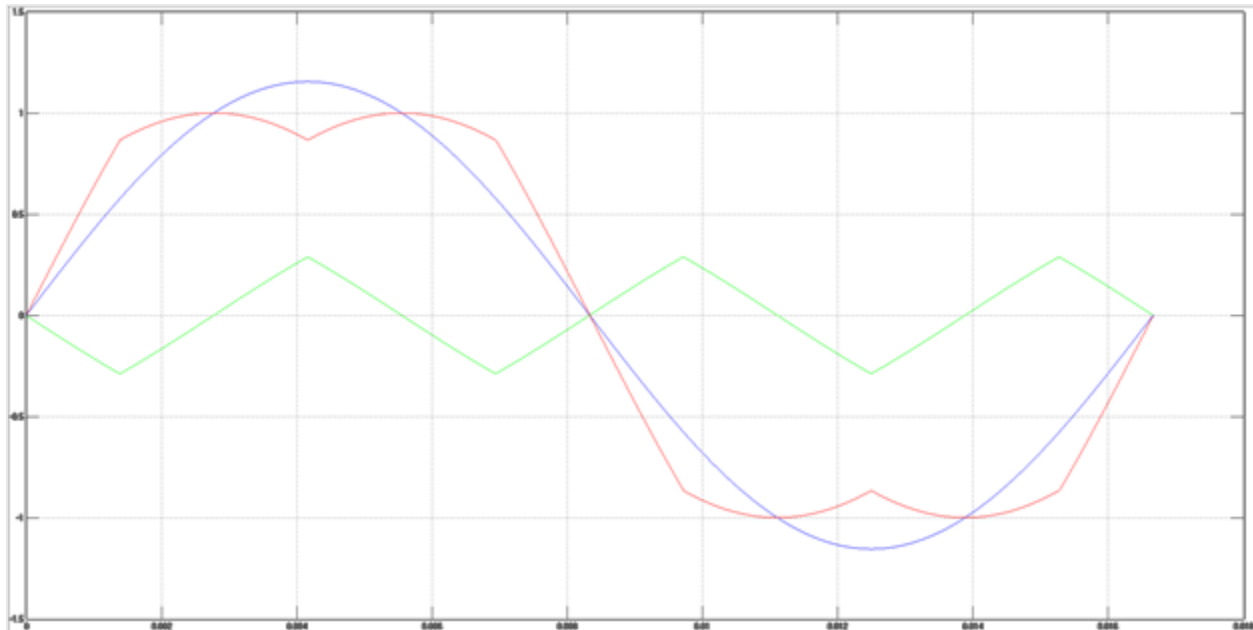


Figure 2. 23. SVPWM Modulation – fundamental, common mode and resulting reference signal

SVPWM Full harmonic spectrum for various modulation indexes and $cf = 69$ is shown in Figure 2.24.

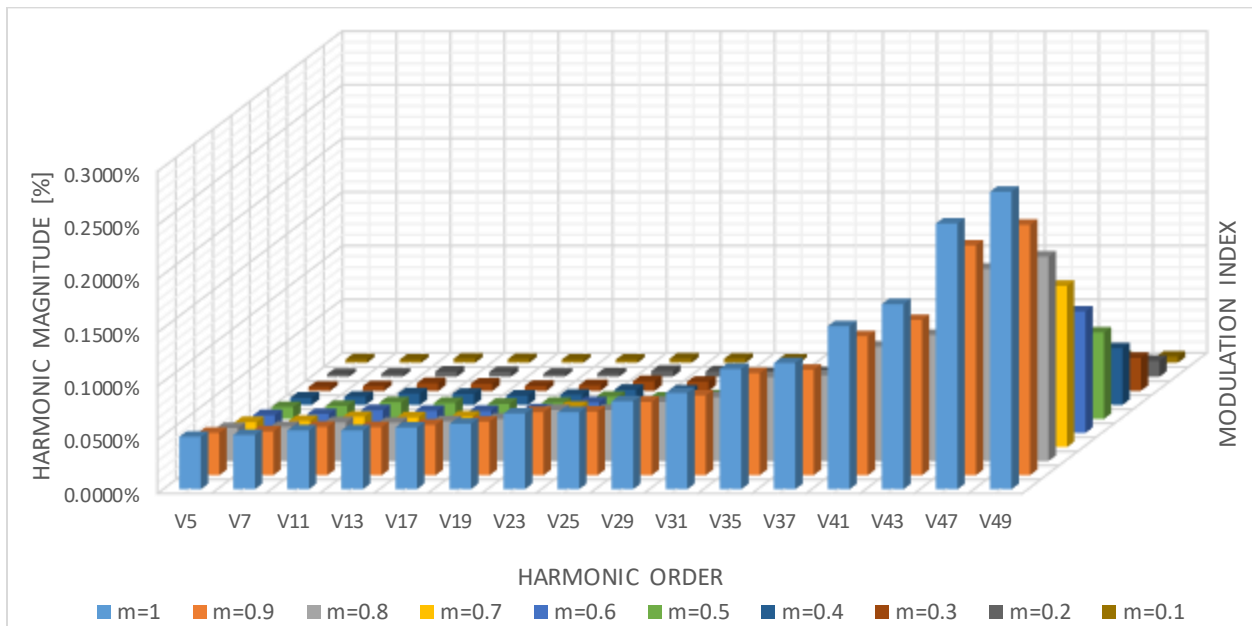


Figure 2. 24. SVM Modulation –Voltage Harmonic spectrum for various m values

From harmonic's spectrum it is shown that all 50 harmonics have significantly higher magnitude in SVPWM as compared to THI. Harmonics are highly dependent on the modulation index value, resulting in higher levels for higher modulation index values. Another point to make is that the harmonic values are increasing with harmonic order. SVPWM has an obvious disadvantage over THI in terms of low order harmonic performance, but it is worthy of pointing out that all 50 harmonics are well below 0.5% of the rated fundamental voltage, thus making it insufficiently effective only for applications with very low carrier to fundamental frequency ratios. Also, SVPWM is mostly a modulation of choice over THI in applications where sudden changes in voltage reference magnitude and frequency is required, which makes determination of the third-harmonic difficult [25].

All three modulation techniques considered so far, SPWM, THI and SVPWM represent PWM schemes where both legs in an inverter phase switch between the upper and lower DC rails at the carrier frequency. These modulation techniques represent continuous modulation, since all devices switch continuously throughout the fundamental cycle. Alternative group of modulation strategies are called discontinuous PWM (DPWM) techniques. In discontinuous modulation strategies, one set of intermediate zero space vectors (V_0 or V_7 ,) in between active space vectors within one half carrier intervals are eliminated. That provides the advantage of eliminating one switching transition in each half carrier interval, resulting in each phase leg only switching during two-thirds of each fundamental cycle equivalent to 240° . This way discontinuous modulation basically reduces the effective switching frequency for the same carrier frequency value. The major distinguishing factor between various different DPWM techniques is the distribution of 120° non-switching zone across fundamental cycle. DPWMMIN, DPWMMAX, DPWM0, DPWM1, DPWM2 and DPWM3 are the most popular DPWM strategies investigated in literature.

DPWMMIN and DPWMMAX are strategies in which one device of each phase leg is always turned on during its 120° unmodulated region, by being clamped to either negative or positive DC bus respectively. That clamped device is always conducting resulting in nonequal sharing of conduction losses and switching losses in respect to the other phase leg device. Also, exclusive clamping to either of the DC bus rails produces an asymmetric line to line voltage across a fundamental cycle, that is missing half wave symmetry, thus producing unwanted even order harmonics [26]. Reasons described above make DPWMMIN and DPWMMAX unpractical to use in MTI application.

DPWM0, DPWM1, DPWM2 and DPWM3 are discontinuous modulation strategies that balance the switching losses and provide the particular benefit of symmetrical line to line voltages by keeping each phase leg unmodulated for only 60° at a time, thus providing alternate DC bus clamping in each phase.

DPWM1 centers the nonswitching periods for each phase leg symmetrically around the positive and negative peaks of its fundamental reference voltage. DPWM2 and DPWM0 place the nonswitching period at 30° lagging and leading as compared to the fundamental voltage waveform position, respectively. DPWM3 clamps the phase legs to DC rail in two separate each 30° segments per half cycle, thus leading to twice the number of halved clamping iterations in a fundamental cycle.

Reference phase fundamental waveform, common mode waveform and resulting reference signal for DPWM0, DPWM1, DPWM2 and DPWM3 are shown in figures 2.25., 2.26, 2.27. and 2.28. respectively.

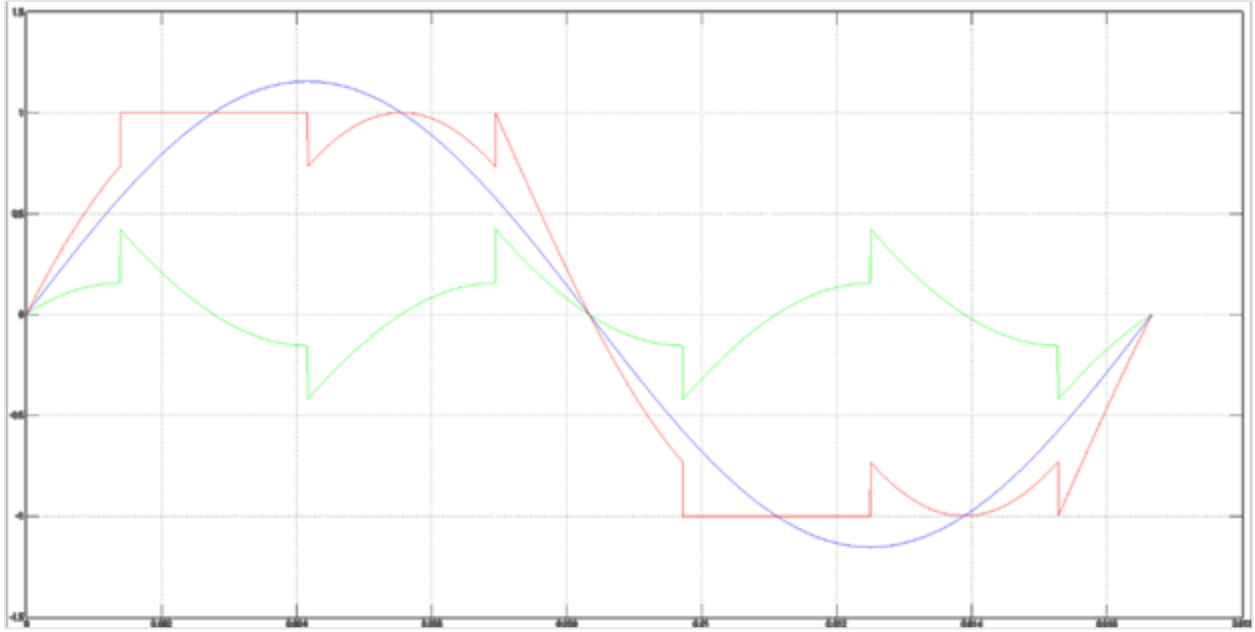


Figure 2. 25. DPWM0 Modulation – fundamental, common mode and resulting reference signal

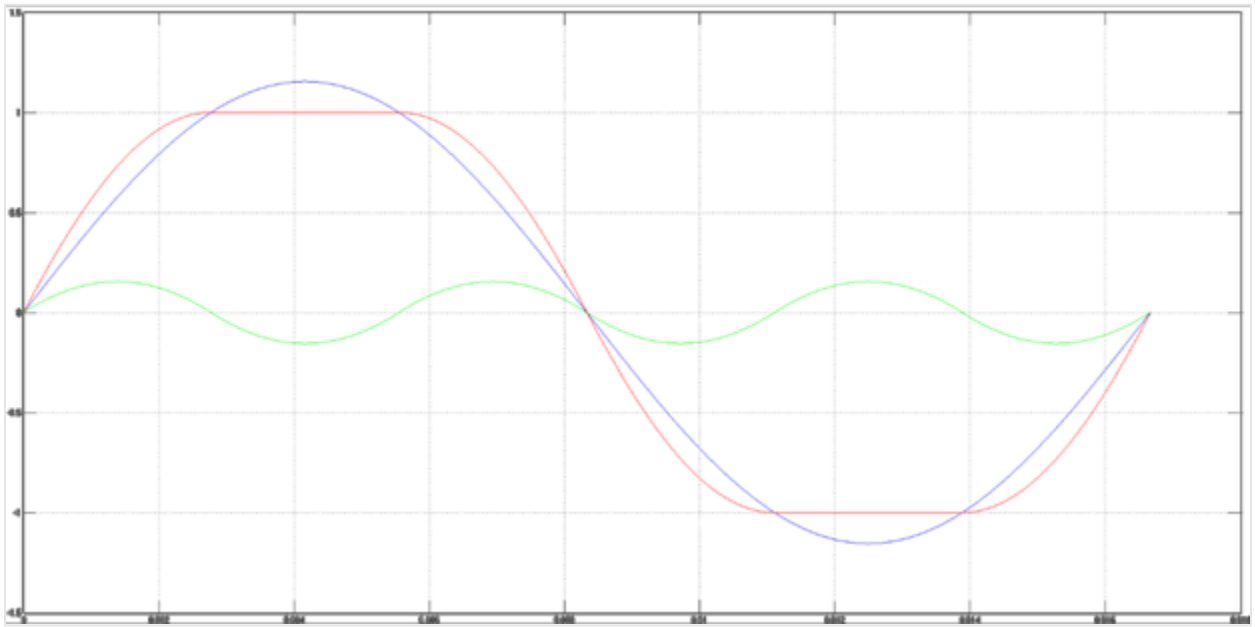


Figure 2. 26. DPWM1 Modulation – fundamental, common mode and resulting reference signal

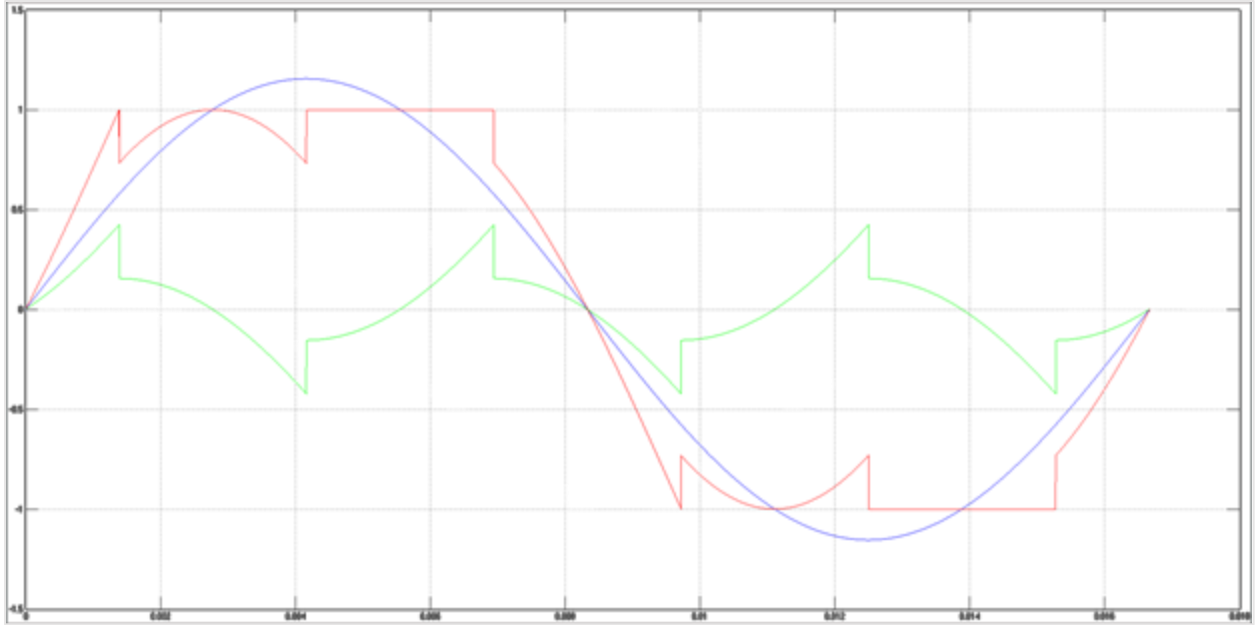


Figure 2. 27. DPWM2 Modulation – fundamental, common mode and resulting reference signal

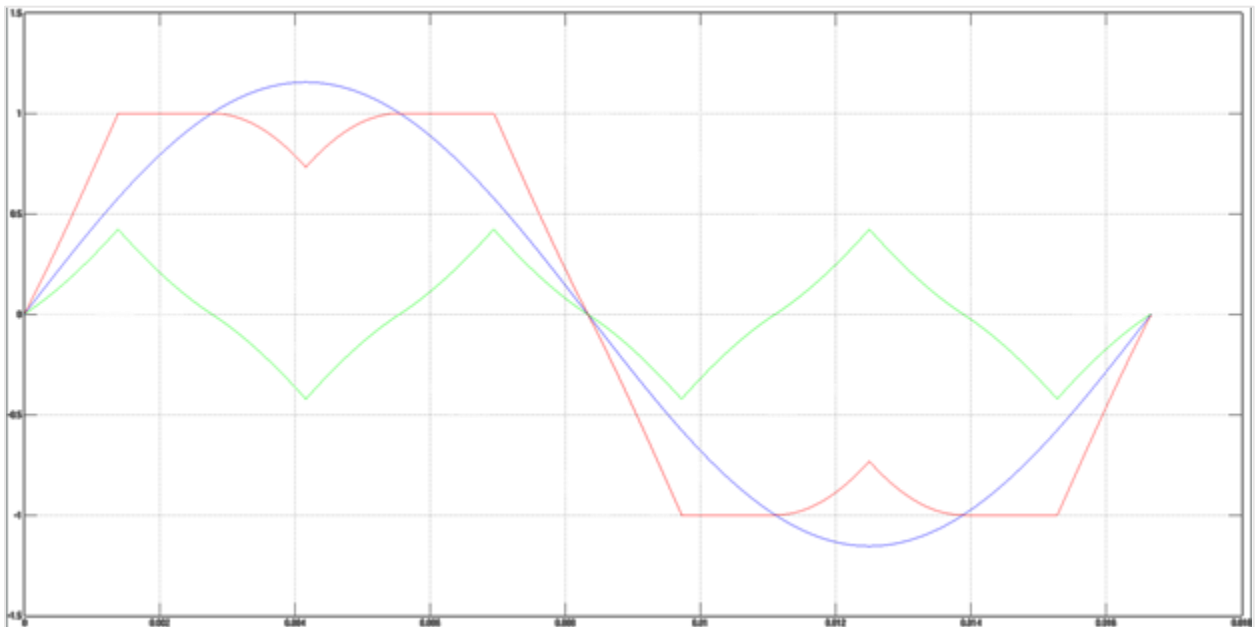


Figure 2. 28. DPWM3 Modulation – fundamental, common mode and resulting reference signal

As opposed to DPWM1 and DPWM3, which possess quarter wave symmetry of the reference waveform, DPWM0 and DPWM2 are only half wave symmetric waveforms. This is due to incorporation of nonswitching period which is purposely shifted from the center of the

fundamental voltage reference. This asymmetry does get passed on to the switched line-line voltage, creating a quarter wave asymmetry.

Full harmonic spectrum for DPWM0, DPWM1, DPWM2 and DPWM3 at various modulation indexes and a carrier to fundamental ratio of 69 is shown in Figures 2.29., 2.30., 2.31. and 2.32.

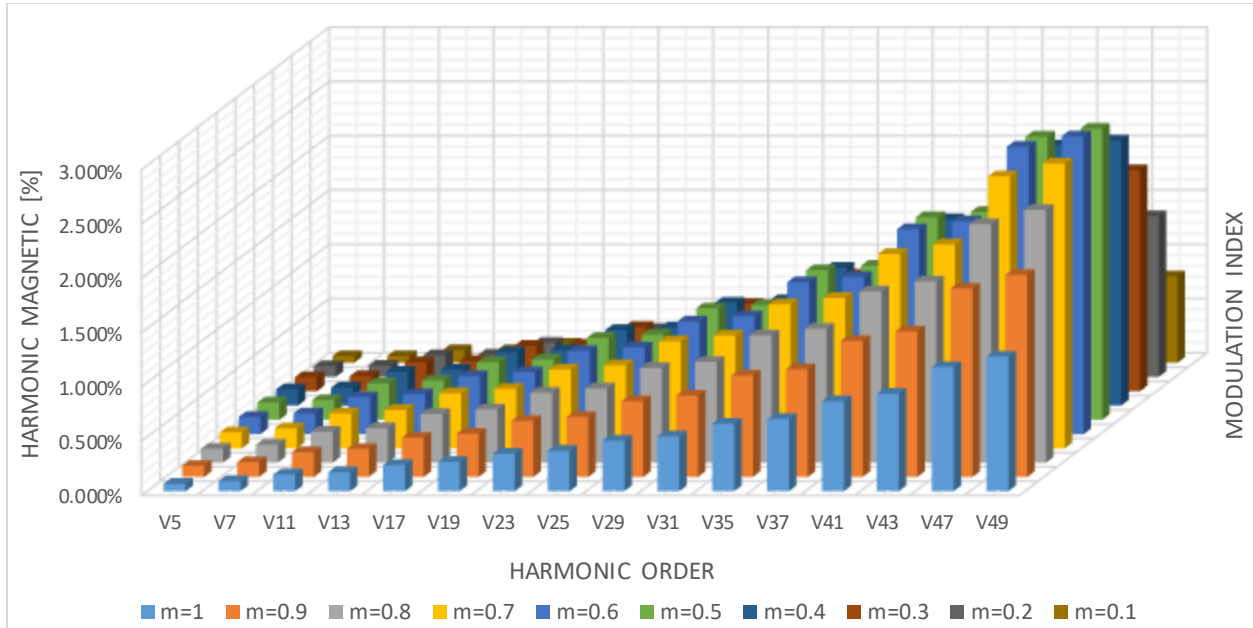


Figure 2. 29. DPWM0 Modulation – Voltage Harmonic spectrum for various m values

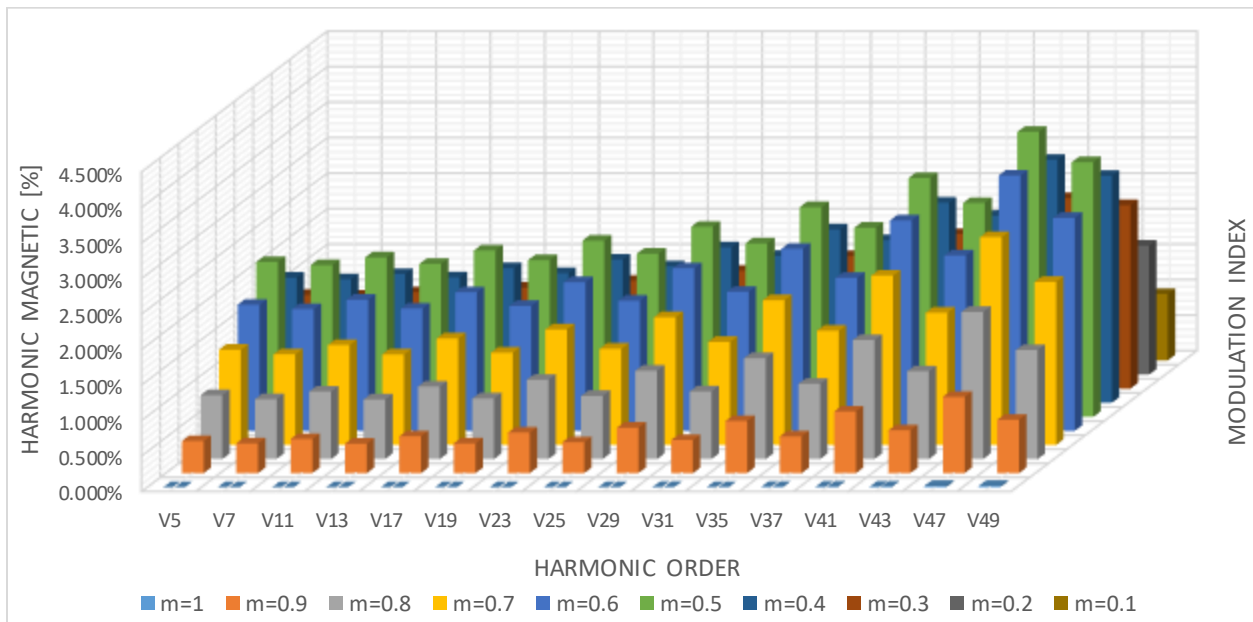


Figure 2. 30. DPWM1 Modulation – Voltage Harmonic spectrum for various m values

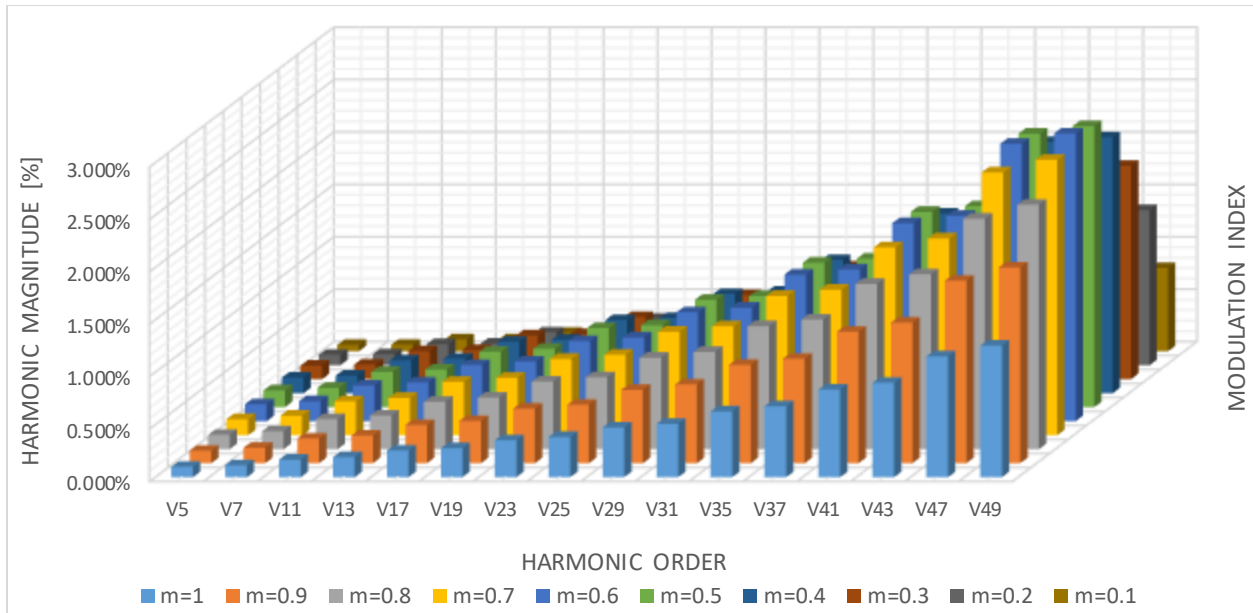


Figure 2. 31. DPWM2 Modulation – Voltage Harmonic spectrum for various m values

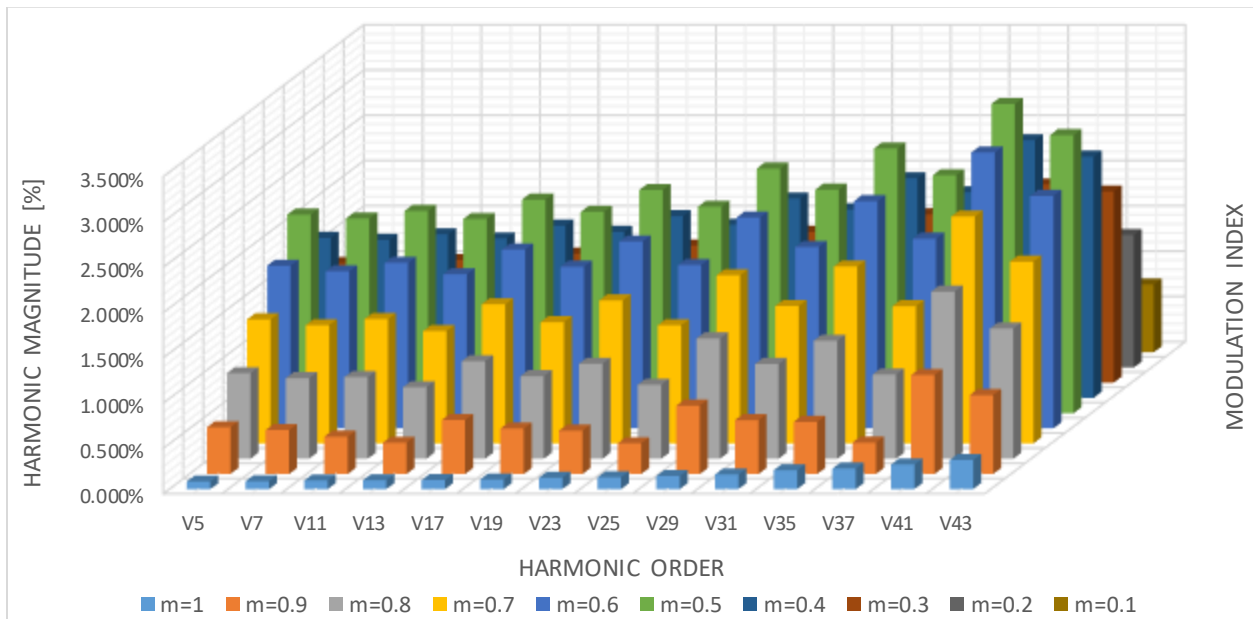


Figure 2. 32. DPWM3 Modulation – Voltage Harmonic spectrum for various m values

In order to compare the performance of the continuous and discontinuous PWM techniques covered previously, Normalized selective total harmonic distortion (NSTHD) will be used. NSTHD for first 50 harmonics across full modulation index range, at carrier to fundamental frequency ratio of $cf=69$ is shown in Figure 2.33.

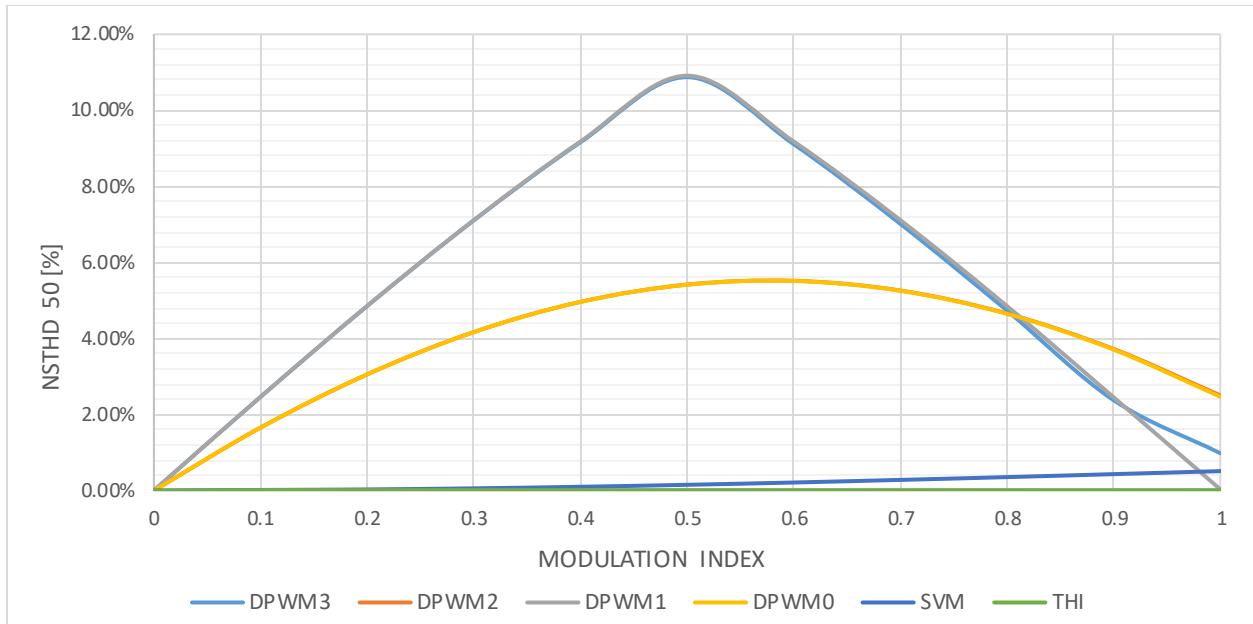


Figure 2. 33. NSTHD50 Comparison between THI, SVM and DPWM0/1/2/3 at various m values

Harmonic spectral analysis for DPWM strategies points out that all low order harmonics have drastically higher magnitude in comparison with SVPWM and THI. Also, harmonic values increase with harmonic order in a non-monotonic fashion. Harmonic values show a dependency on the modulation index value, with maximum value peaking at $m = 0.6$ for DPWM0 and DPWM2 and $m = 0.5$ for DPWM1 and DPWM3. With exception to high modulation index values, where common mode signal for DPWM1 is low triplen, DPWM1 and DPWM 3 have identical NSTHD characteristic, and highest values of all modulation techniques presented. DPWM0 and DPWM2 also have identical NSTHD characteristic, which is expected due to the fact that only phase differences exist for each individual harmonic in the spectrum.

DPWM techniques have an obvious disadvantage over continuous modulation techniques in terms of lower order harmonic performance. However, DPWM techniques are mostly used in cases where there is a demand for minimization of power losses and increased power density and efficiency of the inverter. These benefits are achieved thru reduced switching losses, which depend

on the phase shift between voltage and current. Therefore, DPWM1 performs best with no phase shift condition, since line current peaks along with fundamental voltage, and that coincides with the 60° bus clamping period for DPWM1. Same logic applies for DPWM2 and DPWM0 for 30° lagging and leading condition, respectively. DPWM3 has shown to provide reduced switching loss benefits at phase shift levels close to 90°. [27].

The rate of decay of the sideband harmonic magnitudes, so called harmonic roll-off, is much slower for Discontinuous than for Continuous PWM techniques. This occurs because the common mode injection component for DPWM contains multiple triplen harmonics of higher magnitude. Those higher order triplen components, once passed thru the modulation process, create outer sideband harmonics of high magnitude that intrude into the low frequency region. The magnitudes and frequency range of common mode triplen harmonics, along with their position in respect to the fundamental reference signal, can define levels of outer sideband harmonics. Comparison of common mode signals for THI, SVPWM and DPWM1 for carrier to fundamental ratio of 69 and modulation index of 0.6 are shown in figure 2.34. It is obvious that DPWM1 has the highest magnitude along with the highest rate of rise, thus creating highest level of triplen harmonics, which after modulation process produce the highest level of low order harmonics.

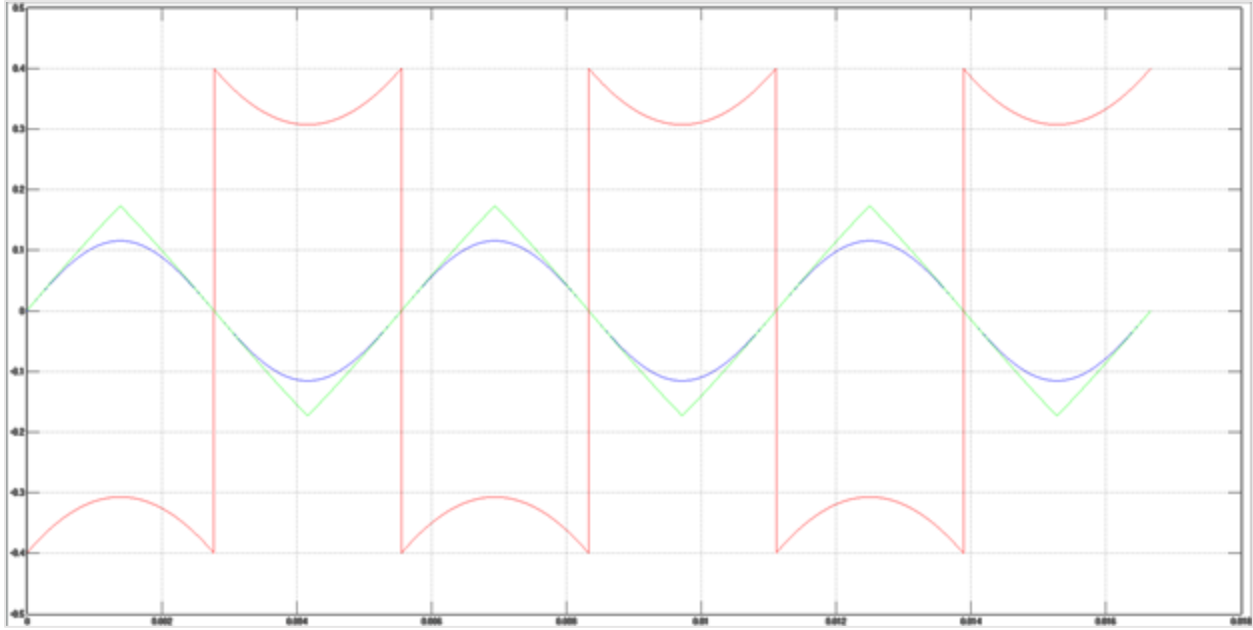


Figure 2. 34. Common Mode Signal Comparison between THI, SVPWM and DPWM1 various m values

In a three-phase system, the harmonic performance of a particular PWM technique used is reflected on the harmonics generated by the switched waveform in particular phase. However, certain harmonic cancellation may occur between switched outputs of individual phases, thus it is better to perform analysis on a phase to phase basis. However, the amount of low order harmonic cancellation that happens between two phases in a three-phase system is highly dependent on the ratio of carrier to fundamental frequency cf . Harmonic spectrum for single phase and phase to phase waveforms for three different carrier ratios $cf=43, 44$ and 45 will be investigated. Carriers were purposely selected at lower frequency such that switching frequency falls within the first 50 harmonics range. DPWM1 at $m=0.6$ is selected based on the significant value of harmonics present, and spectrum for first 50 harmonics is shown in Figure 2.35., 2.36. and 2.37. for carrier ratios cf of 43, 44 and 45 respectively.

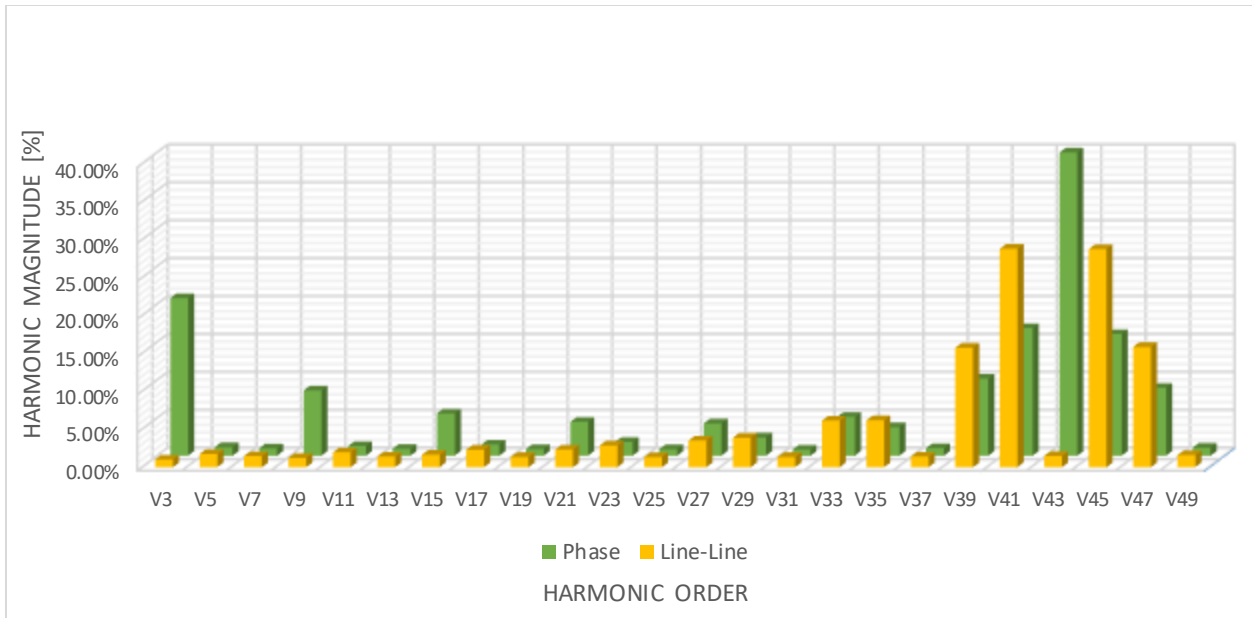


Figure 2. 35. DPWM1 at $f_c/f_f=43$ and $m=0.6$ –Voltage Harmonic spectra for phase and phase-phase waveforms

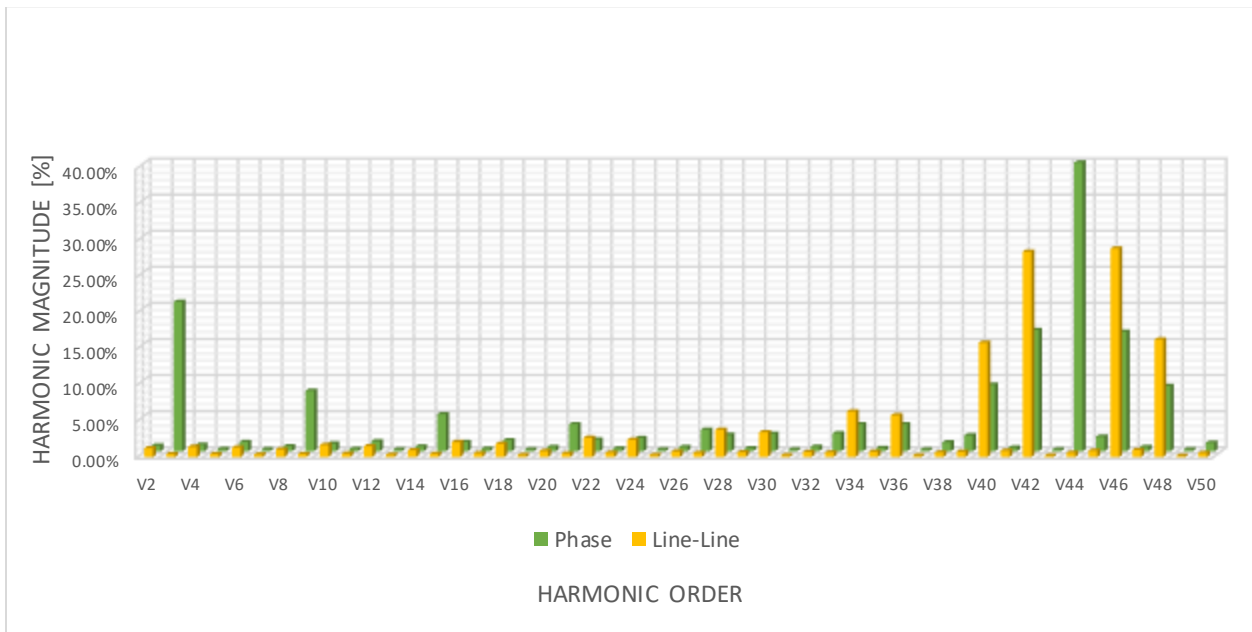


Figure 2. 36. DPWM1 at $f_c/f_f=44$ and $m=0.6$ –Voltage Harmonic spectra for phase and phase-phase waveforms

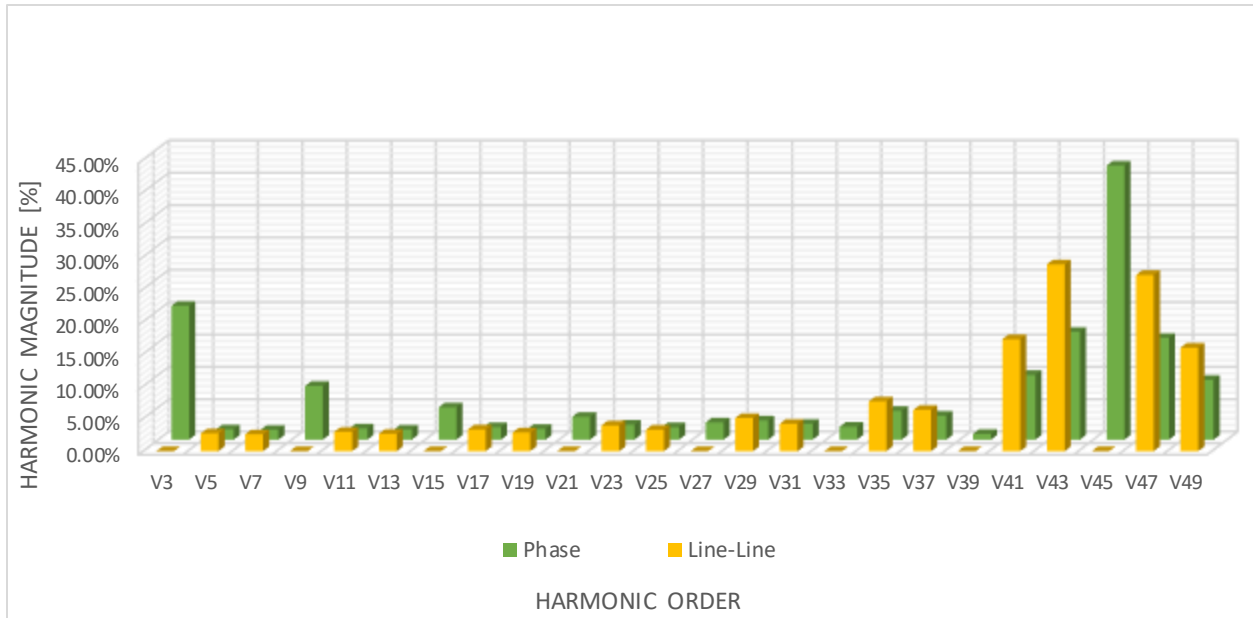


Figure 2. 37. DPWM1 at $f_c/f_f=45$ and $m=0.6$ –Voltage Harmonic spectra for phase and phase-phase waveforms

Figure 2.35., with $cf = 43$, represents a case where carrier frequency is selected as a non triplen multiple of fundamental. Due to that, it is noticeable that odd triplen sideband harmonics between phases as well as carrier harmonic do not cancel out completely, thus creating unwanted odd triplen harmonics in the spectra.

This becomes very obvious by using simple SPWM modulation with a rather extreme value of $cf = 5$, and plotting two phase reference voltage and carrier waveforms along with resulting switched output waveforms for each of the two phases, as shown in Figure 2.38. Despite the fact that all three voltage phase references are symmetrical and modulated using unique common carrier, there is a different phase difference between each of the phase references and carrier, thus creating unequal half wave symmetric pulses in phase outputs. Differences in each of the switched phase outputs create harmonics that do not fully cancel in phase to phase voltages.

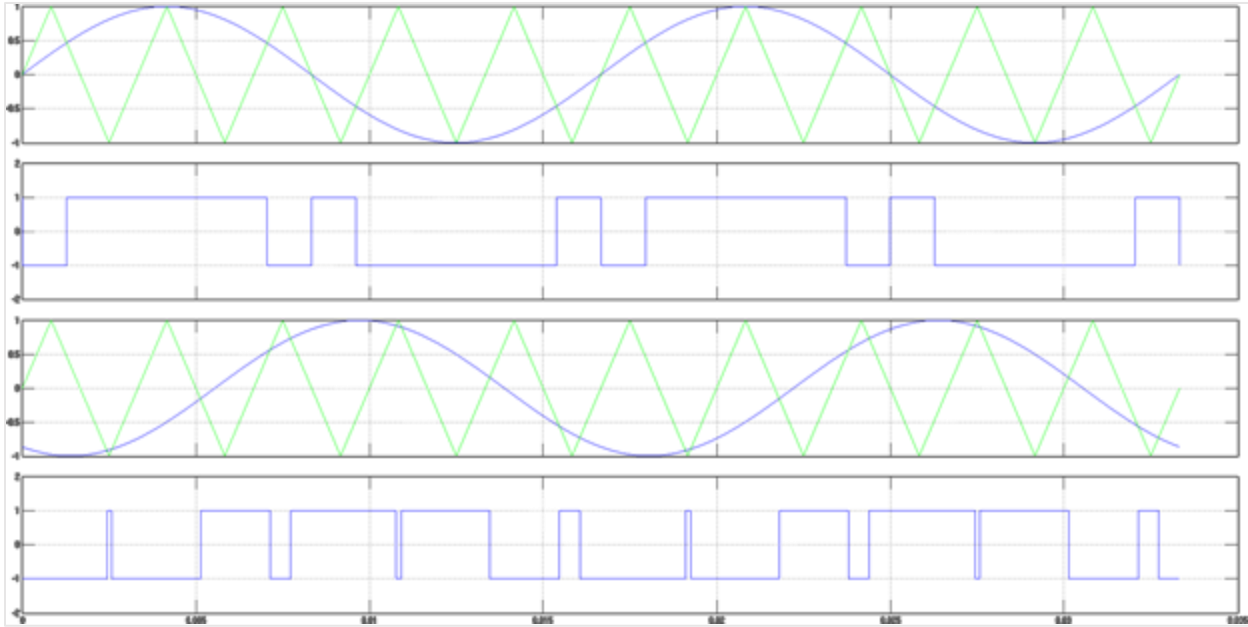


Figure 2. 38. SPWM at $cf=5$ and full modulation index

Figure 2.36., with $cf = 44$, is a case of carrier frequency selected as an even multiple of fundamental. Due to even selection of the carrier, all the sideband harmonics are evenly positioned throughout the phase waveform and phase to phase spectra, which is a highly undesirable outcome. In addition to even harmonics, carrier and odd triplen harmonics are also present in the waveform due to $cf = 44$ being a non triplen multiple of fundamental.

In order to illustrate this better, same SPWM modulation case will be used as previously with $cf = 4$ and shown in Figure 2.39. Since $cf = 4$ is a non triplen multiple, phase outputs between phases are not equal, as was the case in previous example. However, uniqueness is that output phase waveforms have lost half wave symmetry, thus producing even harmonics in the harmonic spectrum.

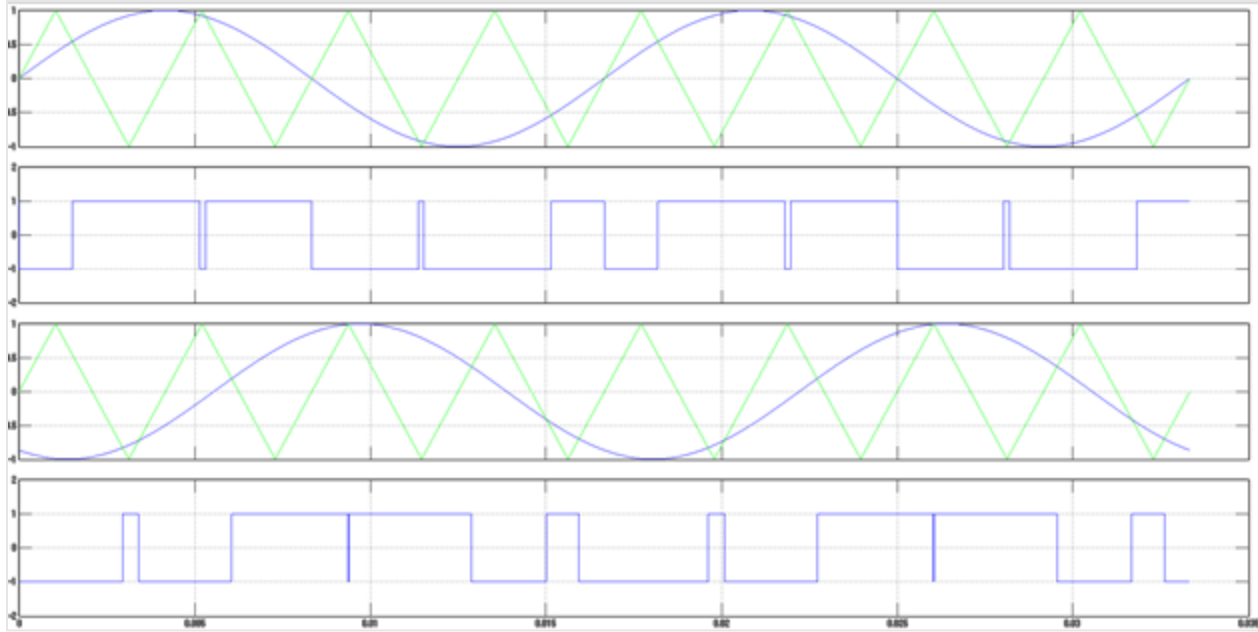


Figure 2. 39. SPWM at $cf=4$ and full modulation index

In figure 2.37., with $cf = 45$, carrier is selected as an odd triplen multiple of the fundamental, which achieves optimum low order harmonic cancelation. The frequency of the carrier harmonic and phase is identical in all phases, and hence cancels between phases. Also, triplen baseband and sideband harmonics that are product of a common mode voltage component in reference waveform cancel out completely between phases in a same fashion.

Also, odd triplen multiple carrier does not produce even harmonics in phase voltage and phase to phase voltage waveforms, thus making it a desirable choice of carrier to fundamental ratio in terms of low order harmonic performance.

For the harmonic analysis of the output voltage waveform, switching frequency does not influence the magnitude of the sideband harmonics in respect to carrier position, but it affects the frequency at which sideband harmonics occur. That has a direct impact on the magnitude of the current sideband harmonics because of attenuation thru the lowpass filter on the output of the inverter, which is highly dependent on frequency. However, in case where first 50 harmonics are

of primary interest, voltage harmonic values will decrease with higher carrier frequency values due to sideband harmonic roll off effect. Figure 2.40. shows a family of STHD50 curves in respect to modulation index m for DPWM1 at various carrier to fundamental frequency ratios. All the curves have proportional STHD50 across full range of modulation indexes, except in case of $cf = 45$. The reason for that exception is that major harmonics in first sideband set (41st, 43rd, 47th and 49th) are all included in STHD50 calculation, thus making its value very high.

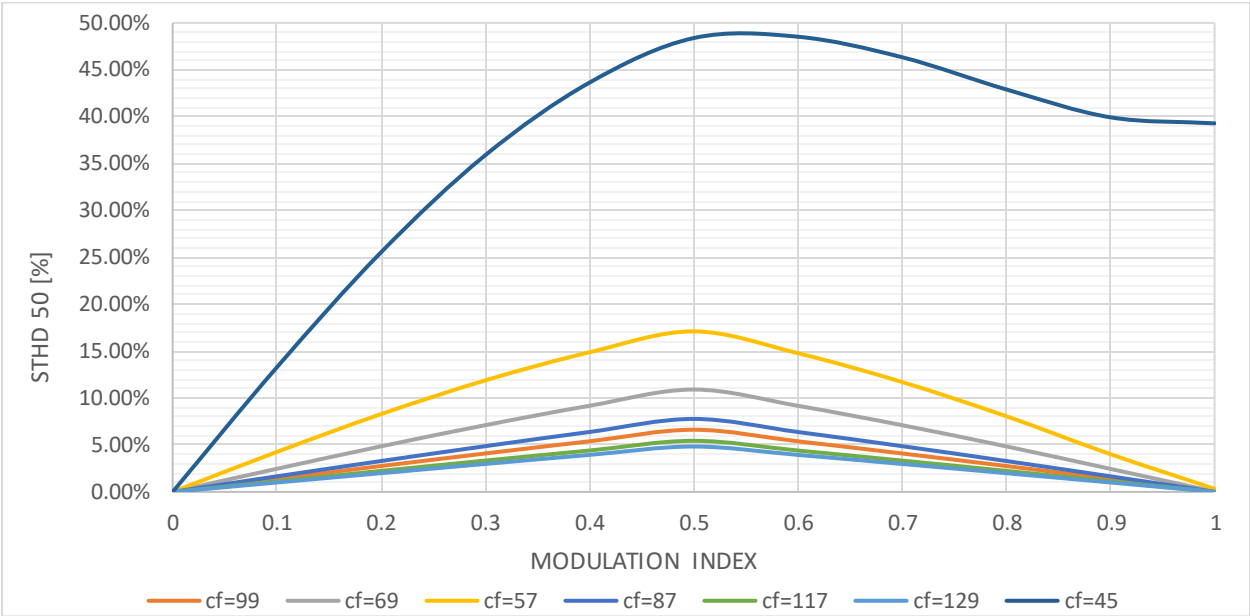


Figure 2. 40. STHD50 for DPWM1 at various at various cf and m values

In a similar fashion, but with the exclusion of $cf = 45$ case, Figure 2.41. shows a family of STHD50 curves in respect to modulation index m for DPWM0 and DPWM2 at various cf ratios. All the curves demonstrate proportional STHD50 across full range of modulation indexes. Results from Figures 2.40. and 2.41. clearly show that the value of first 50 voltage harmonics that DPWM strategies produce is highly dependent on the carrier frequency selection, and it decreases with carrier frequency rise.

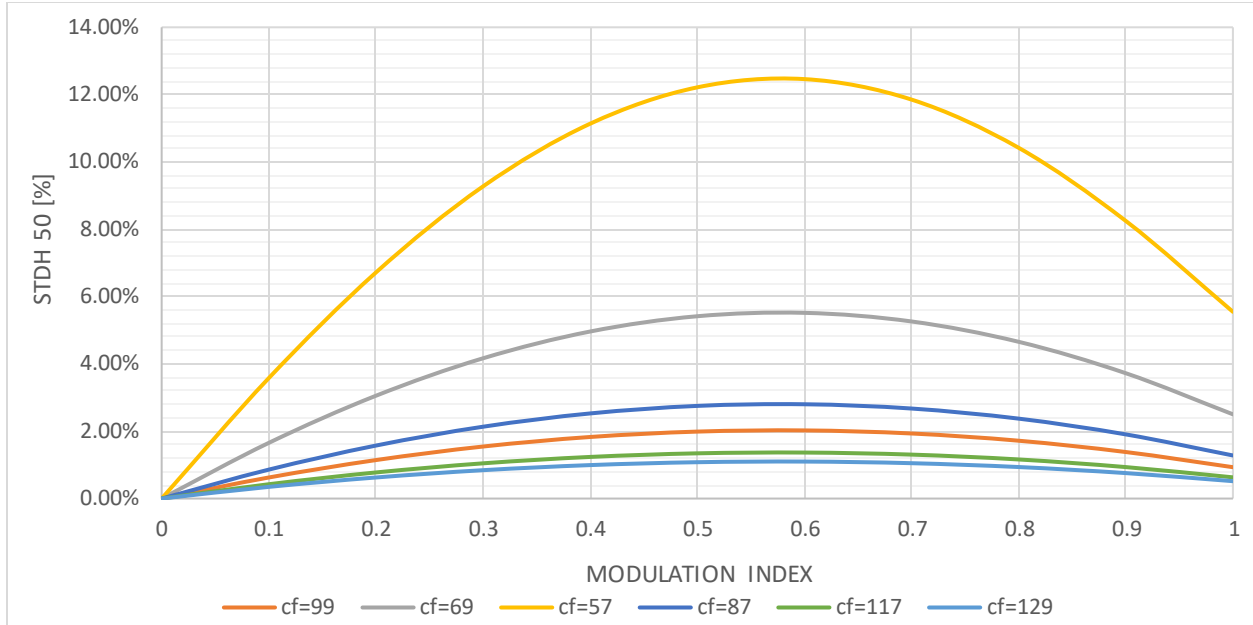


Figure 2. 41. STHD50 for DPWM0 and DPWM2 at various at various cf and m values

In order to quantify a decrease in STHD50 value with respect to carrier increase, a carrier frequency factor k_{cf} is introduced. If $cf = 57$ is considered a reference value for STHD50 across full range of m values, k_{cf} is defined as:

$$k_{cf}(\%) = \frac{STHD50(cf > 57, 0 < m < 1)}{STHD50(cf = 57, 0 < m < 1)} 100 \quad (2.43.)$$

Value of $cf = 57$ is used as a reference value because it is the smallest carrier value that is odd triplen multiple of fundamental frequency that does not include $fc-2$ and $fc-4$ sideband harmonics in STHD50 calculation.

Figure 2.42. shows k_{cf} value for DPWM0/1/2/3 for various cf values. k_{cf} has a rapid decline in value with carrier frequency increase, with DPWM1 and DPWM3 having a slower rate of decline. From the standpoint of low frequency harmonic performance of a DPWM based modulator, based on this analysis, it is desirable to always select the highest carrier frequency possible, which will typically be limited by the power rating of the semiconductor switches used.

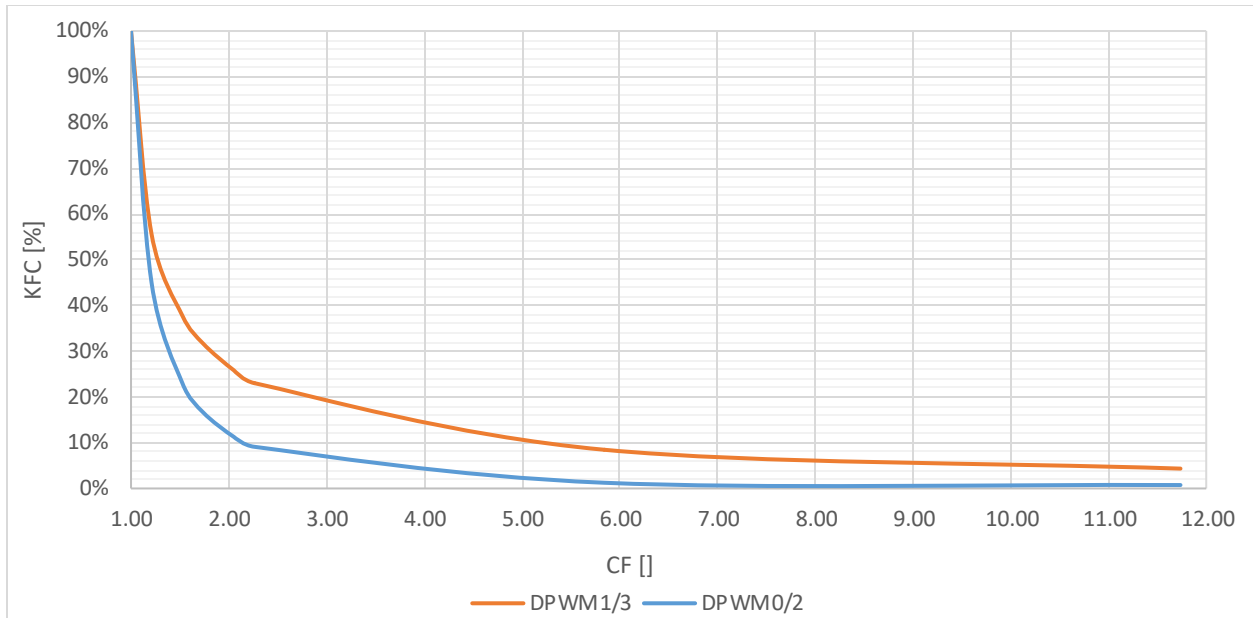


Figure 2. 42. k_{cf} for DPWM0/2 and DPWM1/3 at various cf

Also, it is important to note that with increase in cf decline of k_{cf} value is more rapid than attenuation decline of higher order output low pass filter, as further described in Chapter 3.1. This implies that in applications with high switching frequency, DDPWM modulator has negligible impact on $STHD_{50}$ value and has comparable low order harmonic performance to CPWM modulators.

When modulators using fixed frequency PWM are considered, the possibility of using two basic alternatives for determining the converter switch ON times exist:

1. Naturally Sampled PWM - Switching at the intersection of a reference signal waveform and high frequency carrier
2. Regular Sampled PWM - Switching at the intersection of a regularly sampled reference signal waveform and high-frequency carrier

All the harmonic analysis performed so far has considered naturally sampled PWM. However, naturally sampled PWM is very difficult for implementation in a digital modulation system, because the intersection between the reference and carrier is defined by a transcendental

equation which is complex to calculate. Therefore, regular sampled PWM is a modulation of choice for implementation in MTI. Detailed explanation of both natural and regular (symmetric and asymmetric) sampled PWM is covered in Chapter 4.1.

When comparing regular sampled to naturally sampled PWM, regular sampling creates low-order baseband harmonics just above the fundamental component, but it also attenuates the lower side sideband harmonics and increases the high-side sideband harmonics around the carrier frequency [28]. Figure 2.43. shows a harmonic spectrum comparison for DPWM1 at $cf = 69$ and $m = 0.6$ for natural, symmetrical (peak) and asymmetrical (peak and valley) sampling cases.

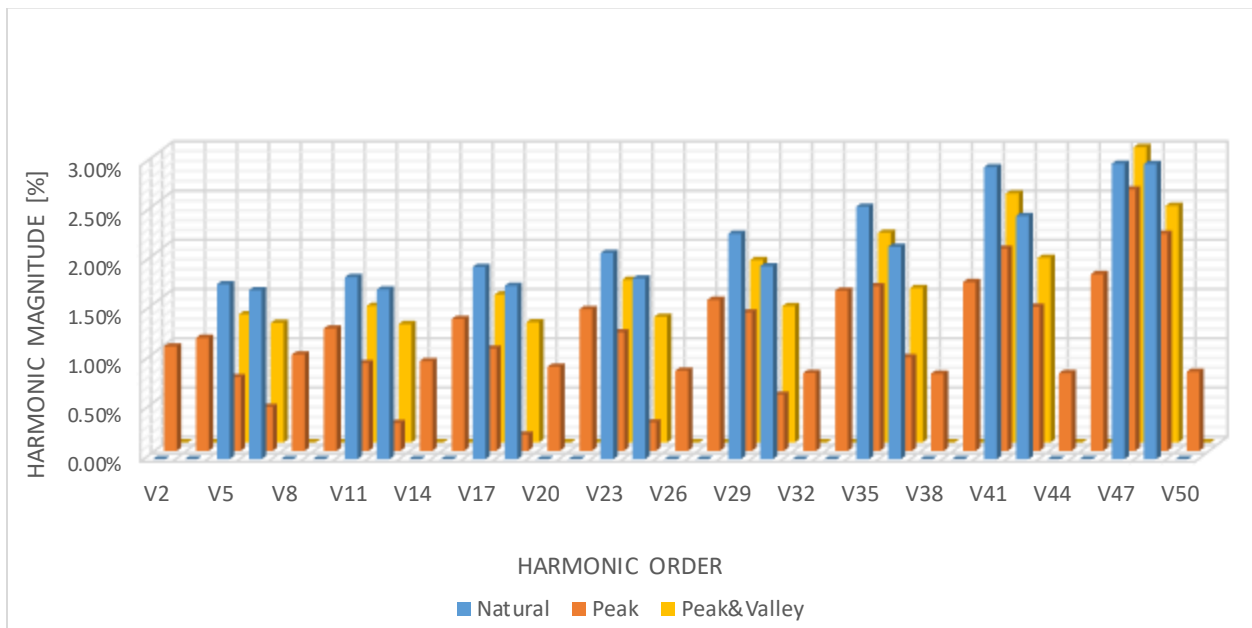


Figure 2. 43. DPWM1 – Harmonic spectra for natural, peak and peak & valley sampling

Results in Figure 2.43. confirm that lower sideband harmonics within first 50 harmonics are reduced in case of regular sampling as compared to natural sampling due to the low sideband skew identified in [28]. Also, another more important conclusion is that there is a major difference between symmetrical and asymmetrical regular sampling methods where symmetrical regular sampled PWM introduces additional sideband harmonic components which asymmetrical PWM

algorithm does not create. Some of those sideband harmonics are even positioned, causing MTI applications with low cf values hard to meet even harmonic distortion limits when symmetrical regular sampled PWM is used.

2.5.3.Low Order Harmonics – Other Effects

Previous literature mostly concentrates on developing compensation methods for phenomena affecting low order harmonics in a switching model. In most cases, the compensation techniques are based on an average value theory, where lost volt-seconds are averaged over an entire cycle and added to the commanded voltage [29]-[35]. An important issue that is seen in these compensation techniques is that they are all based on the polarity of the current. Another phenomenon that was considered is the minimum pulse-width constraint [36]-[38], which was first observed in slow switching devices like thyristors [39].

2.5.3.1. Dead Time and Non-Linearities due to Turn On/Off and Voltage Drop on Switching Devices

Dead time is a necessary blanking time introduced to avoid simultaneous conduction of both switches of the same inverter phase called a shoot-through [40] - [43]. Although individually small, when accumulated over a fundamental cycle, the voltage errors are sufficient to distort the applied PWM signal by affecting both the magnitude and phase error of the fundamental output voltage waveform [44] - [50]. Also, switching times of the semiconductor device used induce the same type of effect, in terms of introducing error to the output voltage [51]. Figure 2.44. illustrates dead time and switching time effects for single IGBT leg.

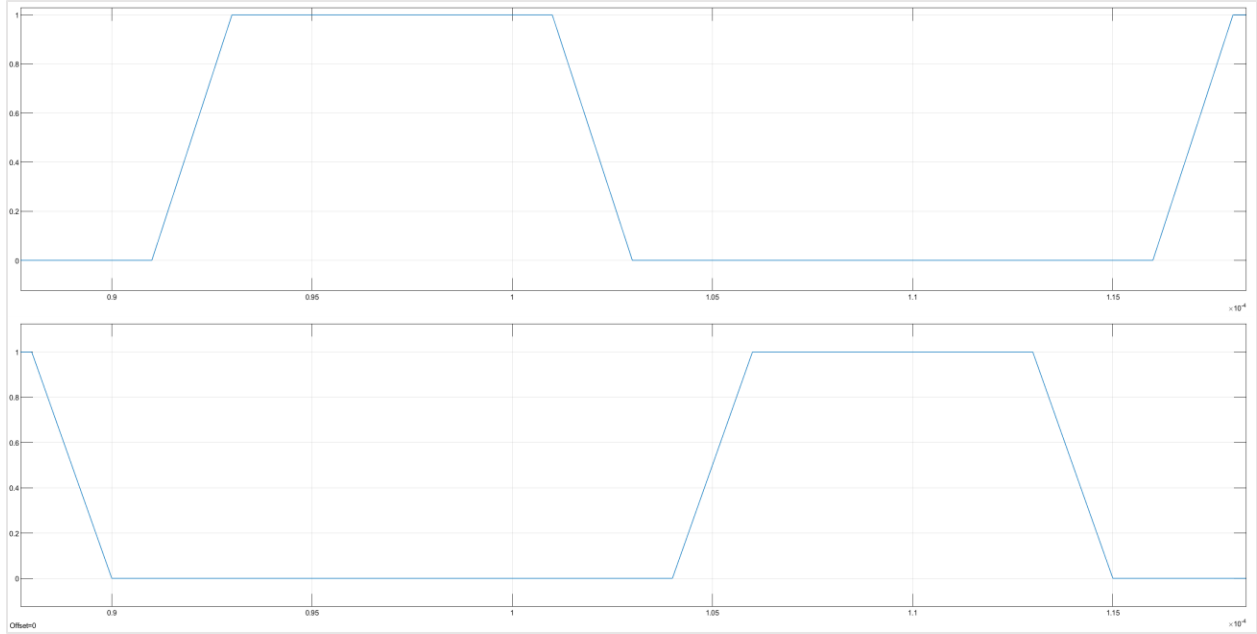


Figure 2. 44. Dead time and switching time effects in single IGBT leg

The average output duty cycle error d_{err} during one switching cycle T_s , resulting from dead time T_d and device switching times T_{on} and T_{off} is given by:

$$d_{error} = \left[\frac{\left(-\frac{T_{off}}{2} + \frac{T_{on}}{2} + T_d \right)}{T_s} \right] \text{sign}(I) \quad (2.44.)$$

Where $\text{sign}(I)$ represent polarity of the output load current.

As opposed to CPWM strategies, where duty cycle error is introduced throughout the full fundamental cycle, DPWM strategies introduce it during switching period equaling two thirds of the fundamental cycle, thus introducing smaller error when averaged over the fundamental cycle. Regardless of modulation strategy, for current controlled inverters, duty cycle errors resulting in fundamental voltage harmonic value changes get compensated thru the gain of the current regulator. However, this duty cycle error also introduces additional harmonic components that need to be quantified. Figure 2.45. shows a voltage error waveform due to introduction of 4.5 us dead time in case of DDPWM at $\theta = 90^\circ$, $m = 1$ and $cf = 69$. Figure 2.46. shows an enlarged

waveform, in which it becomes obvious that usage of average voltage error d_{err} has very little meaning for harmonic impact. The reason is that the actual voltage error waveform consists of train of very narrow pulses that have the amplitude equal to DC bus voltage value $\pm V_{dc}$, depending on the sign of the current waveform. This type of a waveform, despite low average value, has a very “rich” harmonic spectrum, thus significantly impacting overall harmonic performance of the modulator.

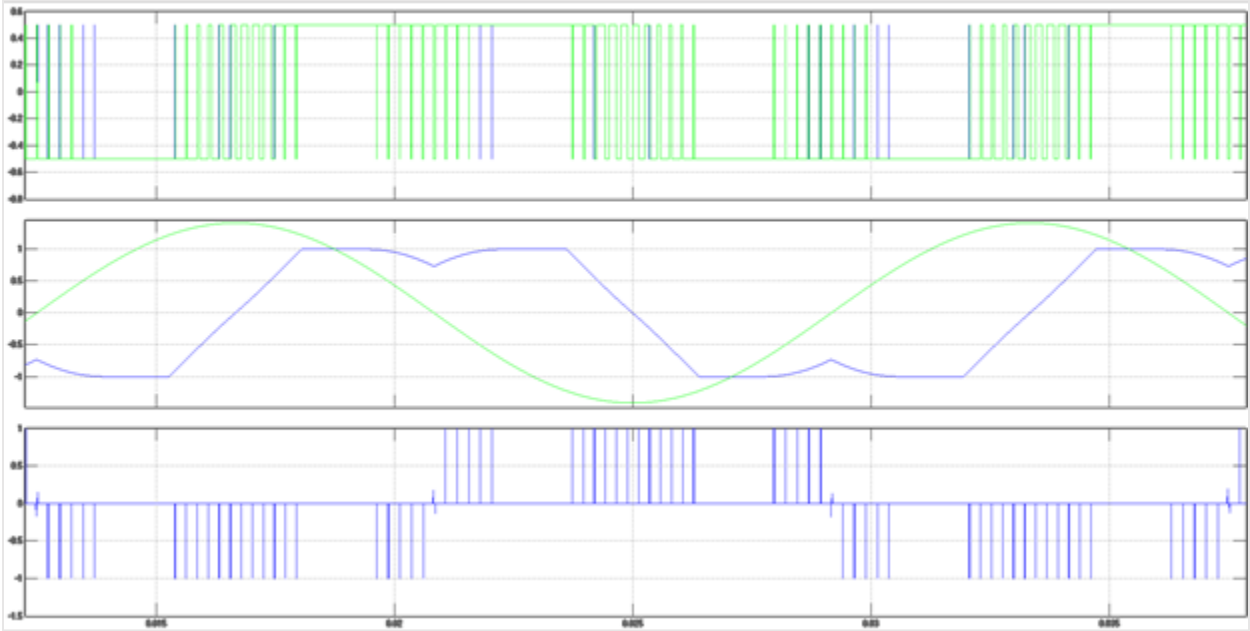


Figure 2. 45. DDPWM at $\theta = 90^\circ$ with $T_d=4.5\mu s$ a) Ideal and actual waveform b) Phase voltage and current c) Output Voltage Error

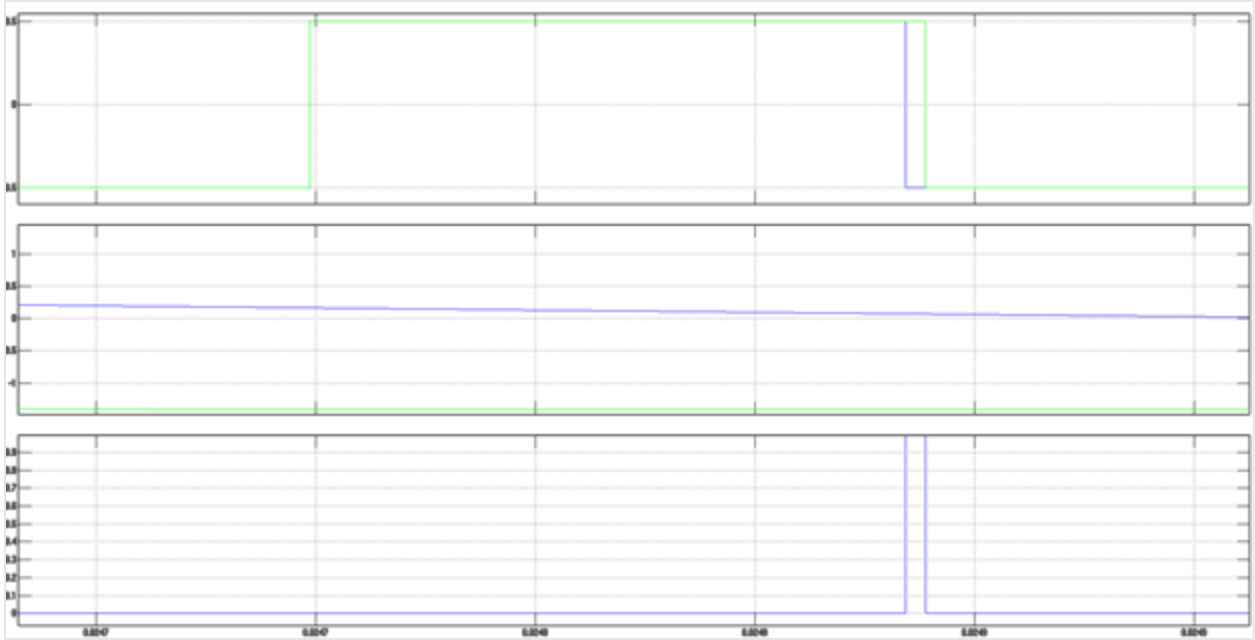


Figure 2. 46. DDPWM at $\theta = 90^\circ$ with $T_d=4.5\mu s$, Enlarged Waveform a) Ideal and actual waveform b) Phase voltage and current c) Output Voltage Error

Due to a highly nonlinear nature of DPWM strategies, harmonic analysis will be performed based on the simulation model. DPWM strategies have been analyzed for varying angle differences between output voltage and current in each phase. Each modulation is used with phase angle corresponding to the minimum switching losses. For instance, Figure 2.47. and Figure 2.48. represent incremental harmonic difference for DDPWM modulation with phase angle difference of -90° and 0° respectively, at $cf = 69$ and $0 < m < 1$ for $T_d + \frac{T_{on}}{2} - \frac{T_{off}}{2} = T_{dt} = 3\mu s$.

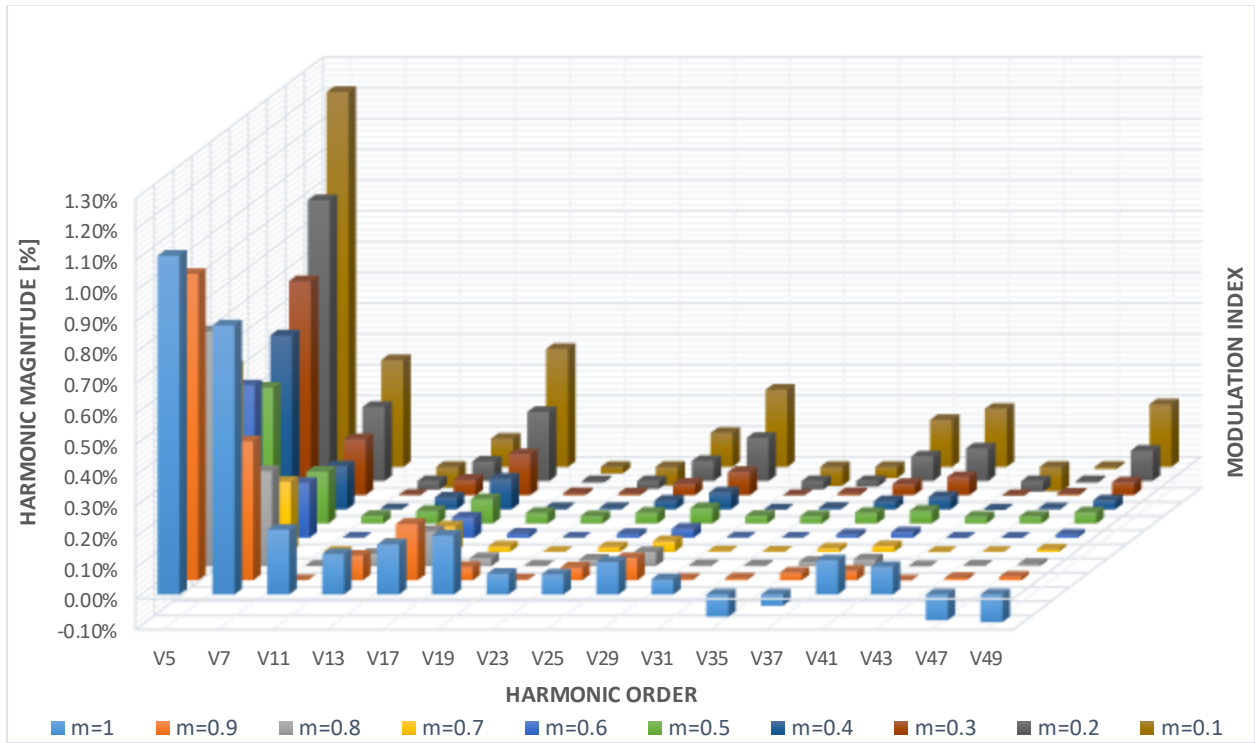


Figure 2. 47. Incremental Low Order Harmonic Spectra for DDPWM with $T_{dt}=3\mu s$ at $\theta = -90^\circ$

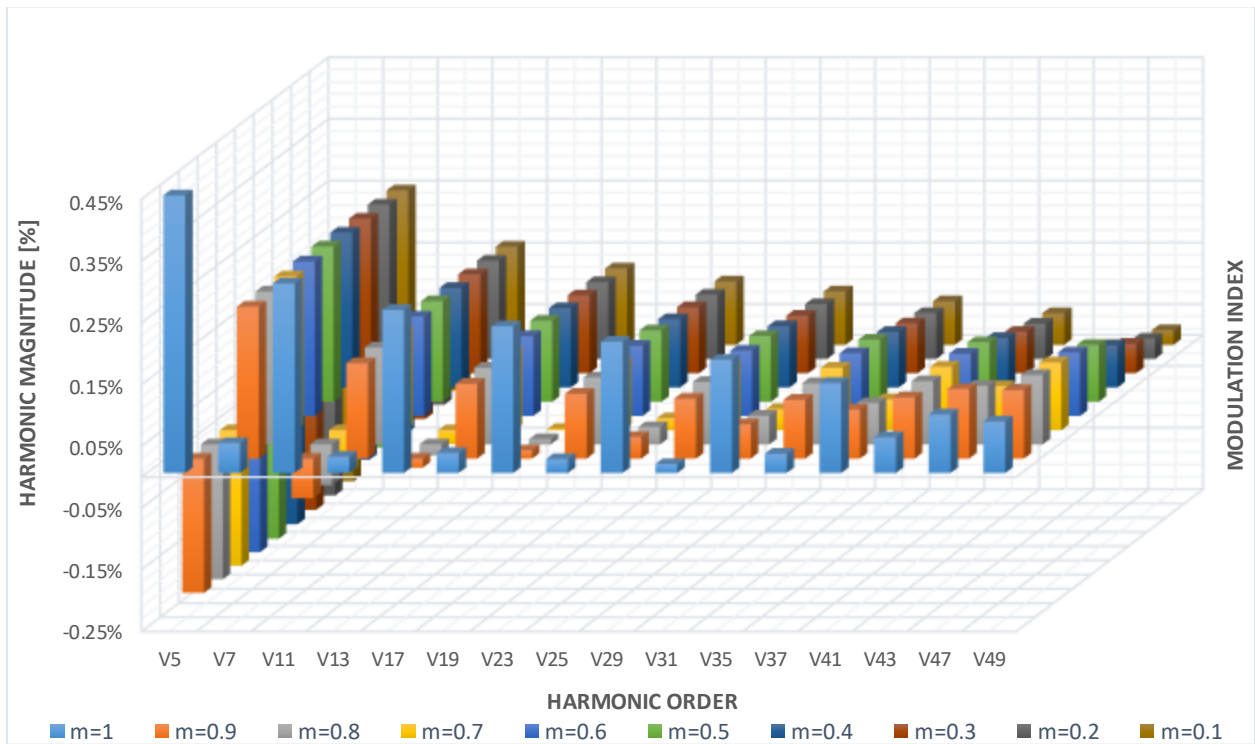


Figure 2. 48. Incremental Low Order Harmonic Spectra for DDPWM with $T_{dt}=3\mu s$ at $\theta = 0^\circ$

Despite a very similar harmonic performance between $\theta = -90^\circ$ and $\theta = 0^\circ$ cases covered in previous section, their incremental harmonic response to dead time and rise and fall times of the switches is very different. Except for $m = 1$ case, $\theta = 0^\circ$ introduces very weak dependency on the modulation index value, and slow roll off. On the other hand, $\theta = -90^\circ$ introduces stronger dependency on the modulation index value and faster roll off.

One other important thing to consider is that error introduced due to dead time and rise and fall times of the switches is based on the polarity of the current. Therefore, same modulation technique will respond differently based on the polarity of the current. Figures 2.49. and 2.50. show incremental harmonic performance for DDPWM with phase angle difference of -60° and 120° respectively, at $cf = 69$ and $0 < m < 1$ for $T_{dt} = 3\mu s$. Figure 2.49. shows stronger dependency of incremental harmonic values on the modulation index value, while Figure 2.50. shows higher incremental harmonic values overall.

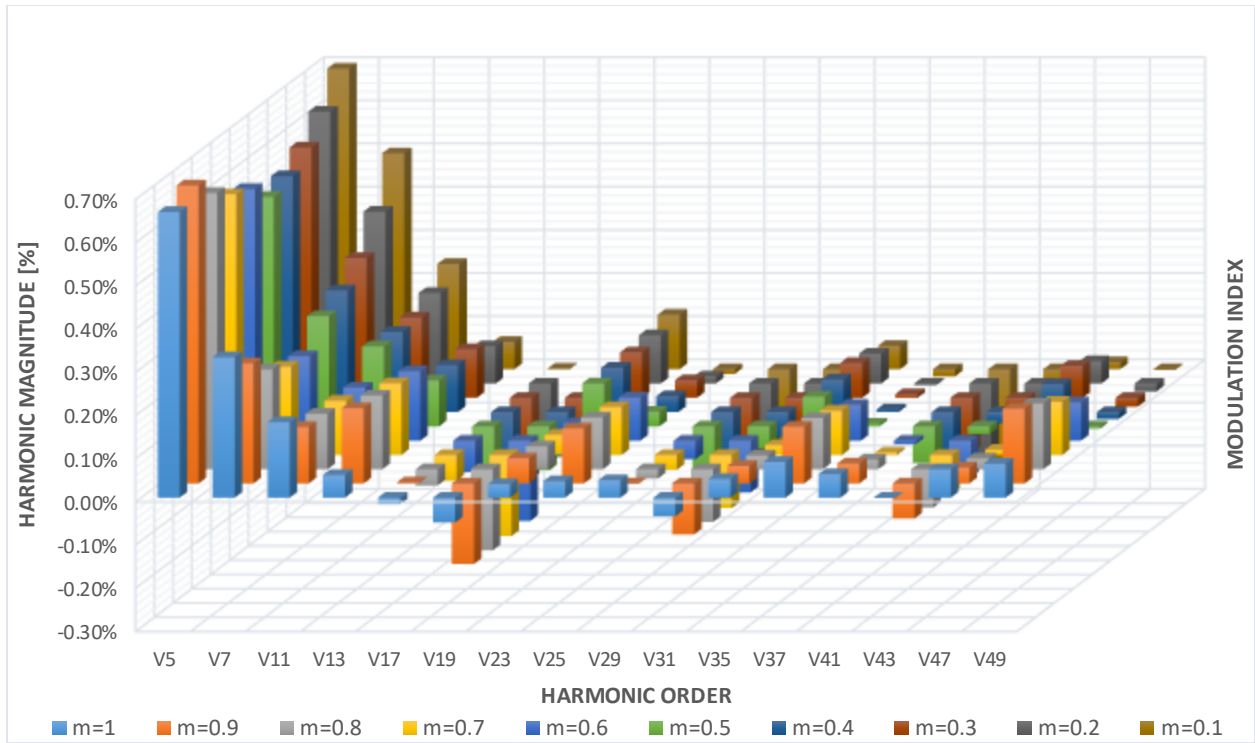


Figure 2. 49. Incremental Low Order Harmonic Spectra for DDPWM at $\theta = 60^\circ$ with $T_{dt} = 3\mu s$

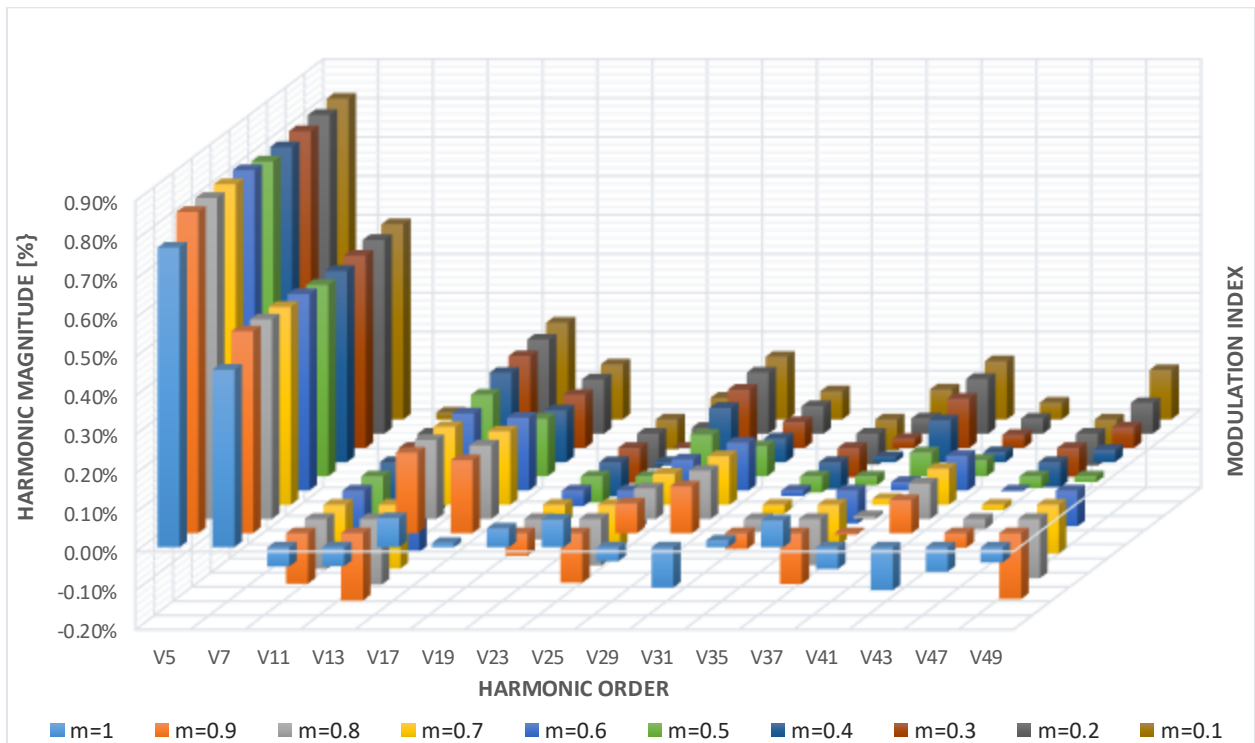


Figure 2. 50. Incremental Low Order Harmonic Spectra at $\theta = 120^\circ$ for DDPWM with $T_{dt} = 3\mu s$

Based on the incremental harmonic analysis performed on DDPWM strategy across full phase angle range, which due to a large scale cannot be fully presented in this work, one common conclusion can be derived. Introduction of Dead time and consideration of rise and fall times of switches have a dominant effect on the 5th and 7th harmonic incremental values. Also 5th and 7th harmonics have the smallest attenuation once passed thru the low pass filter, thus emphasizing more importance due to current harmonic performance of the inverter, which will be discussed later. Therefore, Figures 2.51. and 2.52. represent 5th and 7th harmonic incremental behavior for $0 < m < 1$ across phase angle difference range $-180^\circ < \theta < 180^\circ$ for $T_{dt} = 3\mu s$. It is noticeable that various DPWM techniques respond very differently to dead time and rise and fall time introduction in terms of 5th and 7th harmonic incremental values, with DPWM3 reaching the highest values overall.

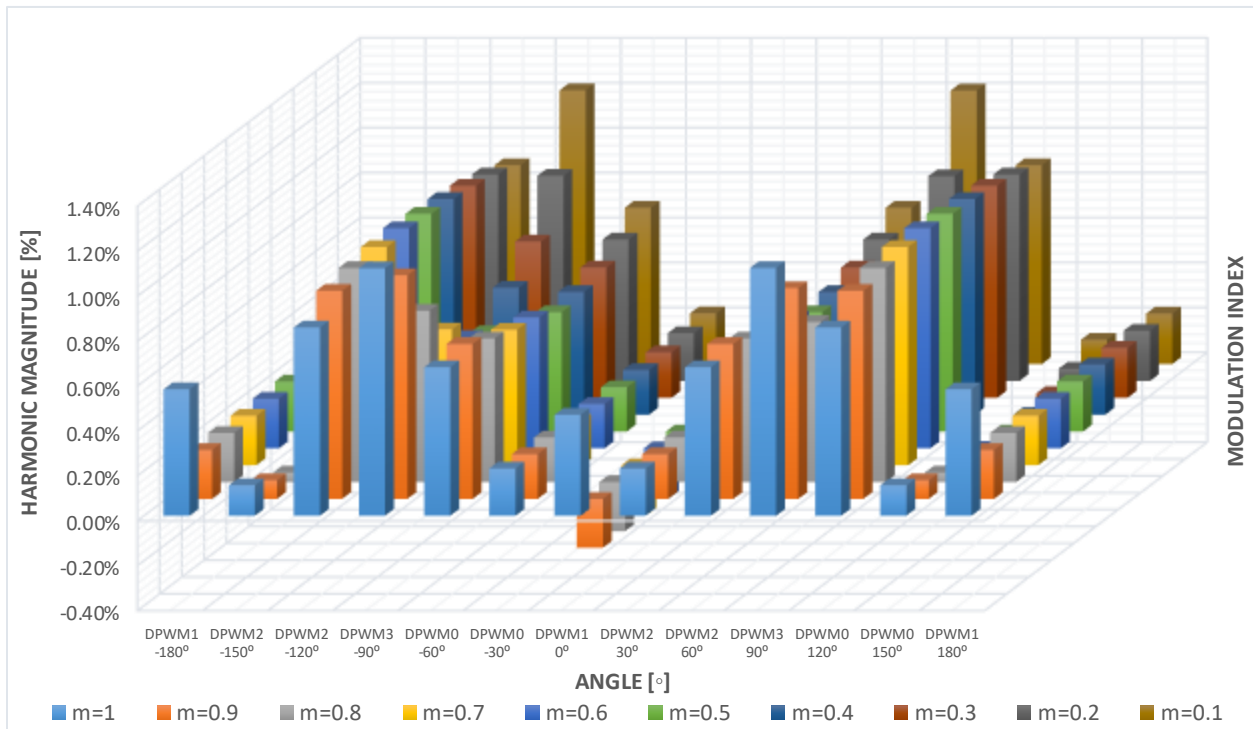


Figure 2. 51. 5th Harmonic Incremental value for $T_{dt}=3\mu s$

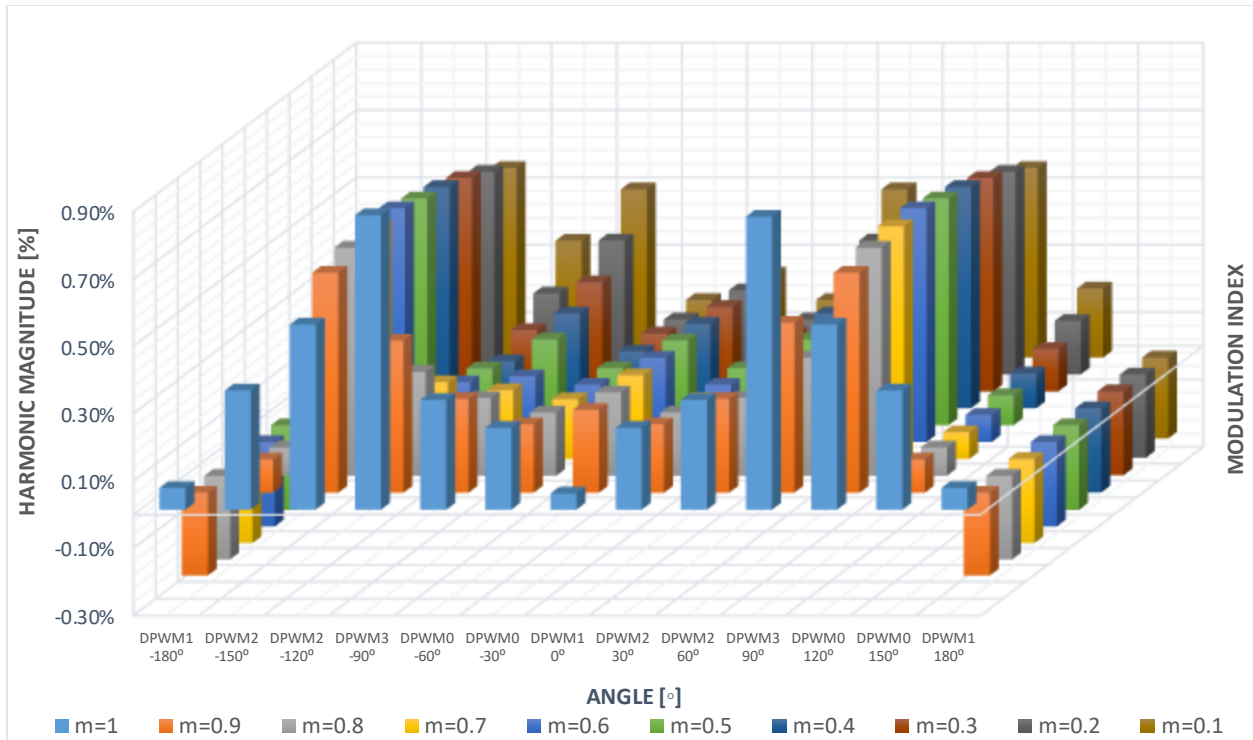


Figure 2. 52. 7th Harmonic Incremental value for $T_{dt}=3\mu s$

Carrier frequency has a direct linear relation to the output voltage error, since the delay occurs in every PWM cycle, thus leading to higher output voltage error with an increased carrier frequency values [44]. Figures 2.53. and 2.54. represents 5th and 7th harmonic incremental behavior for DDPWM at $\theta = -90^\circ$, $T_{dt} = 3\mu s$ for $69 < cf < 690$.

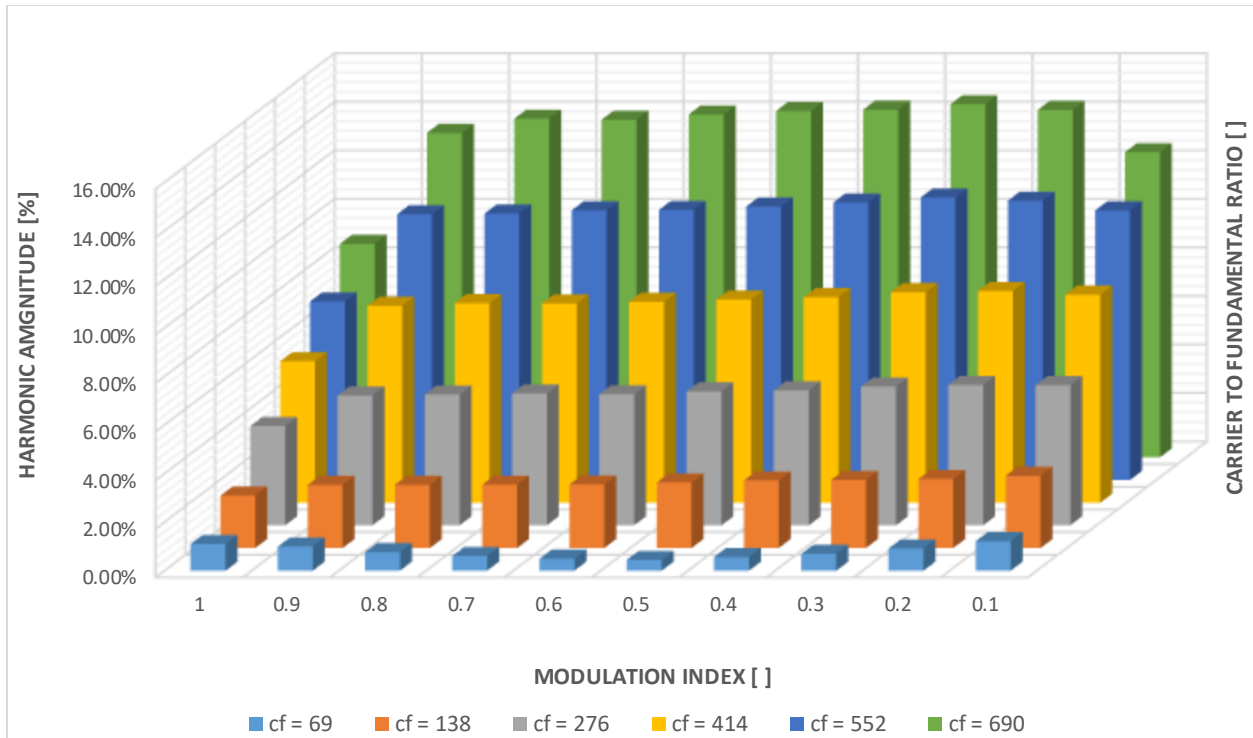


Figure 2. 53. 5th Harmonic Incremental value DDPWM at $\theta=-90^\circ$, $T_{dt}=3\mu s$ for $69 < cf < 690$

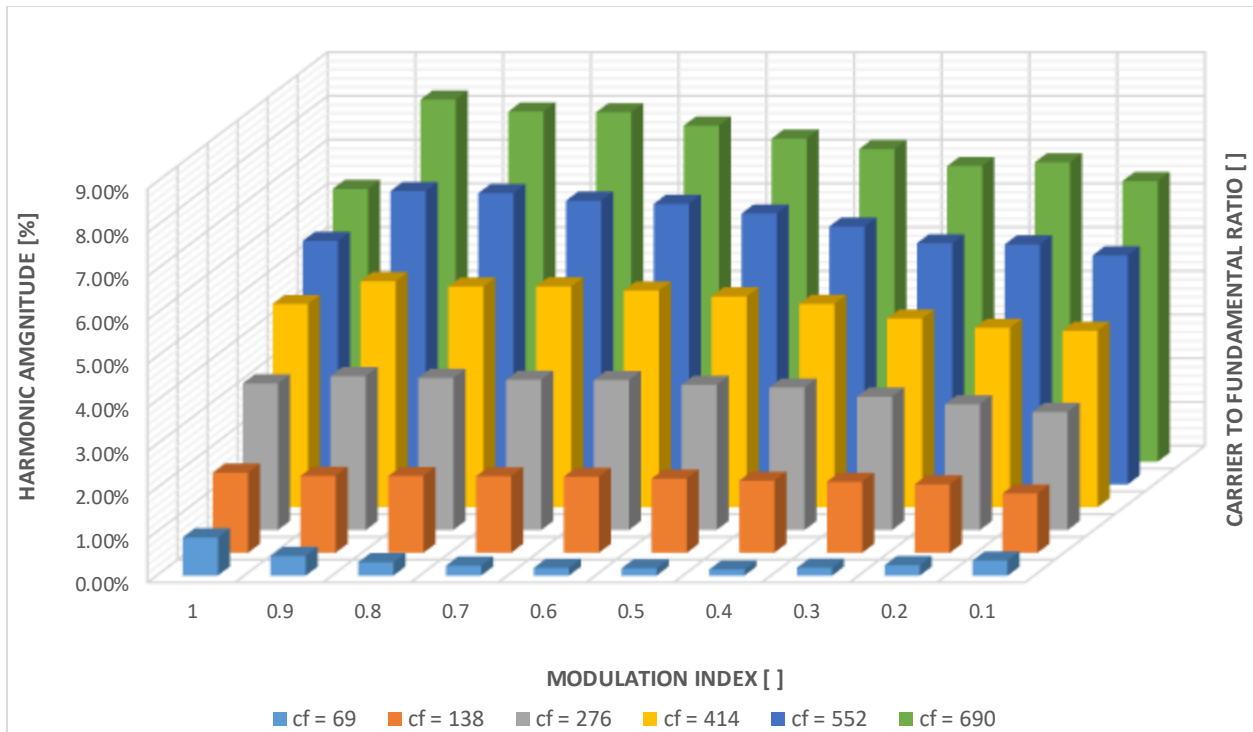


Figure 2. 54. 7th Harmonic Incremental value DDPWM at $\theta=-90^\circ$, $T_{dt}=3\mu s$ for $69 < cf < 690$

Despite a highly nonlinear nature of DDPWM modulator, further analysis of the average distortion of 5th and 7th harmonic values at different cf values shown in Figure 2.55. shows that harmonic performance has a characteristic that can be approximated as linear in relation to carrier frequency.

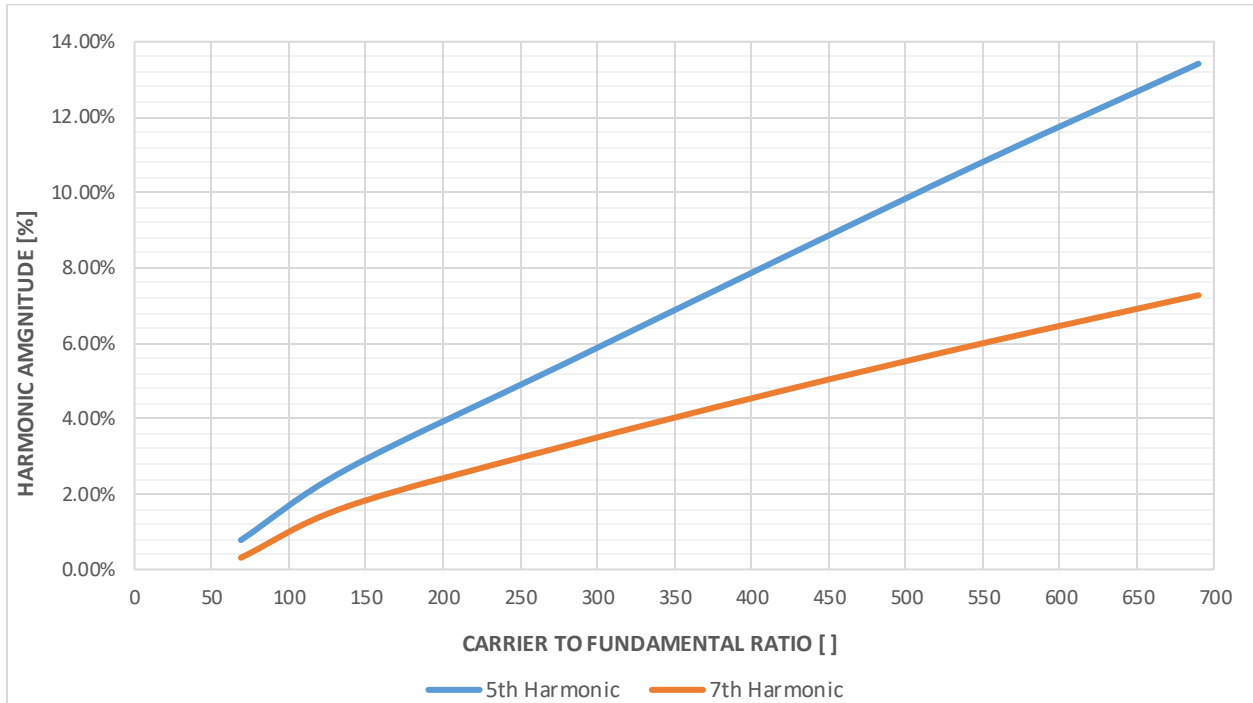


Figure 2. 55. 5th and 7th Average Harmonic Incremental value DDPWM at $\theta = -90^\circ$, for $69 < cf < 690$

Therefore, approximated incremental harmonic distortion of 5th and 7th harmonic ΔV , for cf values being selected as an odd triplen multiple of fundamental, becomes:

$$\Delta V_{5th,7th} (@ cf = f_c) = \Delta V_{5th,7th} (@ cf = f_b) \frac{f_c}{f_b} \quad (2.45.)$$

Where f_c and f_b represent given and base carrier frequencies.

Another parameter that has a linear relation to output voltage error value are the dead time and device switching times themselves. Figures 2.56. and 2.57. represents 5th and 7th harmonic incremental behavior for DDPWM at $\theta = -90^\circ$, $cf = 69$ for $3\mu s < T_{dt} < 12\mu s$.

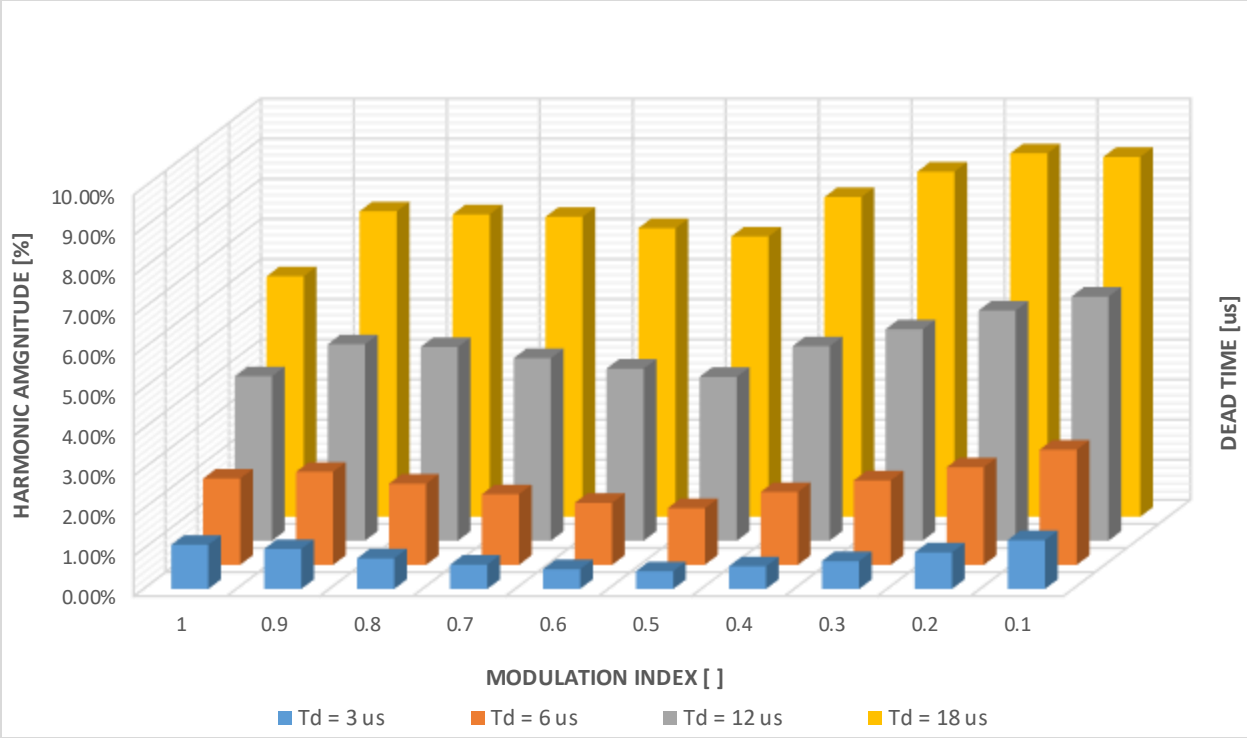


Figure 2. 56. 5th Harmonic Incremental value DDPWM at $\theta=-90^\circ$, for $3\mu s < T_{dt} < 12\mu s$

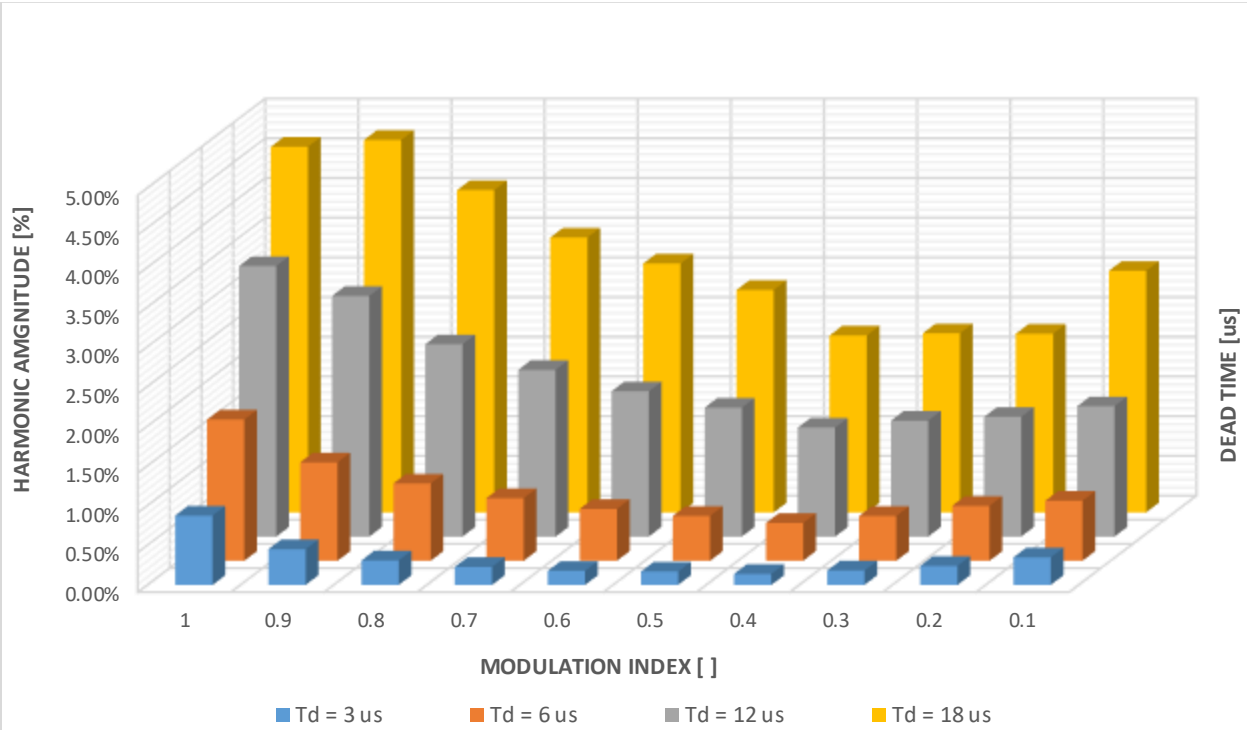


Figure 2. 57. 7th Harmonic Incremental value DDPWM at $\theta=-90^\circ$, for $3\mu s < T_{dt} < 12\mu s$

Similar to increased carrier frequency performance, further analysis of the average distortion of 5th and 7th harmonic values at different dead time values shown in Figure 2.58. shows that harmonic performance has a characteristic that can be approximated as linear in relation to dead time value.

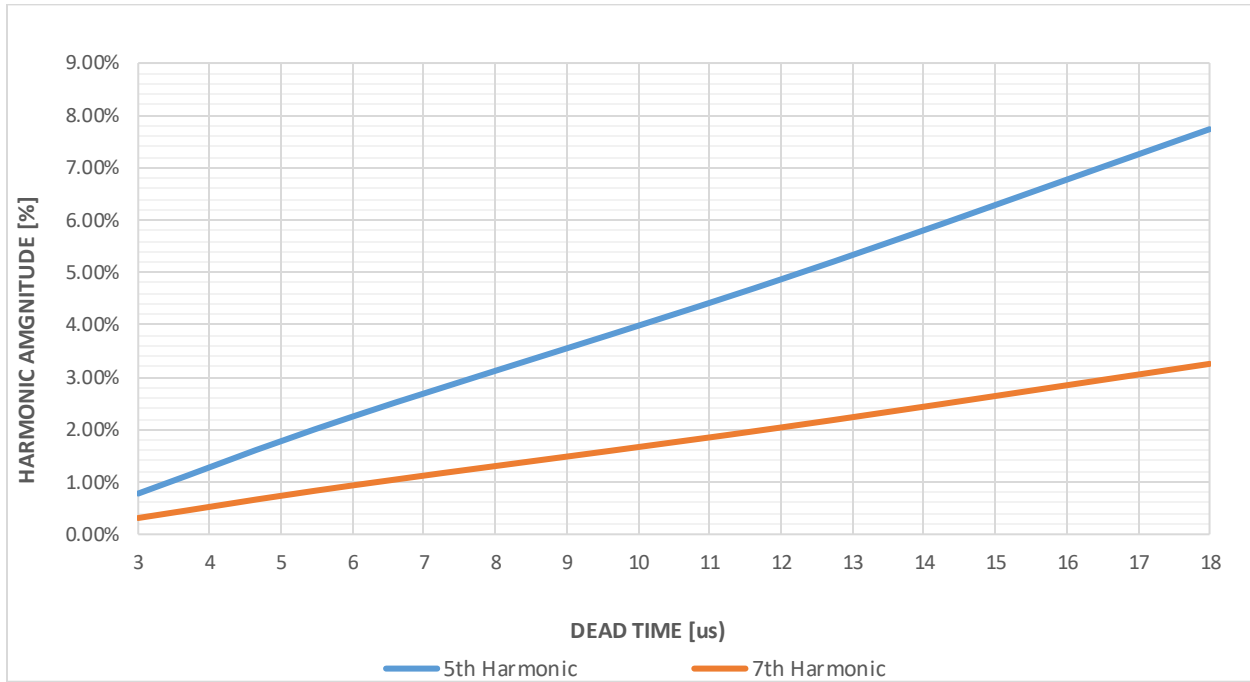


Figure 2. 58. 5th and 7th Average Harmonic Incremental value DDPWM at $\theta=-90^\circ$, for $3\mu s < T_{dt} < 12\mu s$

Higher dead time values lead to increased incremental harmonic distortion of 5th and 7th harmonic ΔV , which can be approximated as linear function:

$$\Delta V_{5th,7th} (@T_{dt} = \tau_c) = \Delta V_{5th,7th} (T_{dt} = \tau_b) \frac{\tau_c}{\tau_b} \quad (2.46.)$$

Where τ_c and τ_b represent given and base total dead time.

Except for dead time and device switching times, another cause of voltage distortion is due to forward voltage drop across switching devices as the voltage drops during the on-state [61].

Voltage drop across the switch V_{ce} and diode V_d causes some non-linearities of the output voltage, thus creating average output duty cycle error d_{err} during one switching cycle T_s defined by:

$$d_{error} = \left[d_{com} \left(\frac{V_{ce}}{V_{dc}} \right) + (1 - d_{com}) \left(\frac{V_d}{V_{dc}} \right) \right] \text{sign}(I) \quad (2.47.)$$

Where $\text{sign}(I)$, d_{com} and V_{dc} represent polarity of the output load current, commanded phase duty cycle and dc bus voltage.

Figure 2.59. shows a voltage error waveform due to introduction of $\frac{V_{ce}}{V_{dc}}$ and $\frac{V_d}{V_{dc}}$ of 1.242% in case of DDPWM at $\theta = 90^\circ$, $m = 1$ and $cf = 69$. Voltage error waveform in case of equal voltage drop across devices is a square wave function at fundamental frequency and magnitude equal to voltage drop. In order to evaluate the effect of asymmetrical drop across devices, Figure 2.60. represents a case where $\frac{V_{ce}}{V_{dc}}$ is eliminated, thus leaving only $\frac{V_d}{V_{dc}} = 1.242\%$.

Asymmetrical voltage drop case basically constitutes of a signed modulated duty cycle signal.

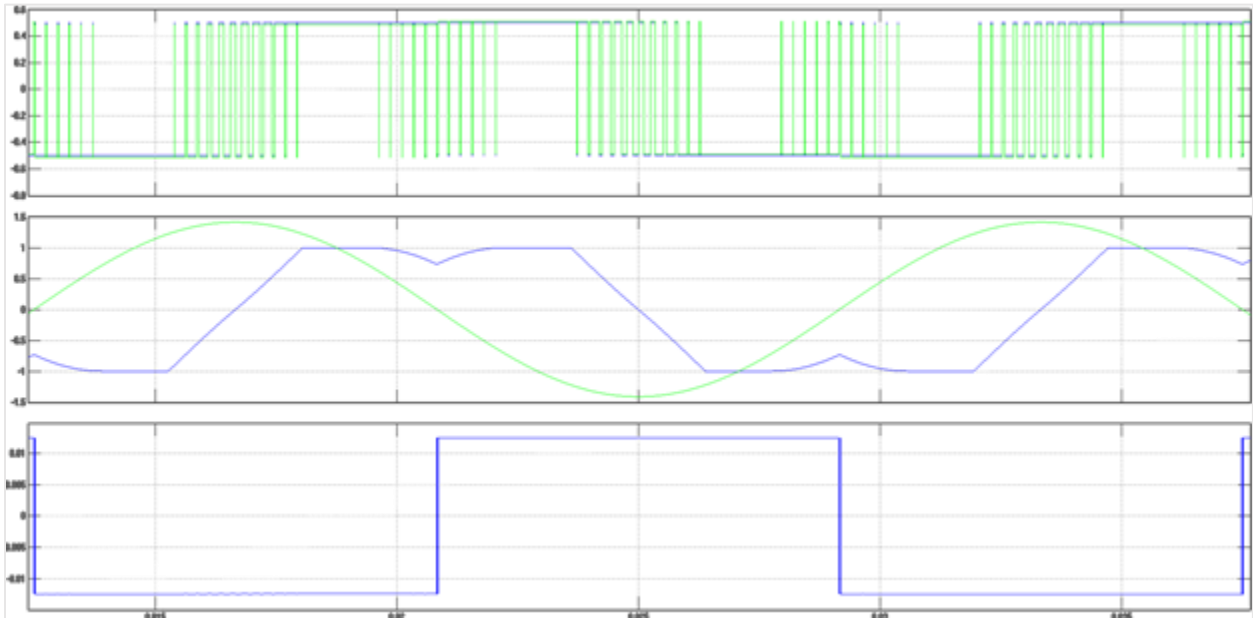


Figure 2. 59. DDPWM at $\theta=90^\circ$, with $V_{ce}/V_{dc}, V_f/V_{dc}=1.242\%$ a) Ideal and actual waveform b) Phase voltage and current c) Output Voltage Error

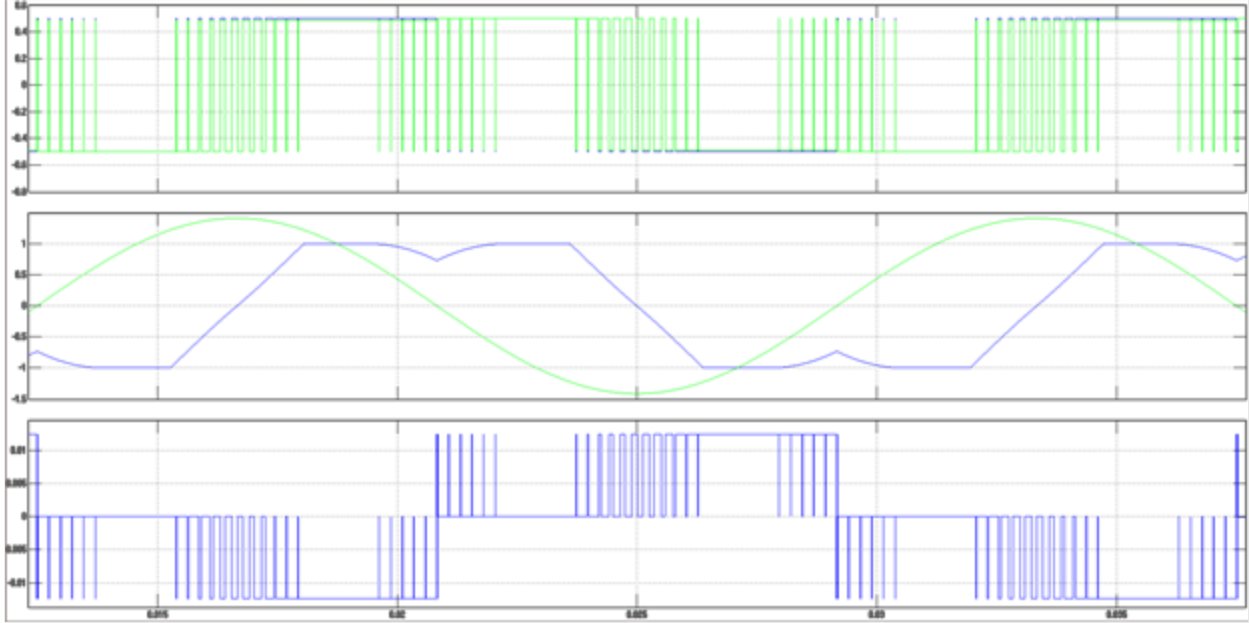


Figure 2. 60. DDPWM at $\theta=90^\circ$ with $V_{ce}/V_{dc}, =1.242\%, V_f/V_{dc} = 0\%$ a) Ideal and actual waveform b) Phase voltage and current c) Output Voltage Error

So far in this analysis, voltage drop across semiconductor switches has been considered as constant. However, that is never the case in practice, since voltage drop always has a resistive component that depends on current values. Therefore, it is useful to consider a purely resistive voltage drop case, which is shown in Figure 2.61. for $R_{ce} = 1.242\% \frac{V_{dc}}{I_{nom}}$ and $R_f = 1.242\% \frac{V_{dc}}{I_{nom}}$. Since voltage drop is proportional to current value in this case, output voltage error signal becomes purely sinusoidal, thus no additional harmonics are created.

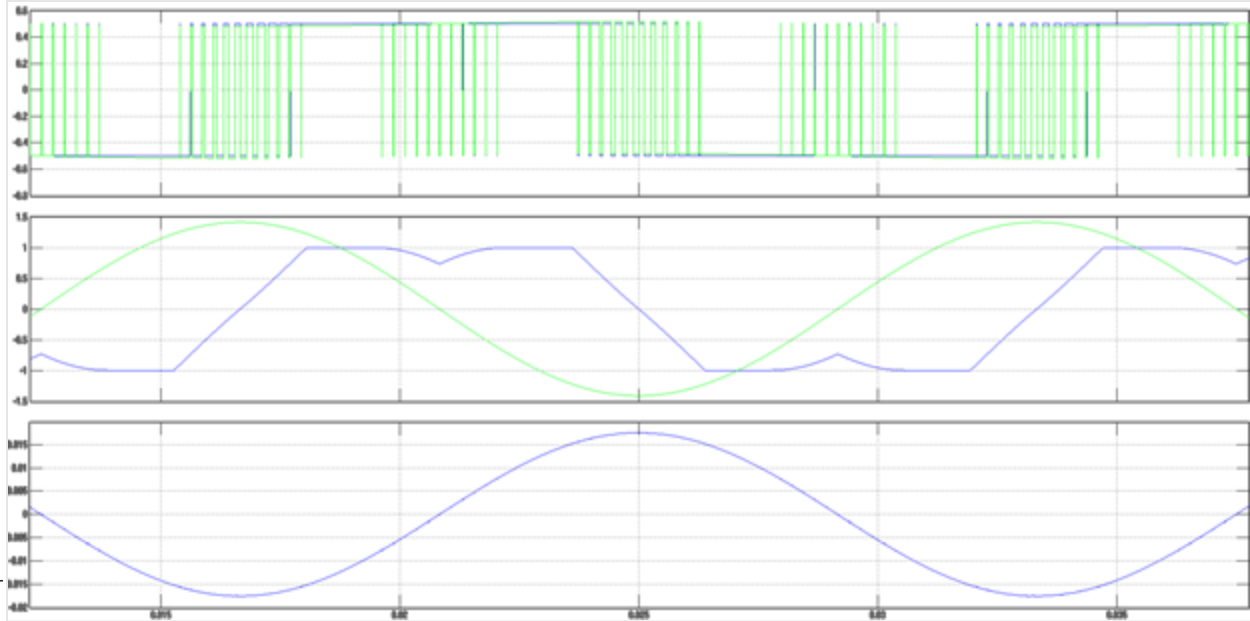


Figure 2. 61. DDPWM at $\theta=90^\circ$ with $R_{ce}, R_f=1.242\%$, V_{dc}/I_{nom} a) Ideal and actual waveform b) Phase voltage and current c) Output Voltage Error

As opposed to dead time introduction case in Figure 2.46, where voltage error consists of train of very narrow pulses that have the amplitude equal to DC bus voltage value, Figures 2.59, 2.60. and 2.61. exhibit lower magnitudes, thus creating lower harmonic values. Comparative harmonic spectrum for waveforms in Figures 2.47., 2.59., 2.60. and 2.61. is presented in Figure 2.62. Parameter values in all cases were selected such that they create the same average voltage error of the output waveform. As previously described, dead time effect has the highest harmonic impact, especially with 5th and 7th harmonic, which are the most pronounced harmonics. It is also important to notice a presence of triplen harmonics in phase voltage error waveform in cases a), b) and c), but those do not contribute in phase to phase voltage waveforms since they cancel out. Waveform in case d) is purely sinusoidal, thus creating only 1st order harmonic.

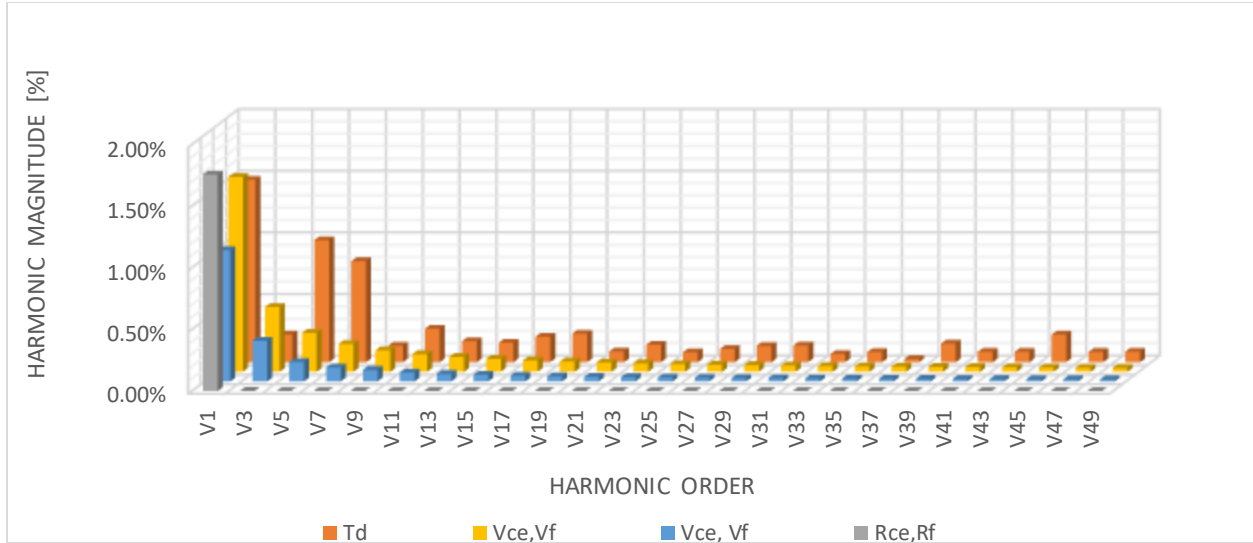


Figure 2. 62. Low Order Harmonic Spectra comparison for Voltage Error signal for a) $T_d=4.5\mu s$ b) $V_{ce}/V_{dc}, V_f/V_{dc}=1.242\%$ c) $V_{ce}/V_{dc}=1.242\%, V_f/V_{dc}=0\%$ d) $R_{ce}, R_f=1.242\% V_{dc}/I_{nom}$

Voltage drop of 1.242% is very high and not realistic for high power semiconductor switches, which are typically in a 0.2-0.4% range. Due to low voltage drop values and the fact that voltage drop introduces inherently lower values of added harmonics to output voltage waveform, voltage drop effect will not be further characterized for various PWM techniques used in MTI, and will only be used as part of the simulated switching model.

Last significant source of output voltage distortion that will be considered here is the minimum pulse-width (MPW) limitation that is introduced due to inability of lower switches to achieve small on time durations. As a consequence, maximum pulse width condition is imposed to the upper switches. MPW limitation is necessary in order to prevent possible damage to semiconductor switches as well as to address gate driver circuit constraints [36]. MPW limitation introduces minimum and maximum limits on to the phase duty cycle as per formula below:

$$d_{min} = \frac{(T_{mpw} + T_d)}{T_s} \quad (2.48.)$$

$$d_{max} = \frac{(T_s - T_{mpw} - T_d)}{T_s} \quad (2.49.)$$

Multiple solutions exist in the literature on how to implement MPW. The least invasive solution from controls standpoint is the one that reproduces the average value of the volt-seconds over a switching period. This can be easily implemented by either holding the MPW value or dropping the pulses completely depending on the desired duty cycle value. Comparison of ideal and MPW limited duty cycle is shown in Figure 2.63. MPW limitation also distorts phase to phase reference waveform, which can be seen in Figure 2.64.

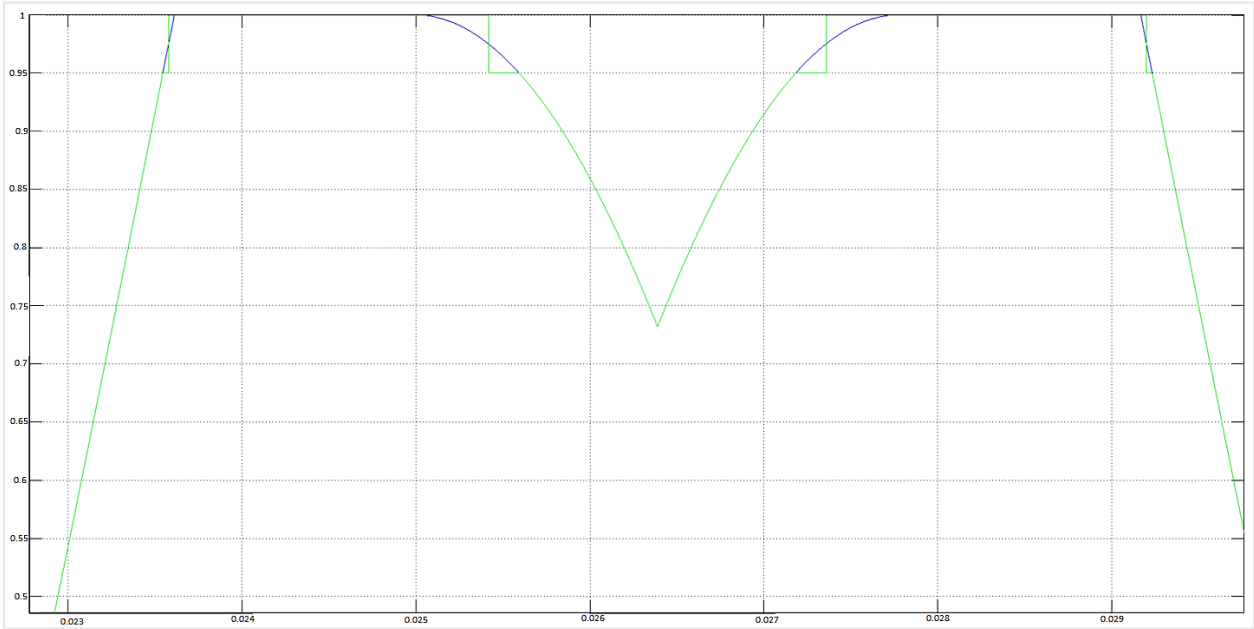


Figure 2. 63. DDPWM at $\theta=90^\circ$ – Ideal vs MPW limited duty cycle

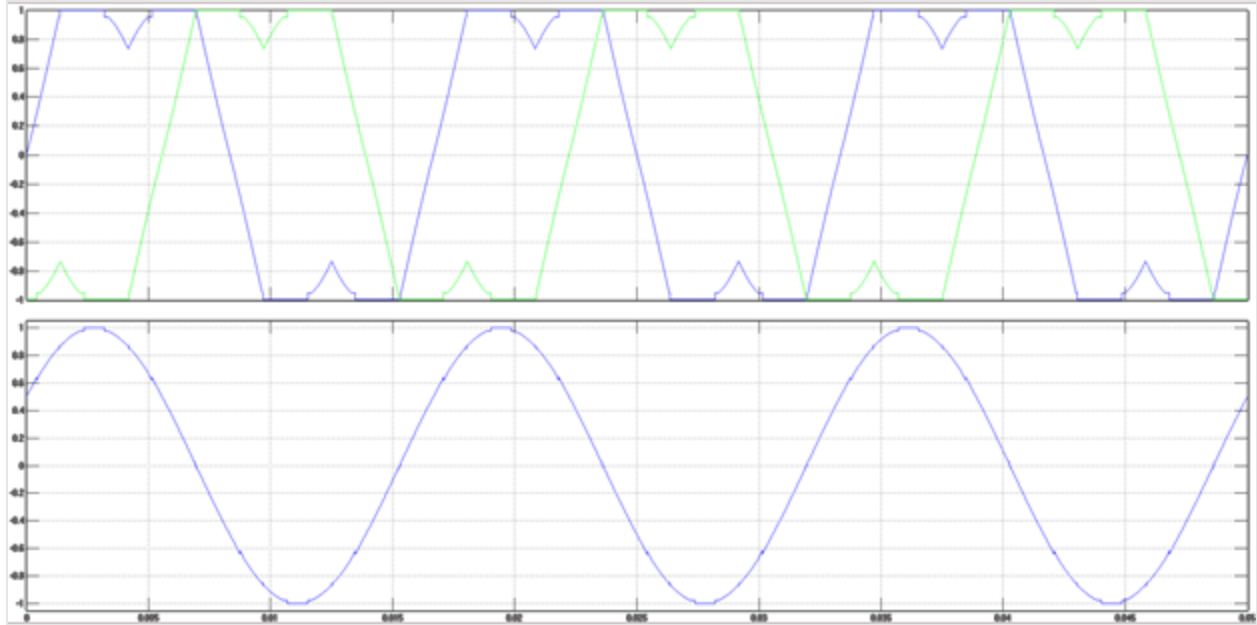


Figure 2. 64. DDPWM at $\theta=90^\circ$ – a) Phase a and b references b) Phase to phase ab reference waveform

Figure 2.65. shows a voltage error waveform due to introduction of MPW limitation of 3us in case of DDPWM at $\theta = 90^\circ$, $m = 1$ and $cf = 69$. Voltage error waveform is represented as a very narrow set of single pulses, occurring around minimum and maximum duty cycle values, with the amplitude equal to DC bus voltage value $\pm V_{dc}$, depending on the whether the pulse was held at MPW value or dropped. This waveform resembles very much on the voltage error waveform in case of dead time introduction, with the difference of error pulses not occurring during every switching cycle, but only certain number of times during fundamental cycle.

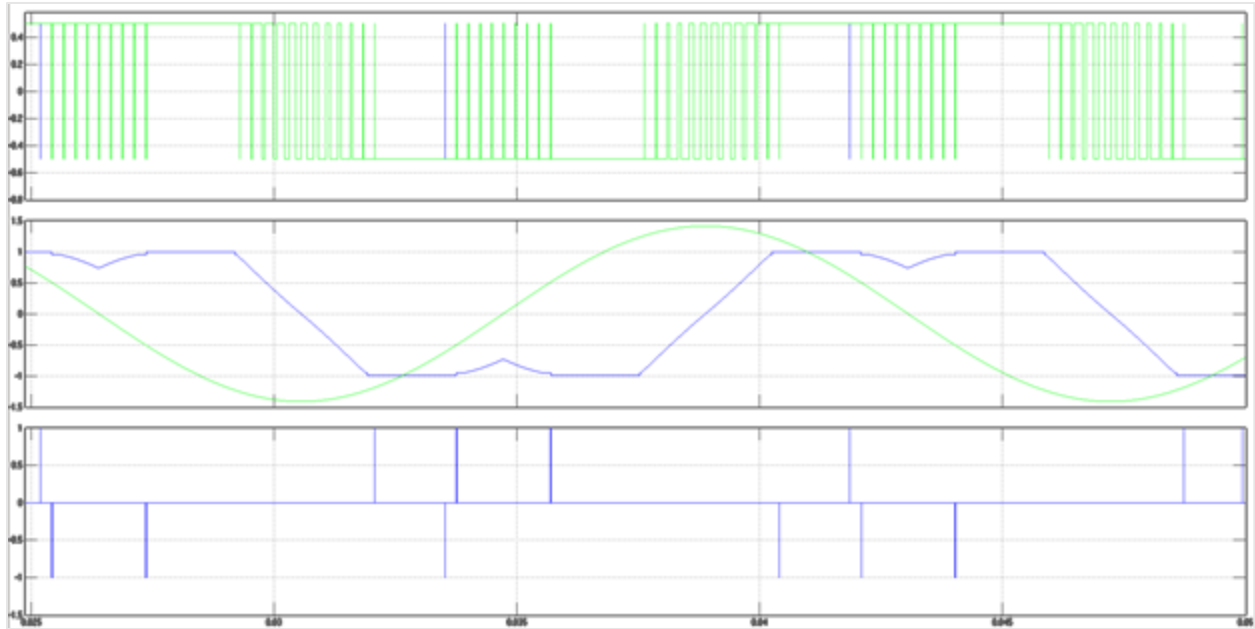


Figure 2. 65. DDPWM at $\theta=90^\circ$ a) Ideal and corrected waveform b) Phase voltage and current c) Output Voltage Error

Harmonic analysis of the voltage error waveform was performed based on the simulation model for DDPWM at phase angle difference of 90° , at $cf = 69$ and $0 < m < 1$ for $T_{mpw} = 3\mu s$. Incremental harmonic difference spectrum introduced by MPW limitation is shown in Figure 2.66.

Harmonic values are higher in the higher frequency range, with overall low incremental values.

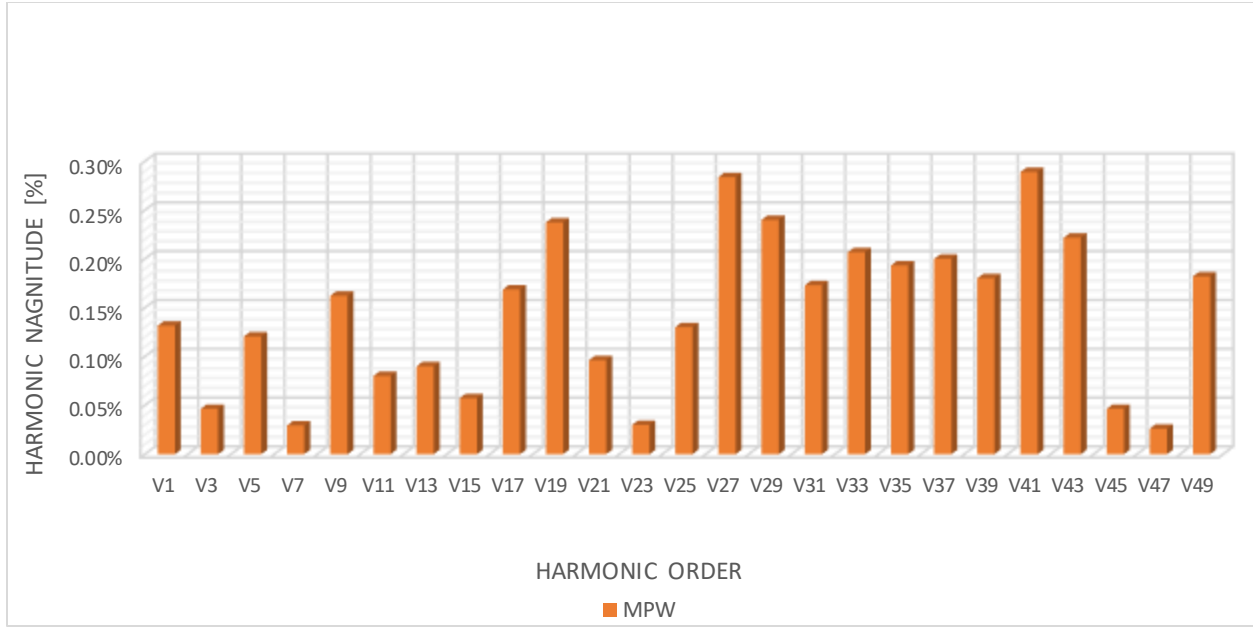


Figure 2. 66. Low Order Harmonic Spectra for Voltage Error signal for Tmpw=3us

Similar as in forward voltage drop case study, MPW limitation introduces inherently low values of added harmonics to output voltage waveform, and therefore it will only be used for current harmonic study as part of the simulated switching model.

Besides the effects that dead time and minimum pulse width limitations along with voltage drops and rise and fall times of the switches have on the harmonic performance of the MTI, there is an impact on the fundamental harmonic as well. Despite the fact that the magnitude and phase differences of the fundamental waveform are expected to be corrected by the current controller, it is important to define those based on the parameters mentioned. Difference between the actual and the ideal fundamental voltage waveforms is defined as:

$$\Delta V = V_{actual} - V_{ideal}$$

Magnitude and phase angle of ΔV per phase is defined as:

$$|\Delta V| = \left(k * \frac{V_{dc} \left(\frac{T_{off}}{2} + \frac{T_{on}}{2} + T_d \right)}{T_s} + \frac{V_{ce} + V_d}{2} \right) * \frac{4}{\pi} + \frac{R_{ce} + R_d}{2} * |I| \quad (2.50.)$$

$$angle(\Delta V) = \angle(I) + \pi \quad (2.51.)$$

Where $k = \frac{2}{3}$ for DPWM and $k = 1$ for CPWM. It is very important to notice that the angle of the ΔV is phase shifted by 180° from output current. Therefore, negative power factors will always result in voltage gain of the actual voltage fundamental on the output as compared to the ideal voltage reference. Phasor in Figure 2.67. shows a case of MTI providing reactive power to the output, thus $\angle(I) = -90^\circ$.

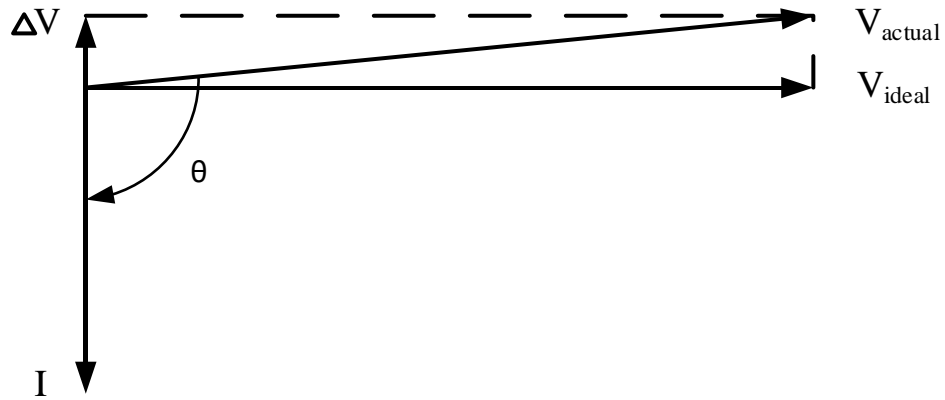


Figure 2. 67. Voltage and current phasor for $\theta_{ideal}=-90^\circ$

Actual voltage fundamental magnitude is increased, and voltage is phase shifted. In order to quantify the overall impact on the actual output voltage fundamental in realistic application, an MTI example calculation has been performed using following parameters $V_{dc} = 750V$, $I_m = 1727A$, $Td + \frac{T_{on}}{2} - \frac{T_{off}}{2} = 3\mu s$, $V_{ce} = V_d = 0.8V$, $R_{ce} = 0.073m\Omega$, $R_d = 0.046m\Omega$, which resulted in $|\Delta V| = 9.96V$ and $\angle(\Delta V) = 90^\circ$. That resulted in increase of actual output voltage of 0.026% and angle difference of. 1.31°

Based on Equations (2.50) and (2.51.), one can notice that Minimum pulse width limitation does not contribute to the output fundamental voltage difference at all. This is due to the usage of

previously described solution for minimum pulse width limitation implementation that reproduces the average value of the volt-seconds over a switching period, and therefore it does not have any effect on the fundamental voltage waveform. Other implementations of MPW limitation affect the fundamental voltage and reduce voltage linearity limit [52] but will not be considered as part of the MTI design.

2.5.4. Output Current Harmonics

From low order harmonic analysis previously covered, it is clear that discontinuous switching patterns lead to worse low order harmonic performance compared to continuous modulation. However, the advantage of these strategies is the reduction in the number of switching transitions per phase leg over each fundamental cycle by 33%.

This reduction allows the usage of increased carrier frequency as compared to CPWM strategies. Alternative, advantage over CPWM strategies could be the increased power rating of the inverter under usage of same carrier frequency, due to decreased switching losses of the power semiconductors, which are typically the limiting factor for high power applications.

On top of low order voltage harmonics, it is also important to quantify high frequency current harmonics as well, since high frequency current harmonic levels are important for LCL filter design. However, it is a very complex and rather unnecessary task to quantify all the sideband current harmonics around different carrier multipliers. In order to compare various modulation methods, literature [8], [53]-[55] provides closed form solution for harmonic currents by calculating normalized current ripple *rms* value r_{rms} for each of those modulation techniques. That data is represented in Table 2.4 in a different form based on modulation index value and compared against DDPWM at various phase angle θ values. Certain phase angle θ ranges for

DDPWM are not represented in Table 2.4 because sliding ranges of DDPWM, per table 2.1, will not have a constant ripple current characteristic, so will be characterized by the area between curves defined in Figure 2.68.

Normalized Current Ripple <i>rms</i> Value	Modulation Techniques
$r_{rms} = \frac{1}{8\sqrt{3}} \sqrt{2m^2 - \frac{32}{3\pi}m^3 + 2m^4}$	<i>SPWM</i>
$r_{rms} = \frac{1}{8\sqrt{3}} \sqrt{2m^2 - \frac{32}{3\pi}m^3 + \frac{16}{9}m^4}$	<i>THI PWM</i>
$r_{rms} = \frac{1}{8\sqrt{3}} \sqrt{2m^2 - \frac{32}{3\pi}m^3 + 2m^4 \left(\frac{3}{2} - \frac{9\sqrt{3}}{8\pi} \right)}$	<i>SVPWM</i>
$r_{rms} = \frac{1}{8\sqrt{3}} \sqrt{8m^2 - \frac{140}{3\pi}m^3 + 6m^4 \left(1 + \frac{3\sqrt{3}}{8\pi} \right)}$	<i>DDPWM</i> $-150^\circ < \theta < -120^\circ$ $-60^\circ < \theta < -30^\circ$ $30^\circ < \theta < 60^\circ$ $120^\circ < \theta < 150^\circ$
$r_{rms} = \frac{1}{8\sqrt{3}} \sqrt{8m^2 - \frac{8m^3}{3\pi} \left(\frac{15\sqrt{3}}{2} + 4 \right) + 6m^4 \left(1 + \frac{\sqrt{3}}{4\pi} \right)}$	<i>DDPWM</i> $\theta = -180^\circ$ $\theta = 0^\circ$
$r_{rms} = \frac{1}{8\sqrt{3}} \sqrt{8m^2 + \frac{8m^3}{3\pi} \left(\frac{15\sqrt{3}}{2} - 31 \right) + 6m^4 \left(1 + \frac{\sqrt{3}}{2\pi} \right)}$	<i>DDPWM</i> $\theta = -90^\circ$ $\theta = 90^\circ$

Table 2. 4. Normalized current ripple *rms* value comparison for various modulation techniques.

This approach is good approximation for purely inductive loads such as electrical machines and magnetics. With inductive load, the load current will rise and fall linearly about its target value over one carrier interval and the overall current ripple *rms* is calculated by integrating this equation over a positive half fundamental cycle. The normalized current ripple *rms* function for the various modulation strategies is compared in Figure 2.68.

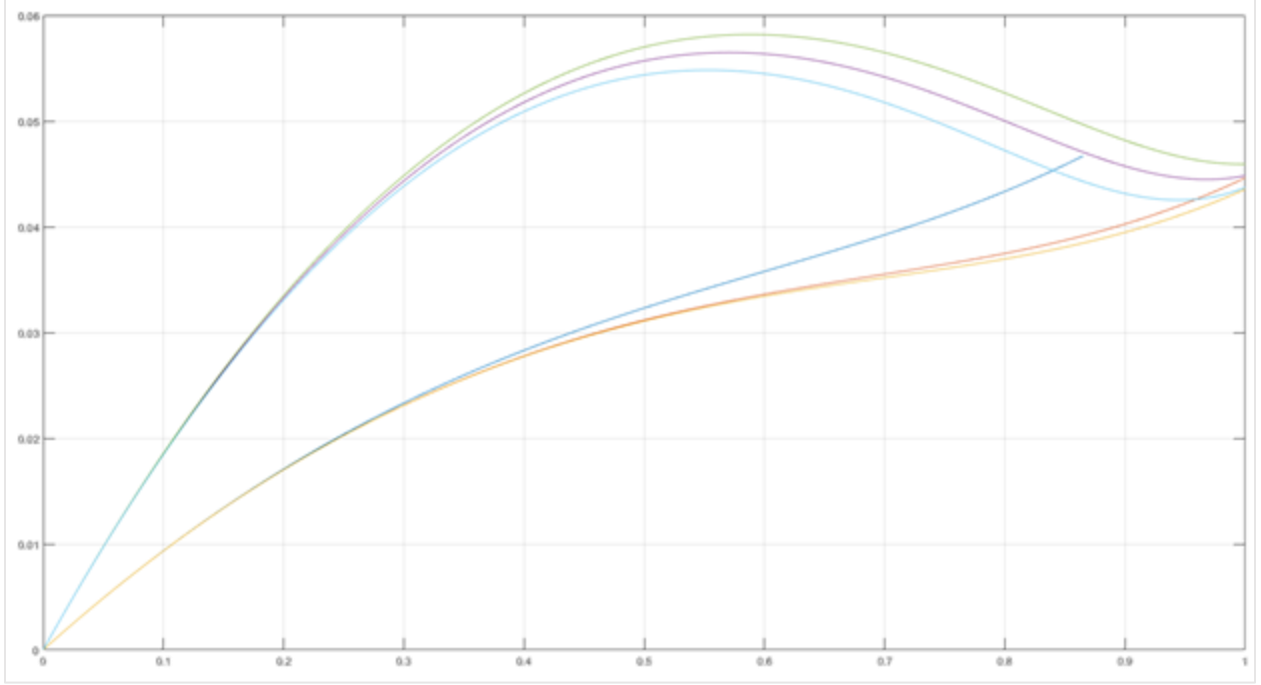


Figure 2. 68. Normalized current ripple rms function

Figure 2.68. confirms the overall superiority of the continuous over discontinuous modulation strategies in terms of ripple current harmonic distortion, when same switching frequency is considered. However, for high modulation index values, DDPWM technique produces comparable results to CPWM even for same switching frequencies.

While ripple current rms value is very useful for sizing of the converter side inductor and capacitor, it does not provide enough information required for design of the LCL low pass harmonic filter. Therefore, it is useful to define the maximum peak to peak value of the current ripple over the whole fundamental period as function of the modulation index for DDPWM as well as CPWM techniques:

$$i_{pp} = \frac{V_{dc}}{f_{sw}L_1} r_{pp}(m) \quad (2.52.)$$

$$r_{max}(m) = \begin{cases} m\left(\frac{2}{\sqrt{3}} - m\right); & \text{for } m \leq 0.821 \\ \frac{m}{3} & ; \text{for } m \geq 0.821 \end{cases} \quad \text{for DDPWM}$$

$$r_{max}(m) = \begin{cases} m \left(\frac{1}{\sqrt{3}} - \frac{m}{2} \right); & \text{for } m \leq 0.487 \\ \frac{m}{3} & ; \text{for } m \geq 0.487 \end{cases} \text{ for CPWM}$$

The maximum value of the normalized current ripple r_{pp} as a function of the modulation index for all DPWM and CPWM techniques is presented in Figure 2.69.

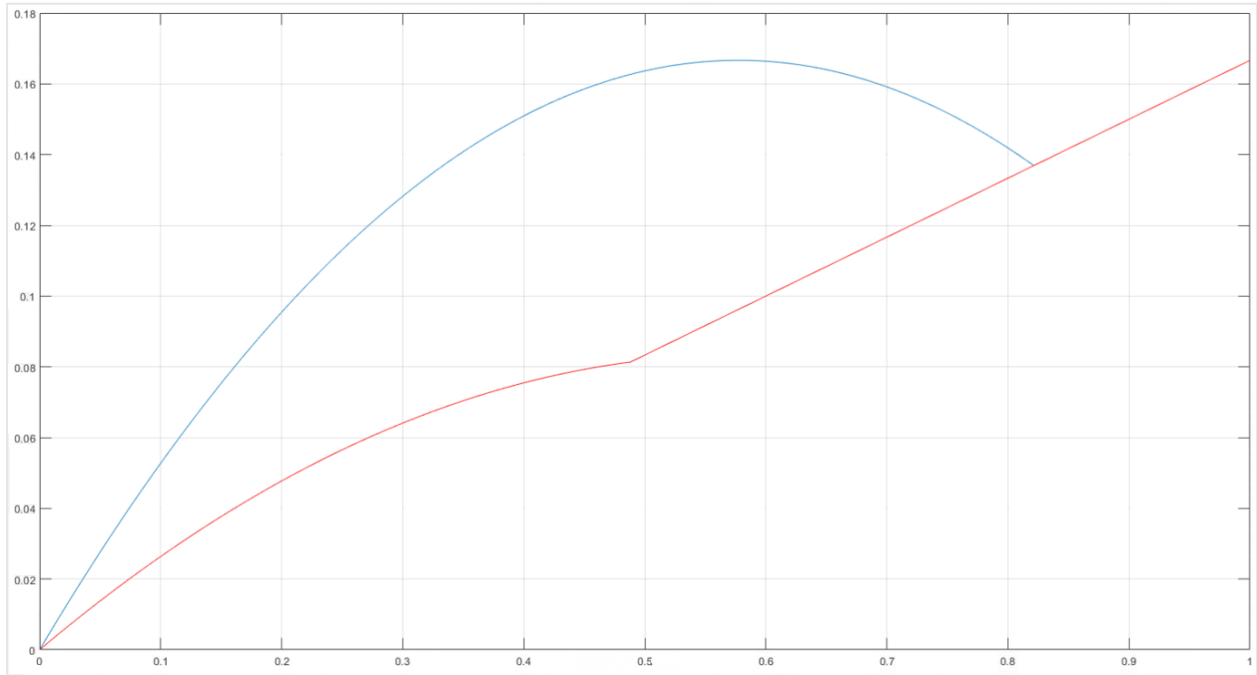


Figure 2. 69. Maximum normalized peak to peak value of the current ripple

For modulation index values up to 0.821, maximum normalized peak to peak ripple current value is lower for CPWM, when considering the same average switching frequency. For $m > 0.821$ CPWM and DDPWM become equal.

Neither *rms* nor maximum peak to peak value of the current ripple provide the value for some of the specific high frequency harmonics of interest for microgrid tie inverter design. Depending on the harmonic standards applied, LCL filter parameters are sometimes designed considering the most significant grid current harmonic. If the limitation for the spectral content of the output current harmonics in high frequency range exist, sideband harmonic values around the switching frequency and multiples of the switching frequency become important.

In case of a constant harmonic attenuation requirement in high frequency range, the dominant harmonics in the first sideband are the hardest ones to achieve due to the highest harmonic voltage amplitude to filter gain ratio. Harmonic voltage amplitude to filter gain ratio is a measure of the potential of the voltage harmonic to produce a corresponding current harmonic. Typically, for inverter applications where $cf > 50$, sideband harmonics of $cf - 2$ and $cf - 4$ order are the ones with highest ratio, thus dictating lower limits of the LCL filter parameters.

Each of the modulation strategies discussed previously have been analyzed in order to obtain magnitudes for each of the two voltage sideband harmonics in PWM waveform in relation to modulation index m . A carrier to fundamental ratio of $cf=69$ for DDPWM at $\theta = -90^\circ$ was selected as an example, and harmonic spectrum around carrier frequency for various modulation index values is shown in Figure 2.70.

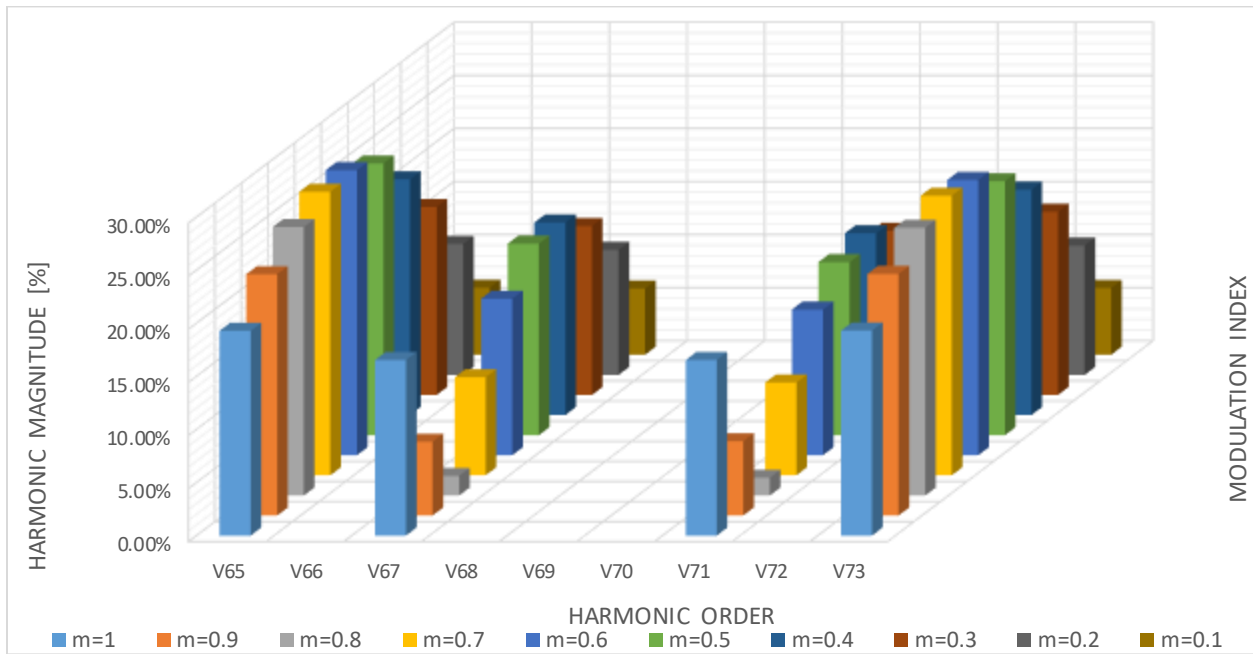


Figure 2. 70. Switching Frequency Sideband Voltage Harmonic Spectra for DDPWM at $\theta = -90^\circ$ with $cf = 69$

Normalized voltage harmonics for $(cf - 2)$ and $(cf - 4)$ for various modulation techniques across full modulation index range is shown in Figures 2.71. and 2.72. respectively. It

is important to point out that the voltage harmonic values are independent of the carrier frequency selection, and only unique in terms of position in respect to carrier frequency.

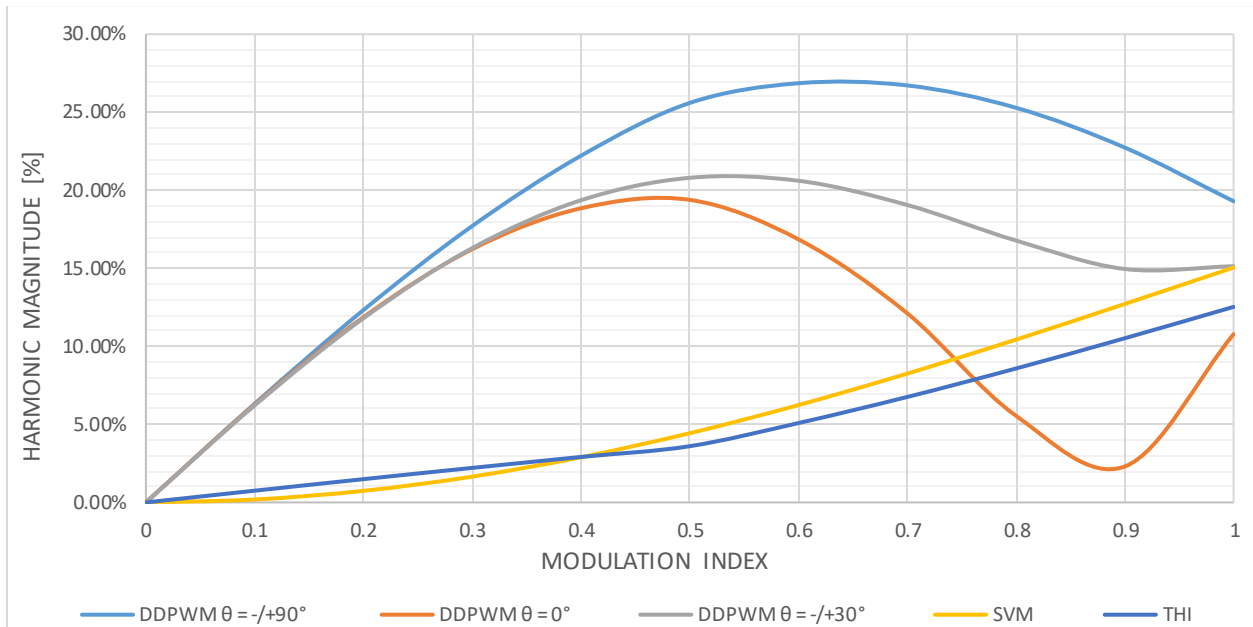


Figure 2. 71. Normalized (cf-4) order voltage harmonic

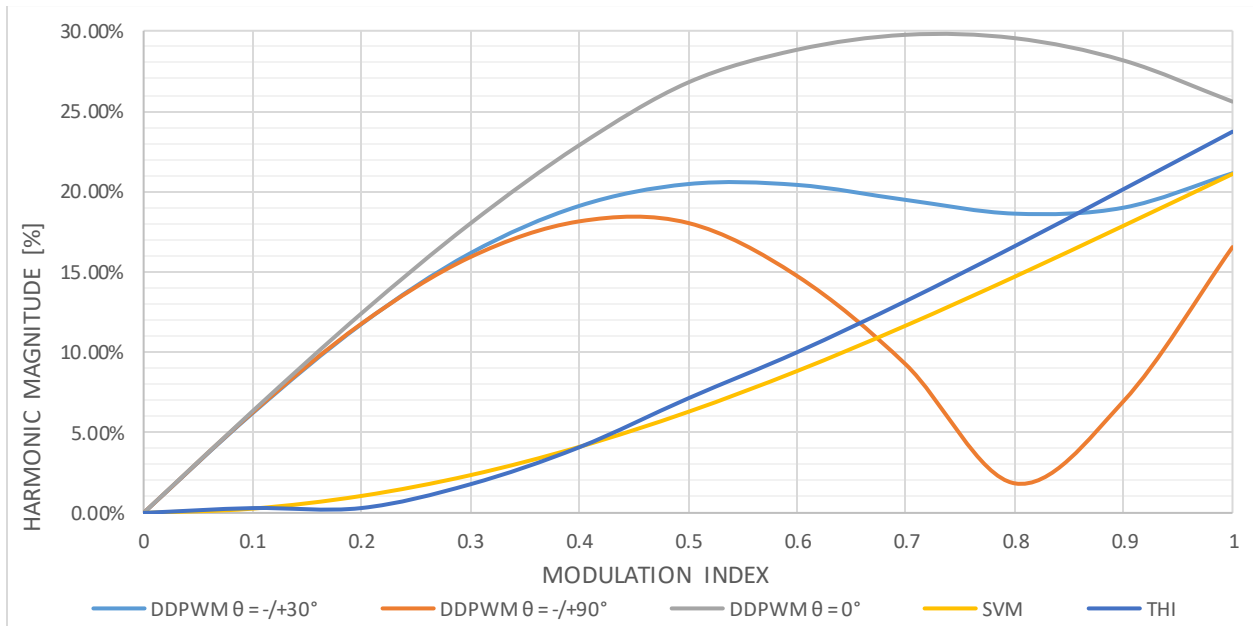


Figure 2. 72. Normalized (cf-2) order voltage harmonic

By comparing the actual sideband harmonic values in Figures 2.70 and 2.71. with the *rms* and maximum peak to peak ripple current values in Figures 2.67 and 2.68 it is obvious that there

is a noticeable difference between particular harmonic values for different modulation technique that is not reflected thru the factors shown in Figures 2.71. and 2.72. Therefore, in cases where attenuation of high frequency harmonics exist as a design requirement, it is essential to perform individual harmonic analysis, rather than relying on other harmonic performance measures already existing in the literature.

2.5.5. DC Input Current Harmonics

Another important characteristic of a certain PWM inverter modulation technique is the DC link current. As opposed to inverter output current characterization, which was thoroughly investigated in literature, dc bus current has gotten less attention. Characterization of DC link current is important for design and performance evaluation of MTI. As per Figure 2.73., DC link current I_{in} consists of source current I_{dc} and capacitor current I_{ac} .

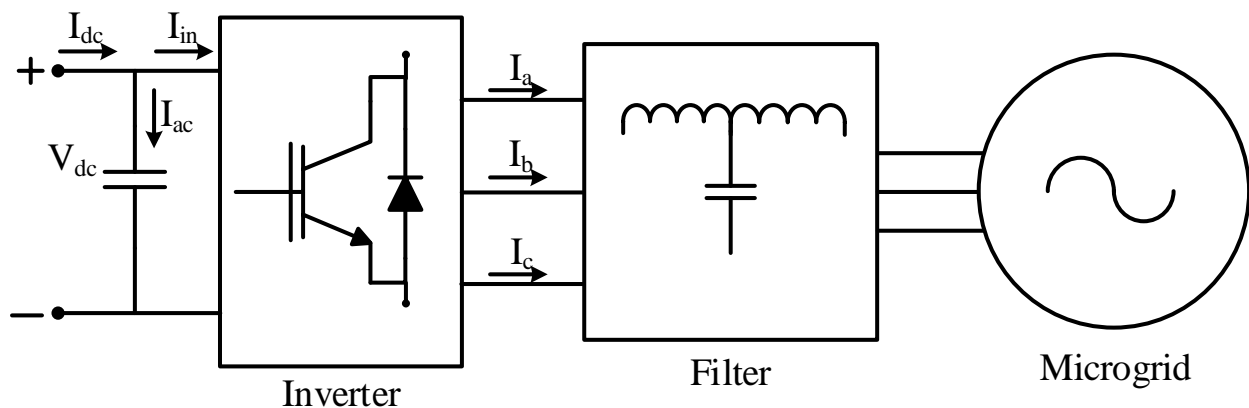


Figure 2. 73. Simplify circuit illustrating DC-Bus current components of MTI.

Since capacitance value in MTI is selected as large by design, it will be considered infinite for the ease of analysis. Also, for the same purpose, dc link voltage value will be considered constant and powered from ideal DC current supply. Finally, steady state operating conditions and

load currents with no harmonics are assumed. In such case, total DC link current I_{in} can be broken down into dc component I_{dc} and ac component I_{ac} , sourced from source and capacitor sides respectively.

I_{dc} corresponds to the average power transfer to the load, and can be represented as a function of the modulation index m , output load current rms value, and load power factor:

$$I_{dc} = \sqrt{\frac{3}{2}} m I_{rms} \cos \theta \quad (2.53.)$$

Formula above is purely derived based on the power transfer formula which shows linear dependency on all three before mentioned parameters, and is independent on modulation technique used.

On the other hand, AC component of dc link current I_{ac} , is a consequence of PWM switching. During zero switching states, where all 3 top or bottom switches are on, DC link capacitors are bypassed and do not participate in the current flowing path in the circuit. Therefore, the rms value of the ripple current is independent of the distribution of zero switching states inside the switching period, and are independent on the modulation technique used [53]. Also, the duration of each of the six active vectors is unrelated to switching frequency value, thus making rms value of I_{ac} independent of switching frequency [53]. The most practical way to calculate rms value of I_{ac} is to evaluate rms value per switching period over a shortest repetitive period, being equal to 1/6th of fundamental cycle [27].

Therefore, rms value of capacitor current I_{ac} can be represented as a function of the modulation index m , output load current rms value, and load power factor:

$$I_{ac} = I_{rms} \sqrt{\frac{m}{\pi} + \left(\frac{4}{\pi} - \frac{2}{3}m\right) m \cos^2 \theta} \quad (2.54.)$$

Dependency of *rms* value of capacitor ripple current I_{ac} as a percentage of output load current value for various power factor values across full modulation index range is shown in Figure 2.74.

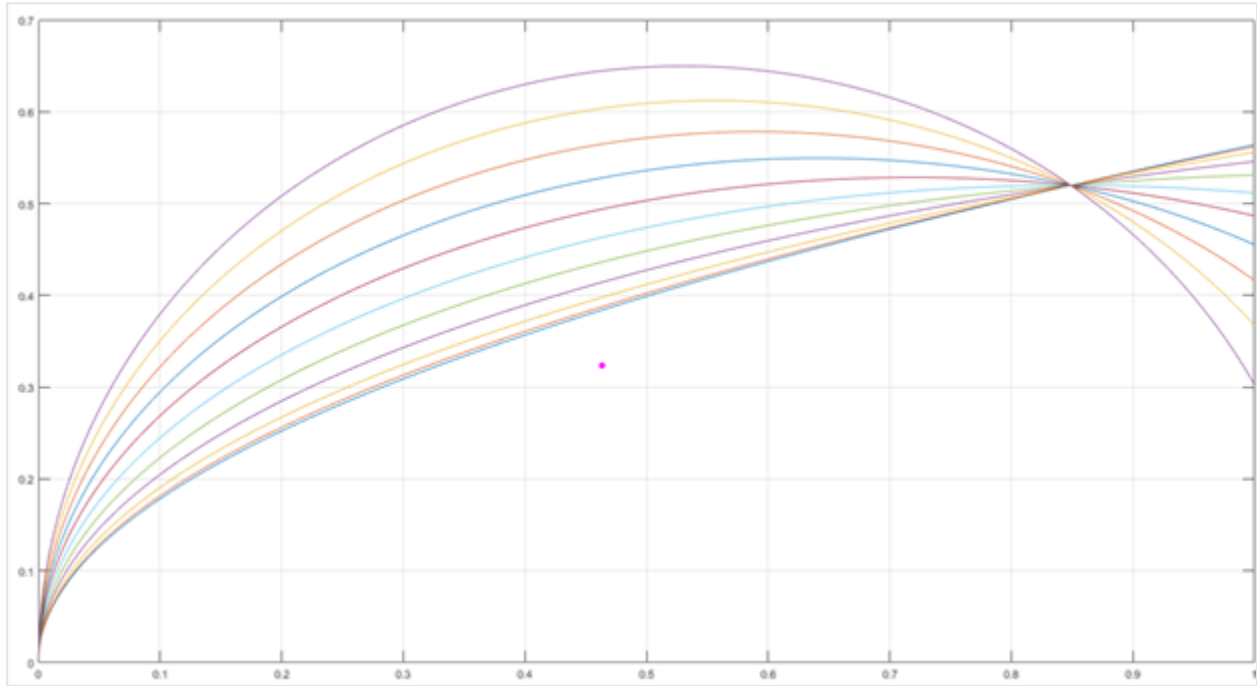


Figure 2. 74. *rms* value of capacitor ripple current I_{ac}

Absolute maximum value of *rms* value of I_{ac} occurs at unity power value and $m = 0.53$, which represent the worst case scenario within the full range of modulation index values. However, at $m = 0.85$, *rms* value becomes unique for all power factor values, and for values m higher than 0.85 operation at lower power factor values become more critical.

Although the *rms* value of I_{ac} is independent of the PWM method used, harmonic spectrum of capacitor ripple current is strongly affected by it [56]. Since dc bus capacitor parameters have frequency dependent characteristics, spectral attributes of capacitor ripple current are of major

importance for thermal performance and voltage ripple [57]-[60]. However, literature does not cover spectral content of various PWM methods at conditions other than unity power factor. Therefore, spectral characterization of DDPWM and SVPWM will be performed across full range of power factor values based on Fourier analysis.

Prior to that, the time domain waveforms of DC capacitor ripple current is presented in Figures 2.75. and 2.76. as an example for SVPWM and DDPWM methods for $m = 0.85$ and $PF = 1$ condition.

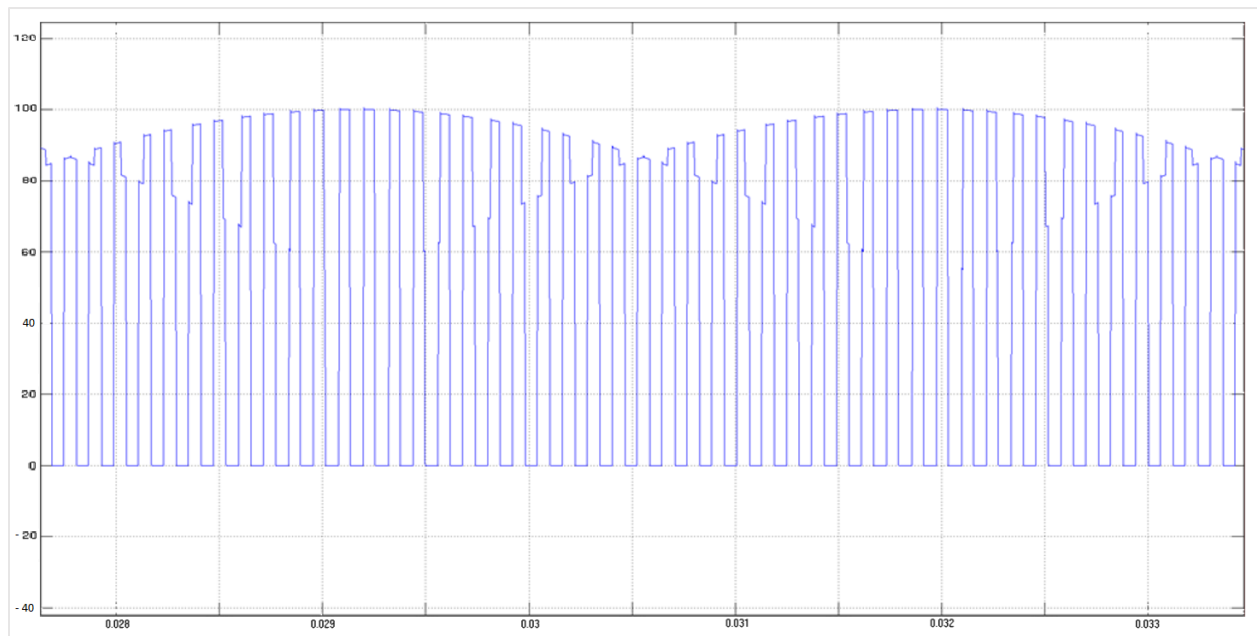


Figure 2. 75. Time domain waveforms of DC capacitor ripple current for SVPWM for $m=0.85$ and $PF=1$

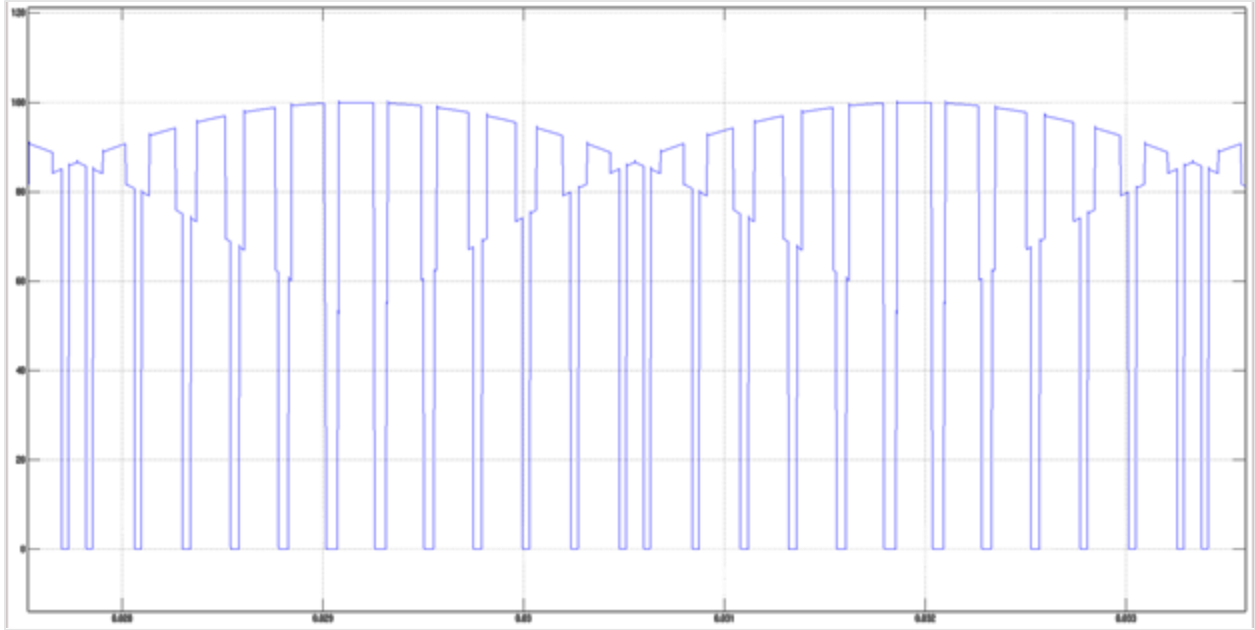


Figure 2. 76. Time domain waveforms of DC capacitor ripple current for DDPWM for $m=0.85$ and $PF=1$

As can be concluded from Figures 2.75. and 2.76., both modulation techniques consist of high frequency components represented as a multiplier of carrier frequency, but with an obviously larger multiplier present with SVPWM.

In order to characterize DDPWM and SVPWM methods in a normalized form, Harmonic spectrum of time domain ripple current waveforms are obtained as a function of modulation index and power factor value.

Harmonics of $cf + 3/-3$ and $2cf$ order are the ones with significant magnitudes, thus harmonic spectrum for various modulation index values and $cf = 69$ is shown in Figures 2.77. and 2.78. for DDPWM and SVPWM respectively.

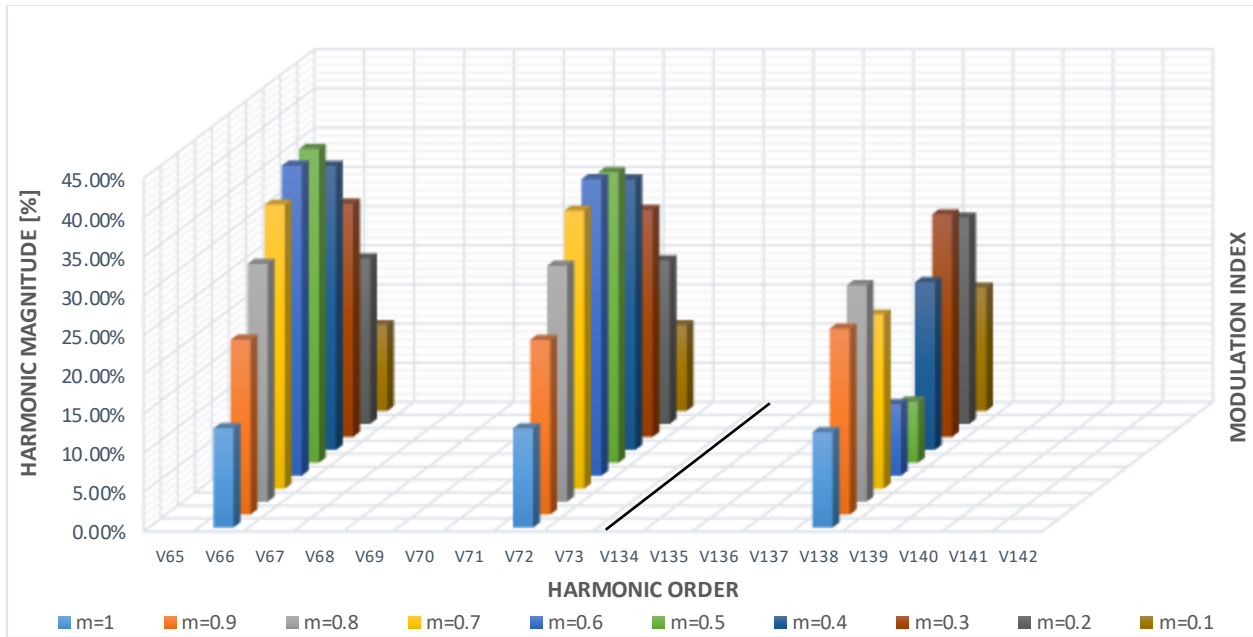


Figure 2. 77. DC Bus Ripple Current Harmonic Spectra for DDPWM with $cf=69$

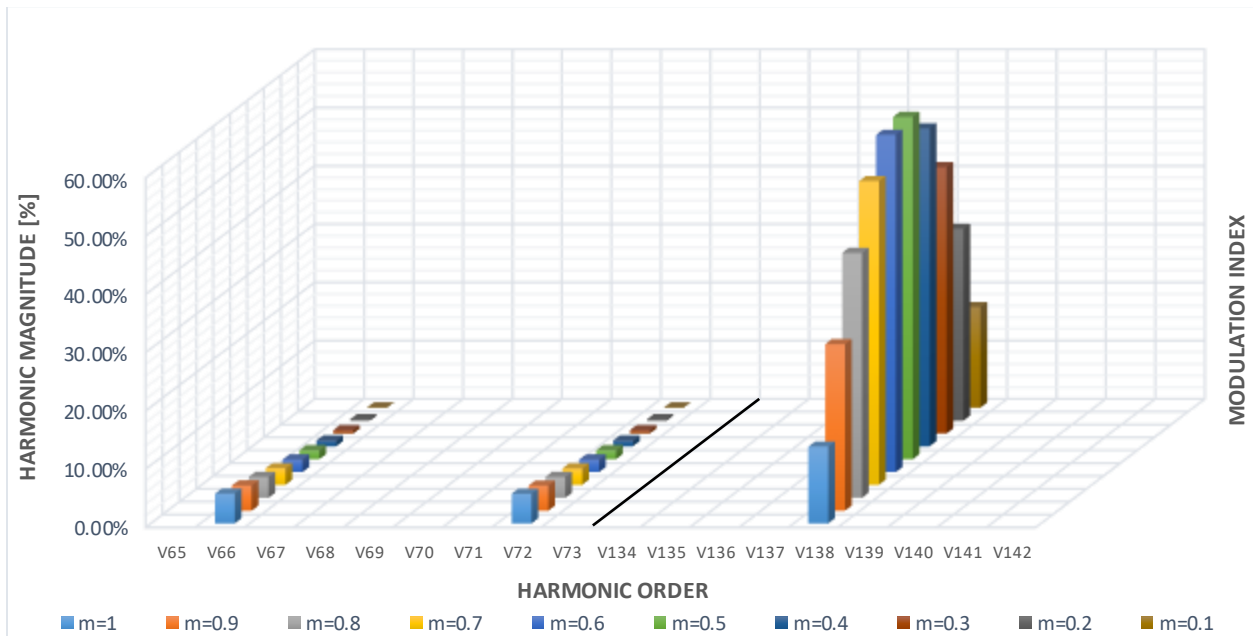


Figure 2. 78. DC Bus Ripple Current Harmonic Spectra for SVPWM with $cf=69$

Normalized current harmonics for $cf + 3/-3$ and $2cf$ for various modulation index values across full power factor range is shown in Figures 2.79., 2.80., 2.81. and 2.82. for DDPWM and SVPWM respectively. Once again, current harmonic values are independent of the carrier frequency selection, and unique in terms of position in respect to carrier frequency.

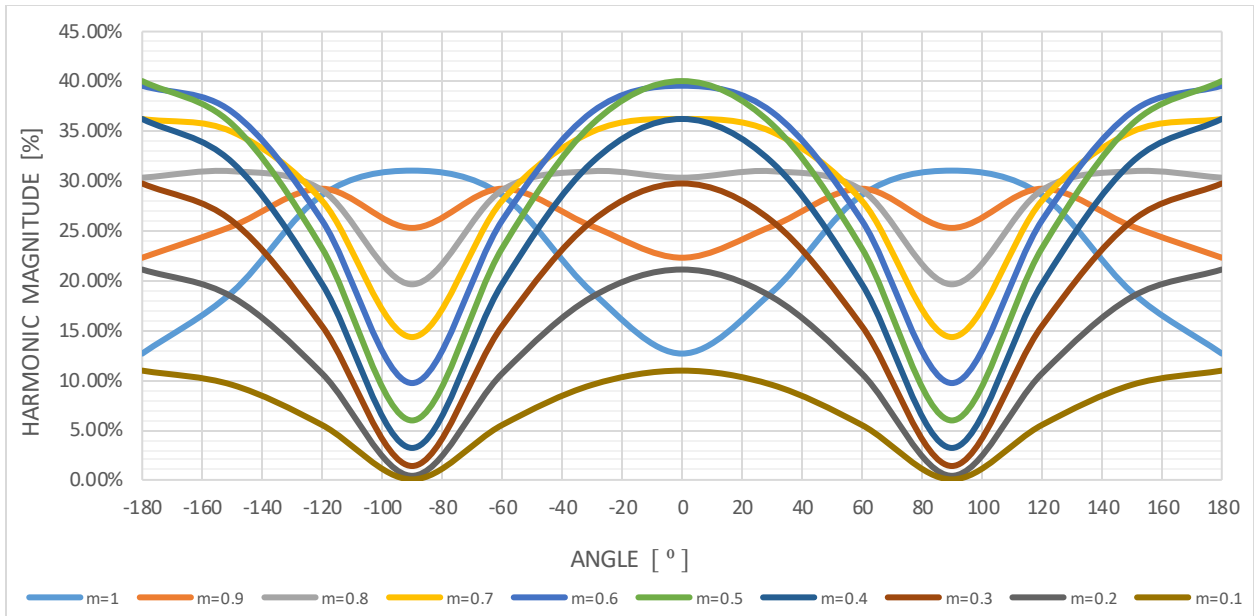


Figure 2. 79. Normalized cf+3/-3 order DC ripple current harmonic for DDPWM across full power factor range

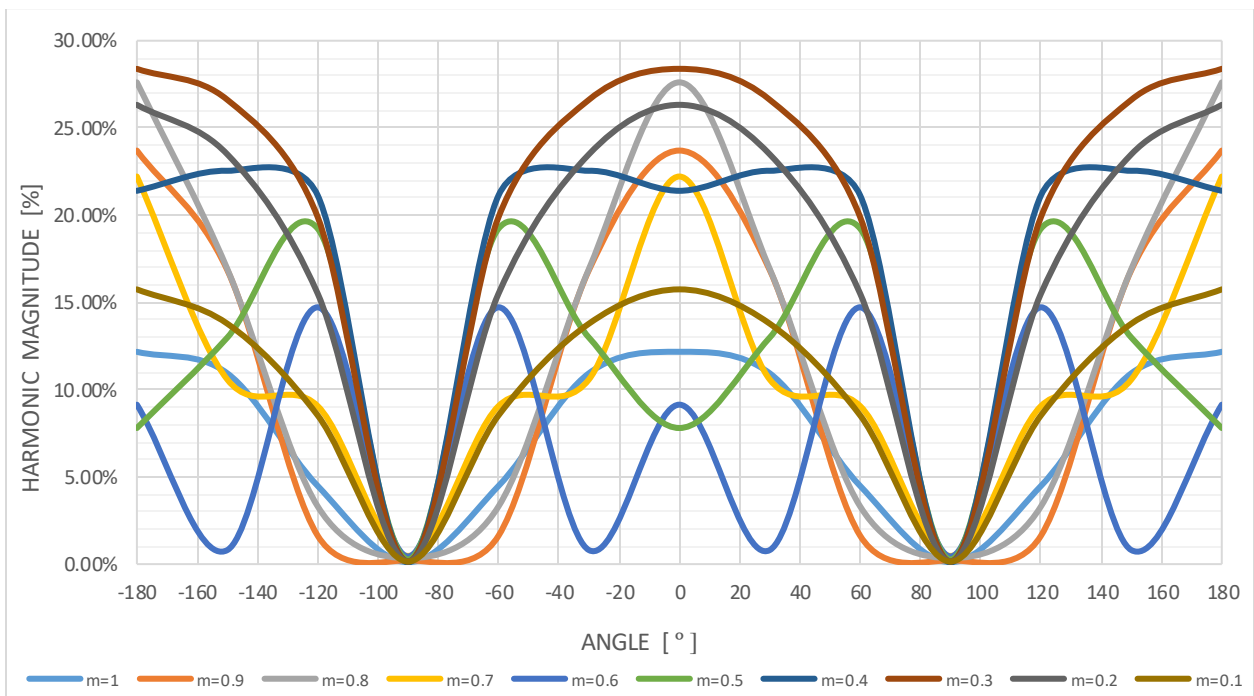


Figure 2. 80. Normalized 2cf order DC ripple current harmonic for DDPWM across full power factor range

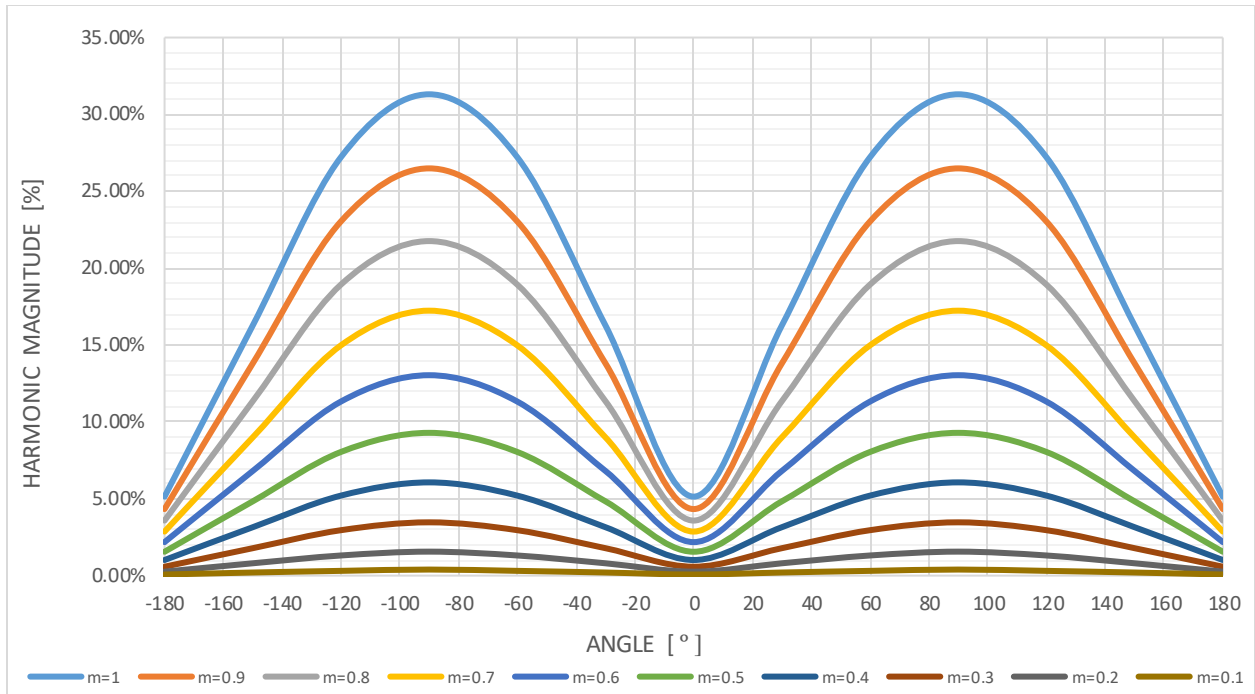


Figure 2. 81. Normalized cf+3/-3 order DC ripple current harmonic for SVPWM across full power factor range

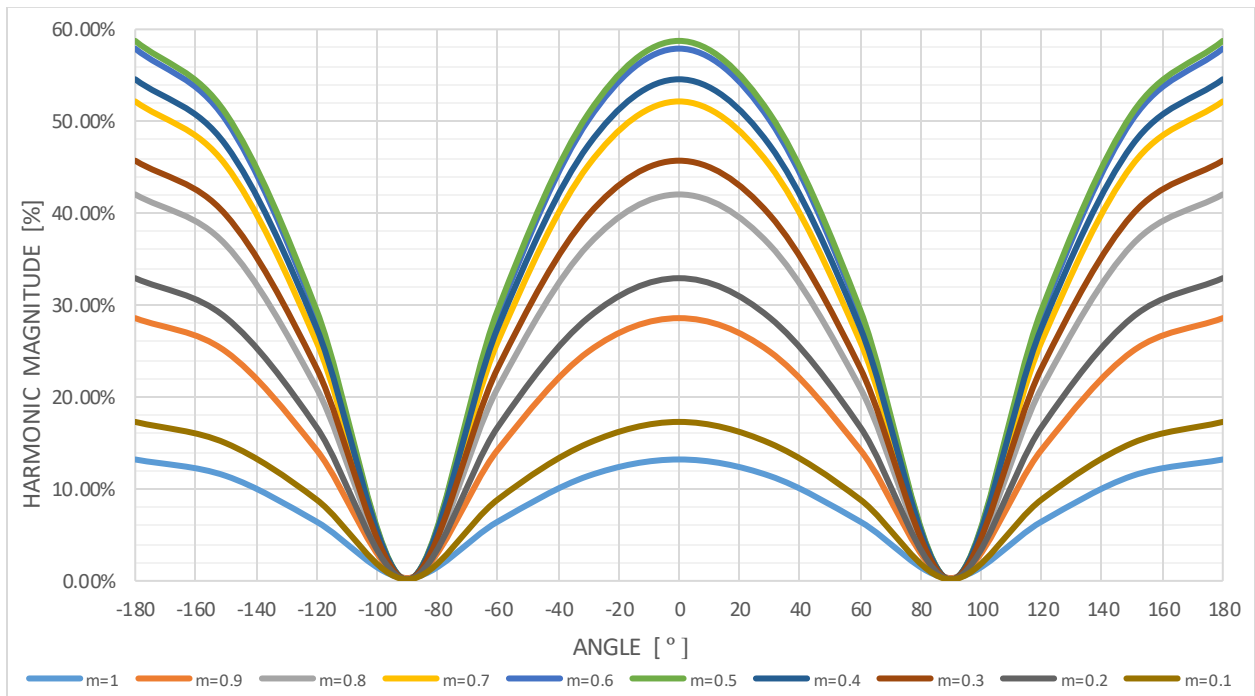


Figure 2. 82. Normalized 2cf order DC ripple current harmonic for SVPWM across full power factor range

Despite the fact that rms values of DC bus current ripple is independent of modulation type, there is an obvious difference in harmonic spectrum between DDPWM and SVPWM, based on

Figures 2.77. – 2.82. above. At unity power factor condition, SVPWM has very dominant $2cf$ harmonic, which changes with modulation index value, and peaks at $m = 0.53$ at 60% of fundamental output current. As absolute value of power factor angle decreases, $2cf$ harmonic value also decreases and becomes zero at $PF = 0$ condition. On the other hand, $cf + 3/-3$ increases its value with power factor decrease and modulation index increase and peaks at $PF = 0$ and $m = 1$ conditions with 31% of fundamental current, which is the same value as DDPWM under this condition. On the other hand, DDPWM shows less consistent harmonic behavior with maximum $cf + 3/-3$ value at unity power factor and $m = 0.53$ at 41.5% of the fundamental output current. Also, DDPWM shows zero value for $2cf$ at $PF = 0$ condition and has maximum of 29% at $m = 0.76$. It is important to emphasize that in cases where $PF = 0$ represents the maximum DC bus ripple current case, which is the case with MTI operating at higher m values, SVPWM and DDPWM have identical harmonic spectrums as well.

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3. MTI Low Pass Harmonic Filter

3.1. LCL Filter Design

Passive filter design for voltage source inverter applications is known to be a complex task. Typically, a first order L type filter or a 3rd order LCL type filter is to be used to filter the switched voltage waveform and limit current harmonic content. The LCL filter has shown to achieve very effective high frequency attenuation with significantly reduced inductance requirement [1][2], thus making it a preferred solution for voltage source inverter applications. Because of mentioned advantages, it is currently widely used in distributed generation applications [3], [4] as well as active power filters [5]. Basic guidelines for selection of LCL-filter parameters using an iterative process based on the current ripple attenuation are presented in [1] and [6]. On the contrary [7] focuses on filter parameter selection based on analytical solution of inverter harmonics. Multiple optimization criteria based on minimization of stored energy [7], losses [8] and volume [9] have been proposed. However, all of the aforementioned studies and algorithms are focused on filter design intended for unity power factor operation, thus not being adequate for MTI application.

The primary role of the LCL filter is to reduce high-order harmonics on the grid side. Inappropriate filter design will lead to poor performance reflected in lower than expected attenuation levels. Sometimes other effects like resonance or inductor saturation may occur. Therefore, the filter should be designed with several characteristics in consideration such as current ripple, filter size and switching ripple attenuation. Also filter design should provide sufficient damping and robustness to harmonics and asymmetries. On the other hand, the filter design is limited by filter size and cost related constraints.

The procedure for selecting the LCL filter parameters is based on the frequency approach and requires following system level parameters:

V_{ll} , line-to-line RMS voltage (inverter output); V_{ph} , phase voltage (inverter output); S_n rated apparent power; V_{dc} , dc-link voltage; f_g , grid frequency; f_{sw} , switching frequency; and f_{res} , resonance frequency.

The base impedance, base capacitance and base inductance are defined respectively by:

$$Z_b = \frac{U_{ll}^2}{S_n} \quad (3.1.)$$

$$C_b = \frac{1}{\omega_g Z_b} \quad (3.2.)$$

$$L_b = \frac{Z_b}{\omega_g} \quad (3.3.)$$

The peak to peak current ripple represents the difference between the peak volt-seconds and the average volt-seconds applied to the inductor over the switching period. For simplification purpose, the influence of the filter capacitance on the current ripple is neglected. The equation for approximation of the maximum peak to peak current ripple for DDPWM modulation has been derived in chapter 2.5.4, and will be used to approximate the maximum peak-to-peak current ripple on the inductor L_1 :

$$\Delta I_{L_{max}} = \frac{V_{dc}}{6f_{sw}L_1} \quad (3.4.)$$

Inverter DC link voltage is targeted to be the lowest voltage that is capable of providing a full reactive power generation capability at the highest line voltage condition, which is typically specified as 10% higher than the rated voltage. This condition differs from a standard grid tie LCL filter design which assumes full active power generation, because the worst-case condition in MTI assumes full reactive power delivery. In order to achieve a capability of providing a full reactive

power, inverter requires higher inverter side voltage which demands higher dc link voltage values. Higher DC link voltage values lead to other issues like need for higher voltage ratings of various components in a circuit, higher switching ripple and overall component losses, and therefore is crucial for the overall inverter design. Also, for the worst case DC bus condition calculation, inverter is assumed to always run in the linear region, meaning no over modulation is present under any condition. The theoretical limit of DDPWM linear region has been calculated in chapter 2.5.1 as 1.

At full reactive power generation condition, total voltage drop across the filter in percentage can be approximated as the:

$$V_{drop}(\%) = \frac{L_1(\%) + L_2(\%) \left(1 - \frac{cf(\%)}{100}\right)}{1.1} \quad (3.5.)$$

Since filter capacitance has a negligible effect on the overall voltage drop across the filter, voltage drop minimization cannot be treated as a design constraint.

This voltage drop needs to be added to the highest line condition in order to calculate the minimum inverter dc bus voltage.

$$V_{dc} = 1.1V_{ll}\sqrt{2}\left(1 + \frac{V_{drop}}{100}\right) \quad (3.6.)$$

Since inverter operation at high line voltage and full reactive power generation requires high DC bus voltage levels, in order to keep all the components within standard ratings, it may be necessary to use a transformer on the secondary side of the filter. This results in a step-down condition of the line voltage on the inverter side, which allows usage of lower standard ratings of components such as semiconductor switches, DC bus capacitors, filter capacitors etc. Also, isolation transformer can be designed such that it's leakage inductance can serve a purpose of a

secondary inductor in a filter. A maximum peak to peak ripple as a fraction of the rated peak current for the design parameters is given by

$$\Delta I_{L_{max}} = k I_{max} \quad (3.7.)$$

Where k represents a desired ripple current factor and

$$I_{max} = \frac{S_n \sqrt{2}}{\sqrt{3} V_{ll}} \quad (3.8.)$$

The ripple attenuation is calculated using below formula which is derived later in chapter 3.3.1:

$$\frac{i_2(s)}{i_1(s)} = \frac{sC_f R_c + 1}{s^2 C_f (L_2 + L_g) + sC_f (R_2 + R_g + R_c) + 1} \quad (3.9.)$$

Ripple attenuation can be calculated for each specific harmonic by utilizing the formula above.

Antiresonant frequency is defined by the following:

$$f_{antires} = \frac{1}{2\pi} \sqrt{\frac{1}{L_1 C_f}} \quad (3.10.)$$

The resonant frequency is obtained by:

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \quad (3.11.)$$

Some additional design constraints may be imposed based on actual standards and application specifics. In the case of microgrid tie inverters LCL filters are designed to meet the

harmonic distortion limits according to IEEE1547-2018, which is a standard that provides a set of criteria and requirements for the interconnection of distributed generation resources into the power grid. The methodology for setting current distortion limits and for distortion measurement are adopted from IEEE-519-2014.

Table 3.1. (IEEE-519-2014. Table 2) defines current distortion limits at the PCC respectively.

Maximum harmonic current distortion in percent of I_L						
Individual harmonic order (odd harmonics)						
I_{sc}/I_L	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h < 50$	TDD
< 20	4.0	2.0	1.5	0.6	0.3	5.0
20 < 50	7.0	3.5	2.5	1.0	0.5	8.0
50 < 100	10.0	4.5	4.0	1.5	0.7	12.0
100 < 1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic levels listed						

Table 3. 1. Current distortion limits at the PCC per IEEE-519-2014

Where:

- Maximum demand load current I_L : This current value is established at the point of common coupling (PCC) and should be taken as the sum of the currents corresponding to the maximum demand during each of the twelve previous months divided by 12.
- Short-circuit ratio: At a particular location, the ratio of the available short-circuit current, in amperes, to the load current, in amperes.
- Total demand distortion (TDD): The ratio of the root mean square of the harmonic content, considering harmonic components up to the 50th order and specifically excluding inter-harmonics, expressed as a percent of the maximum demand current. Harmonic components of order greater than 50 may be included when necessary.

$$TDD = \frac{\sqrt{\sum_{h=2}^{50} I_h^2}}{I_L} 100\% \quad (3.12.)$$

However, IEEE1547, provides tables 26 (table 3.2) and 27 (table 3.3) which define current distortion limits a little differently than IEEE519.

Individual odd harmonic order h	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h < 50$	TRD
Percent (%)	4.0	2.0	1.5	0.6	0.3	5.0

Table 3. 2. Maximum odd harmonic Current distortion in percent of rated current (I_{rated})

Individual even harmonic order h	$h = 2$	$h = 4$	$h = 6$	$8 \leq h < 50$
Percent (%)	1.0	2.0	3	Associated range specified in Table 3.2

Table 3. 3. Maximum even harmonic Current distortion in percent of rated current (I_{rated})

IEEE1547 introduces new term “Total Rated-current Distortion (TRD)” is used instead of TDD. The total rated current distortion (TRD), which includes the harmonic distortion and inter-harmonic distortion, can be calculated using following:

$$TRD = \frac{\sqrt{I_{rms}^2 - I_L^2}}{I_{rated}} 100\% \quad (3.13.)$$

Where:

- I_L is the fundamental current as measured at the PCC
- I_{rated} is the units rated current capacity (transformed to the PCC when transformer exists between the unit and the PCC)
- I_{rms} is the root-mean-square of the current, inclusive of all frequency components, as measured at the PCC.

Also, based on table 3.3, even order current distortion limits in IEEE1547 above the second order are relaxed as compared to IEEE519. Finally, opposite to IEEE519, IEEE1547 is free of voltage distortion limits, since they are not defined in the standard.

In order to meet TRD requirements, TRD needs to be alternately defined by splitting the root mean square of current I_{rms} into high frequency I_{hf} and low frequency I_{lf} rms components such that:

$$TRD = \frac{\sqrt{I_{hf}^2 + I_{lf}^2}}{I_{rated}} 100\% \quad (3.14.)$$

Since high frequency current components represent a unique ripple current characteristic for each PWM modulation technique, they can be calculated using Table 4 in chapter 2.5.2 and ripple attenuation formula defined in (3.9.). Formulas in Table 4 define ripple current rms value for inductor L_1 , which if conservatively assumed to occur only at switching frequency f_{sw} , allows to calculate ripple attenuation at that frequency per (3.9.), and estimate I_{hf} at PCC. This way it is possible to estimate low frequency I_{lf} rms current component value limit, which actually represents STHD50 value:

$$STHD50 < \sqrt{\left(\frac{TRD}{100\%} I_{rated}\right)^2 - I_{hf}^2} \quad (3.15.)$$

Defined STHD50 limit provides information on maximum level of low order harmonics allowed to occur to meet IEEE1547 TRD requirement. These low order harmonics are dominantly induced by nonlinearities defined in chapter 2.5.3, filter resonance and PWM modulator itself.

As part of the detailed LCL filter design process for microgrid tie inverter, certain optimization criteria needs to be adopted. Typically, the most common LCL filter optimization criteria are minimum volume, weight and filter stored energy. However, each design has certain uniqueness based on the application specifics and ratings. This LCL filter design study provides

general guidelines and is not intended to address those specifics. Therefore, no optimization criteria will be imposed.

3.1.1. Calculation Example

The following calculation example is based on the parameters of 1 MVA rated microgrid tie inverter:

V_b [V]	S_b [KVA]	f_{sw} [Hz]	I_b [A]
430.00	1,000.00	4,140.00	1,491.86

Table 3. 4. Parameters of 1 MVA rated microgrid tie inverter

The base impedance, base inductance and base capacitance are calculated using (3.1.), (3.2.) and (3.3.) formulas as:

Z_b [Ohm]	L_b [H]	C_b [F]
0.16641	0.000441416	0.015940042

Table 3. 5. Base impedance, inductance and capacitance calculation

As per previous derivations, in order to calculate the minimum inverter dc bus voltage couple of assumptions need to be made:

- Inverter runs in the linear region, with maximum modulation index of 1, per (2.21.).
- Line conditions are the highest at 10% above the rating at 473V.

Total voltage drop across the filter at full reactive load in percent's is calculated as 11.27% based on the final filter parameters and equation (3.5.).

Minimum inverter dc bus voltage is calculated based on (3.6.) and rounded as:

$$V_{dc} = 750V$$

Rated peak current is calculated by (3.8.):

$$I_{max} = 1,918 A$$

A maximum peak to peak current ripple on the inductor L_1 is calculated as 35% of the rated current per (3.7.):

$$\Delta I_{L_{max}} = 671.3 A$$

Inductance L_1 is calculated based on (3.4.) as:

$L_1 [uH]$	$L_1 [%]$
44.977	10.189

Table 3. 6. Inductance L_1 calculation

In order to have a resulting current ripple value on the grid side, one assumption needs to be considered. Due to high attenuation rate of $-60db/dec$ at high frequencies, ripple current on the grid side of the filter can be approximated by a first harmonic of a triangle waveform at switching frequency, thus leading to reduction factor of $8/(\pi)^2$ as compared to triangle peak value. Therefore, the resulting ripple attenuation and grid side ripple current is calculated per (3.9.).

Ripple Attenuation	$I_{ripple} [A]$	$I_{ripple} [%]$
0.044	24.39	1.27

Table 3. 7. Ripple attenuation and grid side ripple current calculation

Ripple attenuation value was extracted from the filter parameter solution that satisfy IEEE 1547 harmonic limits, and will be covered in more details later.

Based on the desired ripple attenuation, an infinite number of combinations of Inductance L_2 and capacitance C_f can be selected. However, anti-resonance of the filter is the parameter that determines the value of the filter capacitance. Anti-resonant frequency, per (3.10.), is selected to target the 11th and 13th harmonic that naturally appear in the microgrid. Frequency of those harmonics is high enough that, depending on the designed bandwidth, it can cause difficulty for

the feedforward control to compensate. Anti-resonant frequency is set to 720Hz leading to capacitance C_f being calculated as:

C [mF]	C [%]
1.084	6.8

Table 3. 8. Capacitance C_f calculation

Therefore leading to inductance L_2 calculated as:

L_2 [uH]	L_2 [%]
9.711	2.2

Table 3. 9. Inductance L_2 calculation

Finally, the resonant frequency is calculated by (3.11.) as:

$$f_{res} [Hz] = 1,710.55$$

Also, some of the parasitic resistances need to be introduced into the circuit to represent individual component losses, therefore, inductors have series resistance values equal to $R_1, R_2 = 1\% X_1, X_2$ representing 1% of the reactance at line frequency, and capacitor equivalent series resistance is selected as 1m Ω .

As discussed previously, LCL filter design needs to comply with the current harmonic limits provided in tables 3.2 and 3.3 of IEEE 1547. In order to obtain magnitudes for each of the first 50 harmonics in output current waveform, model of an inverter filter and grid is used in open loop mode in order to evaluate current harmonics based on filtering of switched waveforms without any influence from current controller. It has been previously shown in Figure 2.32 that modulation index value m has a dominant effect on the values of low order harmonics in switched voltage waveform. Therefore, worst harmonic performance for any of the DDPWM waveforms is expected at lower modulation indexes. With the fixed DC bus voltage level, lowest modulation index is expected at low line voltage condition, selected as X percentage of V_b , with reactive power

flow import in direction from grid to inverter. Lowest modulation index under this condition can be calculated as

$$m = X * \left(1 - \frac{L_1(\%)}{100} - \frac{L_2(\%)}{100} * \left(1 - \frac{Cf(\%)}{100} \right) \right) \quad (3.16.)$$

For the LCL filter design example used here, lowest modulation index is calculated as 0.64 for X value selected at 90%. Since this is a zero power factor operating condition, looking at Figure 2.32, DDPWM produces highest harmonics. Also, in order to properly represent all low order harmonics, dead time and minimum pulse width limitations along with voltage drops and rise and fall times of the switches will be considered as well. Since IEEE 519 current harmonic limits are defined for $I_{sc}/I_l < 20$, 5% equivalent line impedance is added in between line and filter.

Based on parameters selected as the worst case scenario, high frequency rms component of current I_{hf} is calculated using table 2.4 in chapter 2.5.2 and ripple attenuation formula defined in (3.9.):

$$I_{hf} = 0.12I_{rated} * 0.044 = 0.00528I_{rated}$$

Based on calculated I_{hf} , low frequency I_{lf} rms current component value limit, represented in STHD50 value, is derived as:

$$STHD50 < 4.97\%$$

STHD50 limit value is very close to TRD level of 5%, which shows that overall harmonic limitations are almost independent from high frequency ripple current, and they mostly affect low order harmonics, dominantly induced by nonlinearities previously defined in chapter 2.5.3, filter resonance as well as DDPWM modulator.

Simulated current harmonic spectrum for first 50 harmonics is shown in Figure 3.1. IEEE 1547 harmonic limitations are not satisfied since 19th harmonic has a value of almost 20% of the

rated current, which is a consequence of filter resonance occurring at 1118 Hz with 5% line impedance. Therefore, in order to dampen the resonance effect, damping resistor of $R_c = 0.1\Omega$ in series with filter capacitors will be temporarily considered for the analysis purpose only, and other means of dampening will be introduced later in the work.

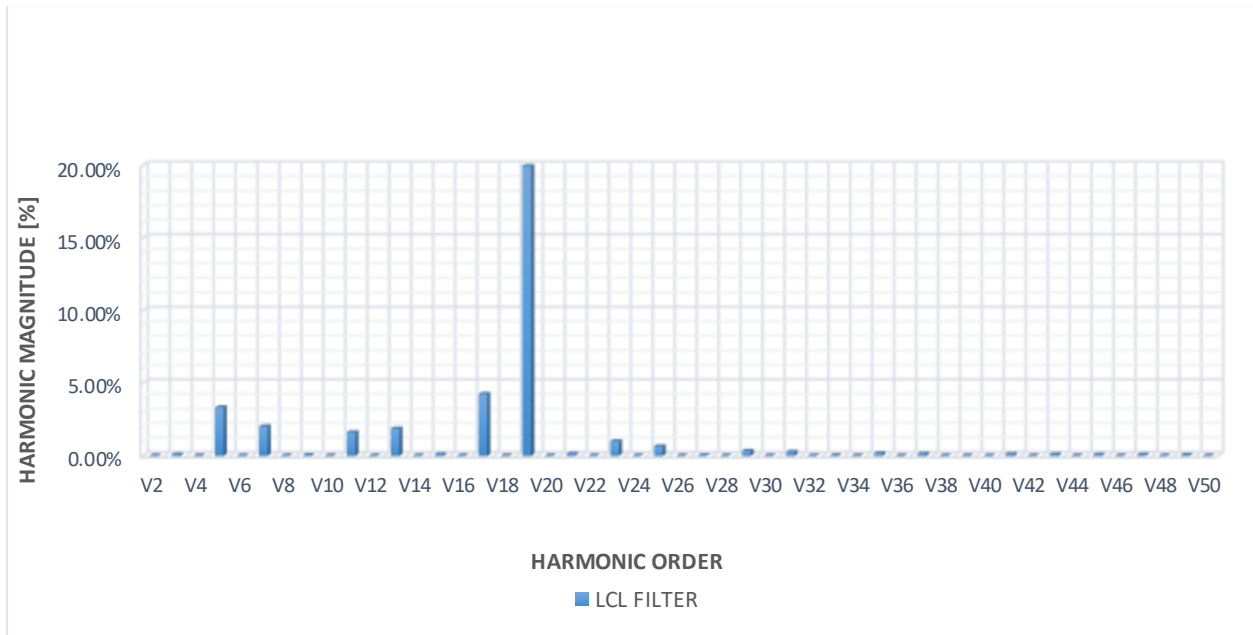


Figure 3. 1. Low Order Current Harmonic Spectra for LCL filter with $R_c = 1m\Omega$

Current harmonic spectrum for first 50 harmonics for $R_c = 0.1\Omega$ is shown in Figure 3.2. Along with it is the harmonic spectrum for the case where capacitors are completely removed from the circuit and filter consists of inductance L only, equal to summation of L_1 and L_2 . Both filter solutions meet individual harmonic limits defined in Tables 3.2 and 3.3. Based on results in Figure 3.2., it is clear that lower order harmonics within the first 50 harmonics are dominant in both solutions, with LCL filter solution having higher overall magnitudes.

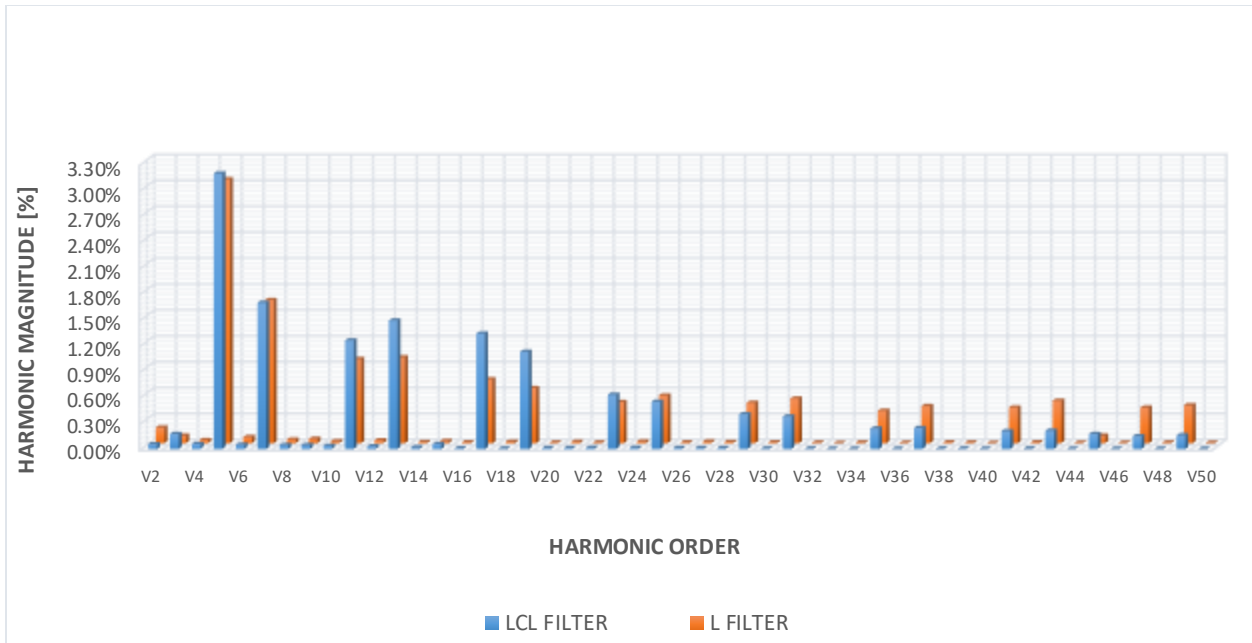


Figure 3. 2. Low Order Current Harmonic Spectra Comparison between LCL filter with $R_c=100\text{ m}\Omega$ and L filter only

Figure 3.3. compares LCL and L filter solution in terms of TRD, which has a limit of 5% defined in IEEE 1547. Comparison of TRD along with the STHD for first 10, 15, 20, 30, 40 and 50 harmonics for LCL and L filter solution is shown in Figure 3.3. Despite lower values of STHD for first 50 harmonics, L filter solution does not satisfy TRD limitation of 5%.

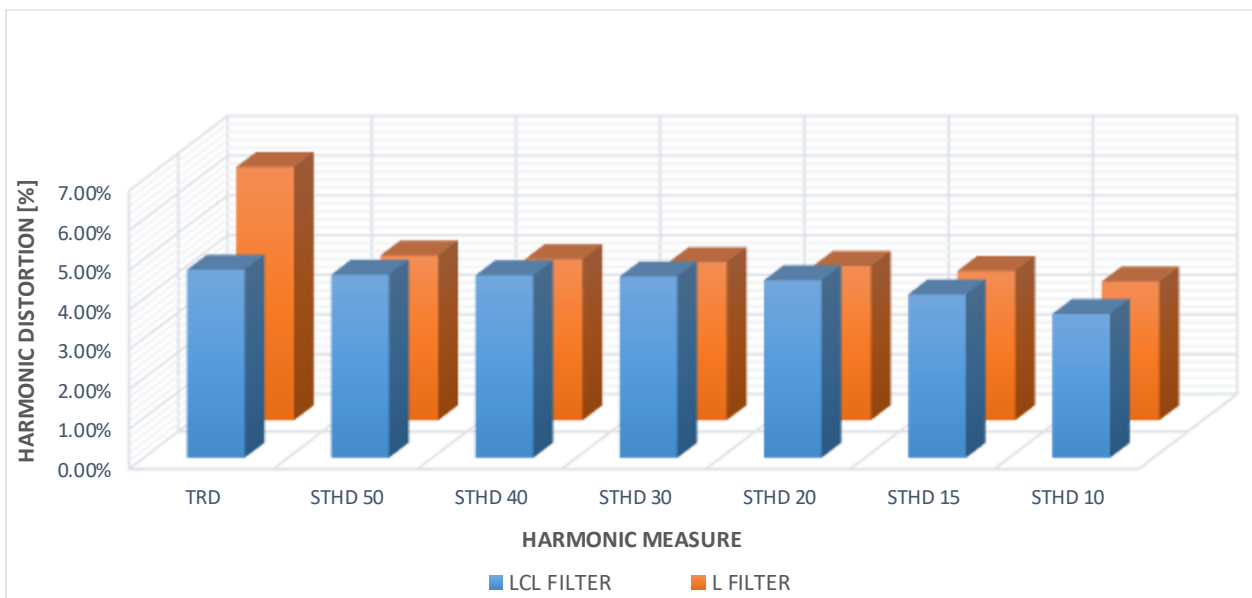


Figure 3. 3. TRD and STHD10/15/20/30/40/50 Comparison between LCL filter with $R_c=100\text{m}\Omega$ and L filter only

In order to explain this better, frequency characteristics of LCL filter solution with $R_c = 1m\Omega$ and $R_c = 100m\Omega$ along with L filter solution are shown in Figure 3.4. Increase of damping resistor value to $R_c = 100m\Omega$ has dampened the resonant peak of LCL filter, but has decreased filtering performance in the high frequency range. L solution shows slightly higher attenuation rates than dampened LCL filter solution in the frequency range between $200Hz$ and $2.2 KHz$, thus leading to better $STHD$ performance in low frequency range. However, due to lower attenuation rates in the higher frequency range above $2.2 kHz$, resulting in higher ripple current related harmonics, L filter cannot meet TRD requirements.

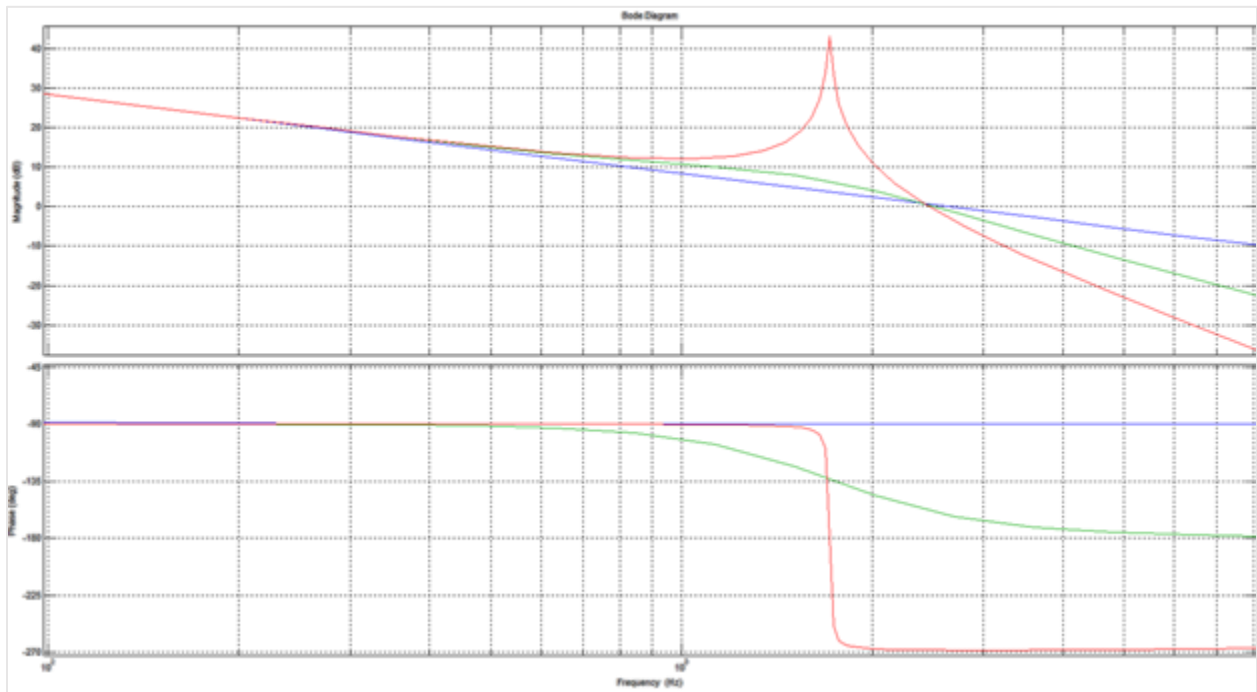


Figure 3. 4. Frequency Characteristic Comparison between L filter and LCL filter with $R_c=1m\Omega$ and $R_c=100m\Omega$ (missing label)

In order to reflect high frequency performance, first set of sideband current harmonics around carrier frequency are computed and compared between L and LCL solution in Figure 3.5. Higher high frequency current harmonic levels in L filter are due to lower attenuation rate for frequency range above resonance.

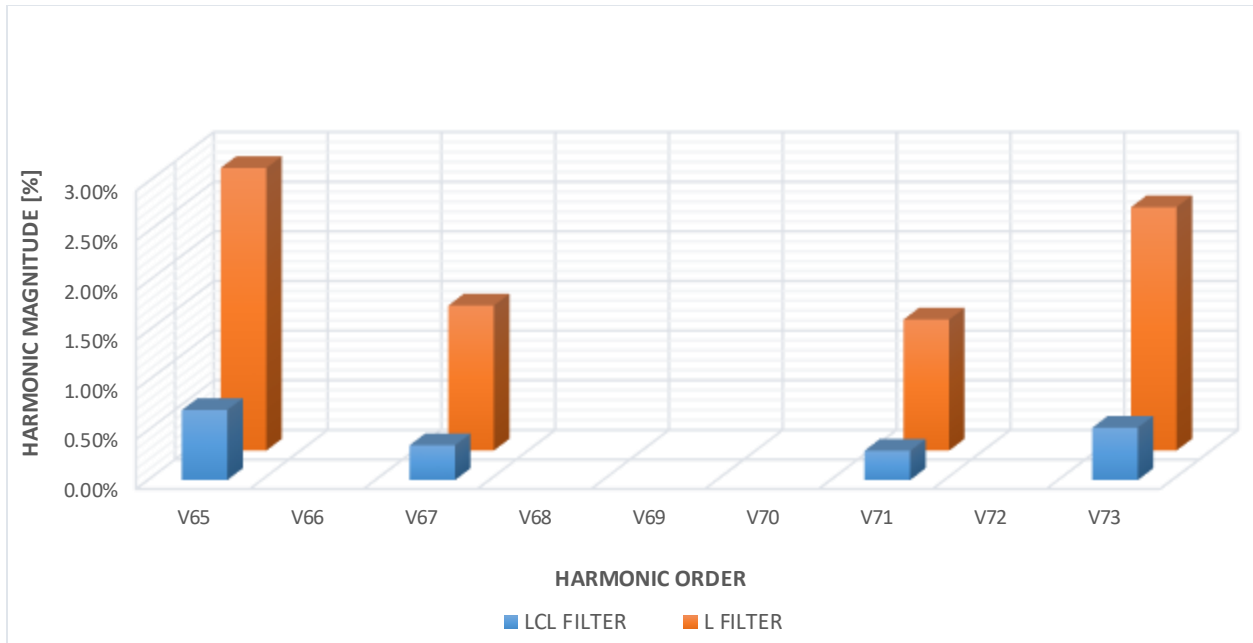


Figure 3. 5. First Sideband Harmonics Comparison between L filter and LCL filter

Therefore, using L filter for MTI is not a viable solution, since inductance values need to be significantly increased in order to meet the TRD requirements and that would have a major impact on the power structure ratings and control performance of the MTI.

3.1.2. Comparison between MTI and GTI Filter design

As discussed previously, numerous studies dedicated to design aspects of the LCL filter under unity power factor operation of the inverter exist. A comparative design of a grid tie inverter filter that meets IEEE 519 limits, that is designed for unity power factor operation using DPWM1 technique, and is within similar voltage, power and switching frequency ratings as MTI filter design example is presented in [10]. The parameter comparison between state of the art filter designed for unity power factor operation called Grid Tie Inverter (GTI) and microgrid tie inverter (MTI) is shown bellow in table 3.10:

Inverter Type	V_{ac} [V]	V_{dc} [V]	L_1 [%]	C [%]	$L2$ [%]	f_{res} [Hz]	$f_{antires}$ [Hz]
MTI	480	750	9	5	3	1788	892
GTI	430	750	10.19	6.8	2.2	1710	720

Table 3. 10. Comparison between GTI and MTI filter design

As explained previously, total voltage drop across the filter at full reactive load had induced a necessity for lowering AC voltage rating in order to keep DC bus voltage within the standard rating. Also, reactive power import condition requires operation at lower modulation index values that leads to higher voltage harmonic generation. That results in slight increase in total filter inductance and increase in total filter capacitance for the microgrid tie inverter, as compared to state of the art grid tie inverter design, in order to meet IEEE 1547 limitations.

As part of the frequency analysis further bellow, filter can be divided into low and high frequency range. Within the low frequency range, where all the 50 harmonics defined in Table 3.1 fall within, inductances have a major influence. Within the high frequency range, capacitance starts having a major influence.

A comparison of performance between the microgrid tie and standard grid tie filter design is shown in figure 3.6. and figure 3.7. Transfer function $G_i(s)$, defined thru (3.29.), is shown in the bode plot in figure 3.6. A higher attenuation across the full frequency range is noticeable in case of microgrid tie inverter filter, which is a consequence of the previously described necessity for reactive power support operation under lower modulation index values. As per previous calculations, resonance frequency is obviously lower in case of a MTI.

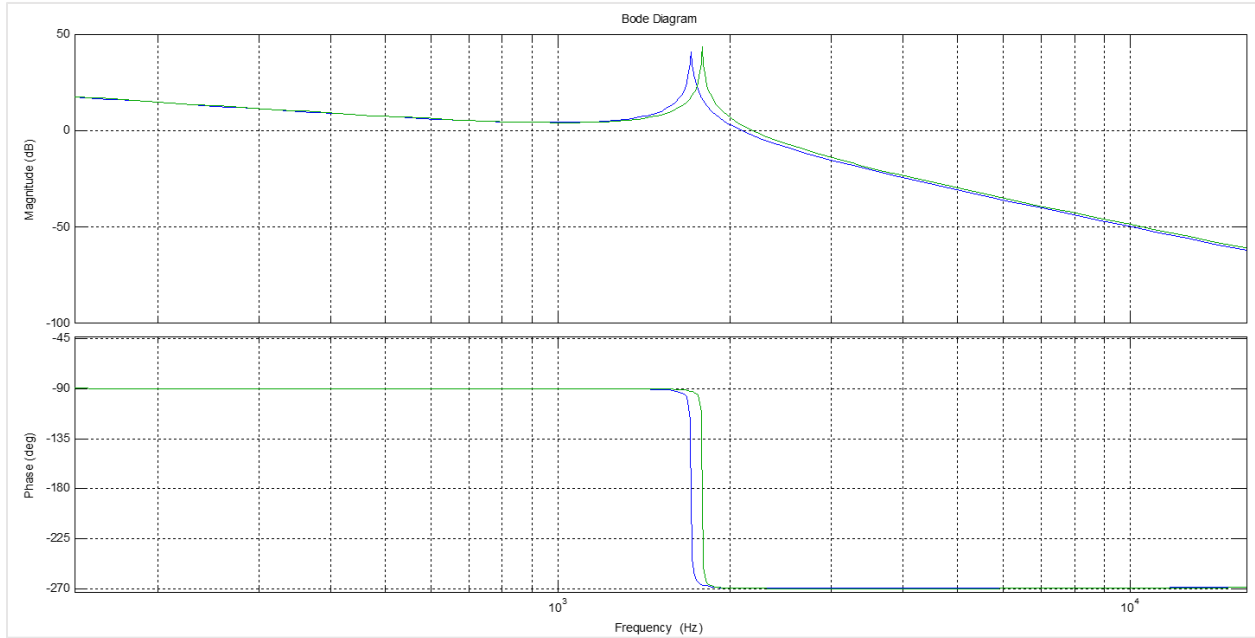


Figure 3. 6. A comparison of $G_i(s)$ between the microgrid tie and standard grid tie filter (blue MTI, green GTI)

Transfer function $G_g(s)$, defined thru (3.32.), is shown in the bodeplot in figure 3.7. Based on the literature review, the anti- resonant frequency is not considered as a design target for state of the art grid tie inverter filter, and clear guideline on how to select it does not exist. Therefore, there is an obvious difference between the two designs in terms of anti-resonant frequency. A higher attenuation across the low frequency range is noticeable in case of MTI filter. Also, a lower attenuation across the high frequency range is noticeable in case of MTI filter.

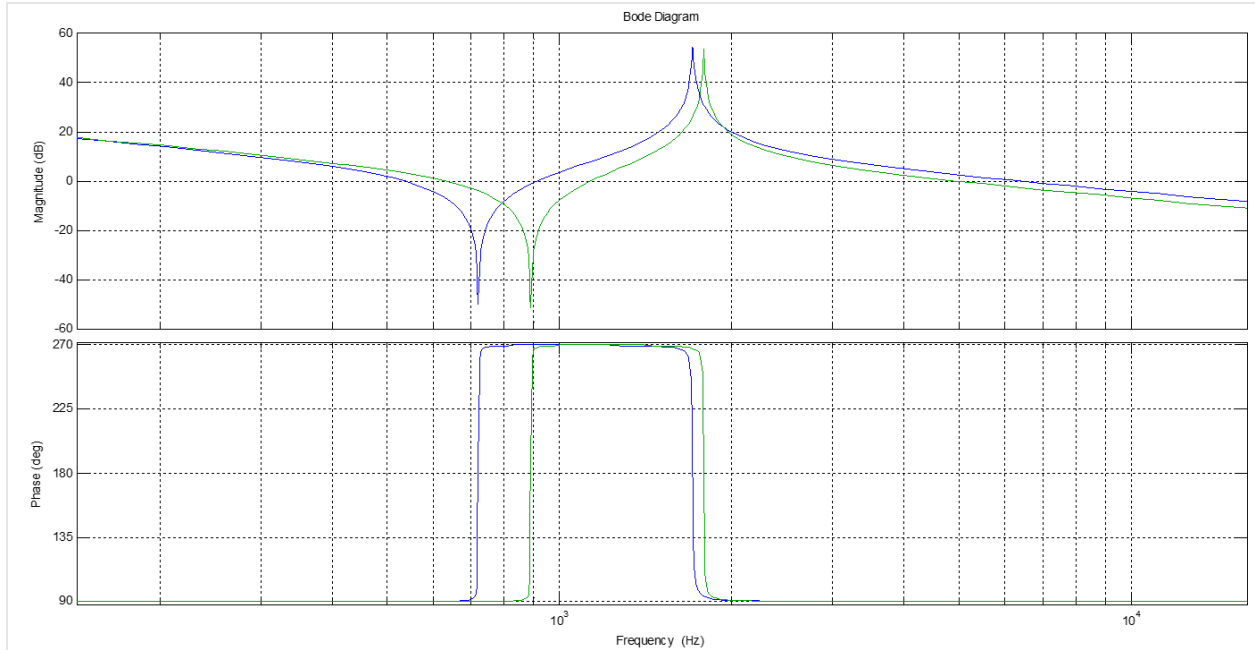


Figure 3. 7. A comparison of $G_g(s)$ between the microgrid tie and standard grid tie filter

3.1.3. Influence of main Filter Parameters

In order to provide the ability to properly optimize MTI, it is important to fully analyze the effect that variation of main filter parameters C_f , L_1 and L_2 have on the filter performance. Figures 3.8-3.13 show the family of curves for the bode plot of transfer functions $G_i(s)$ and $G_g(s)$ for variation of main filter parameters C_f , L_1 and L_2 correspondingly. Filter parameters used for the analysis have been derived in chapter 3.1.1.

Figures 3.8 and 3.9 correspond to the filter capacitance variation between 1% and 10% with 1% increments. Regarding $G_i(s)$ in Figure 3.8., It is noticeable that for low frequency range filter attenuation rate does not get influenced, and has an almost constant attenuation rate of $-20dB/dec$. Resonance frequency significantly drops with the capacitance increase, but the

resonance magnitude does not get affected. High frequency range has a constant attenuation rate of $-60\text{dB}/\text{dec}$ regardless of the capacitance value. However, the resonance frequency determines the point where high attenuation starts, thus leading to significantly higher attenuation for a specific frequency value.

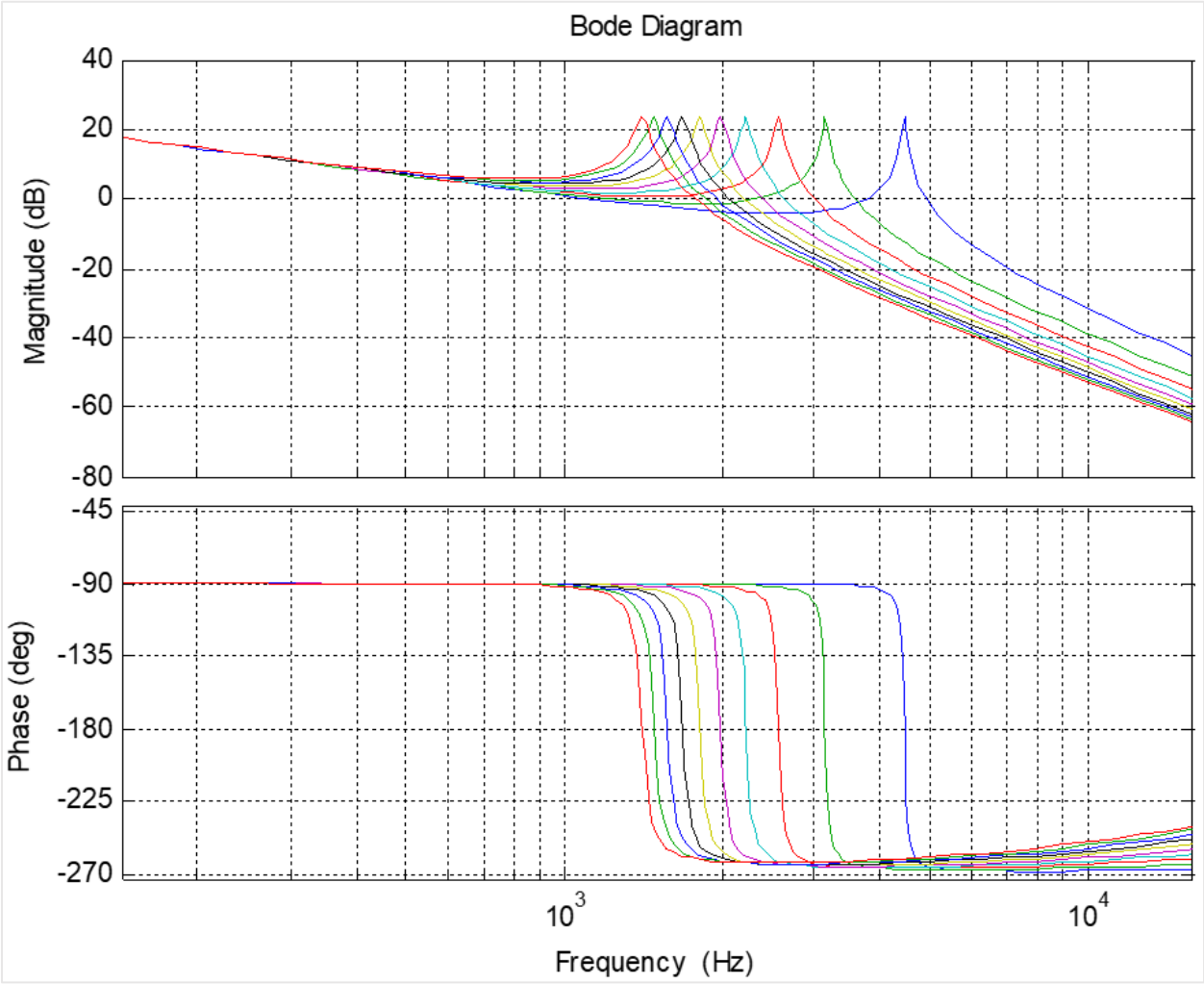


Figure 3. 8. Bode plot of transfer function $G_i(s)$ for capacitance C_f variation

For $G_g(s)$ in Figure 3.9., it is noticeable that neither the low frequency, nor the high frequency range attenuation gets influenced, and has an almost constant attenuation rate of $-20dB/dec$. Both resonant and antiresonant frequency significantly drop with the capacitance increase. However, in resonant case magnitude does not get affected, but in the case of anti resonance a certain level of damping can be observed with the increase in filter capacitance.

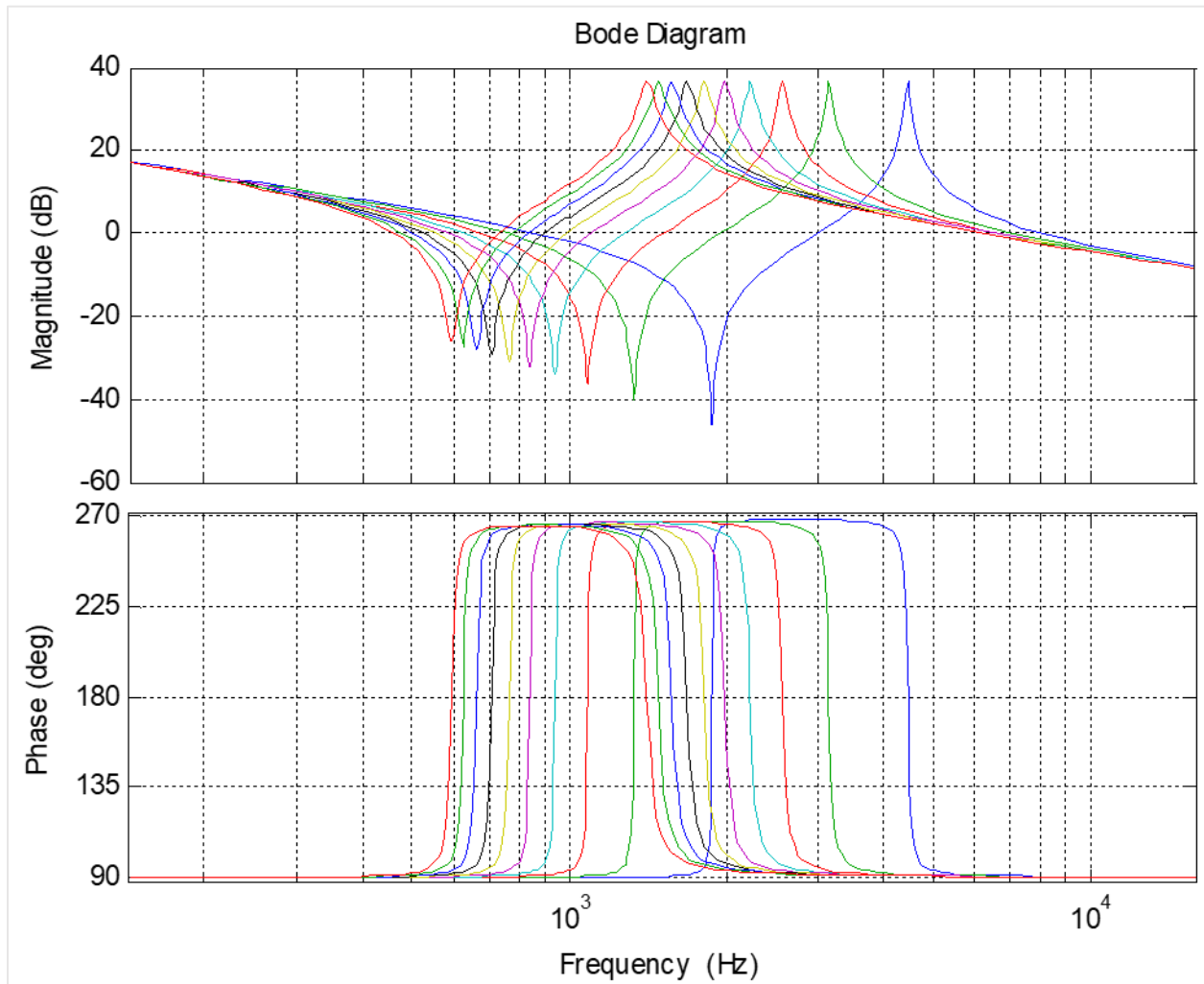


Figure 3. 9. Bode plot of transfer function $G_g(s)$ for capacitance C_f variation

Figures 3.10. and 3.11. correspond to the filter inductance L_1 variation between 5% and 15% with 1% increments. For $G_i(s)$ in Figure 3.10., both low frequency and high frequency range

filter attenuation gets affected in the same manner. Curves are linearly shifted in both ranges, with higher inductance leading to higher attenuation. Attenuation rate in low frequency and high frequency range is constant at -20dB/dec and -60dB/dec respectively. Both resonance frequency and magnitude drops with the inductance increase.

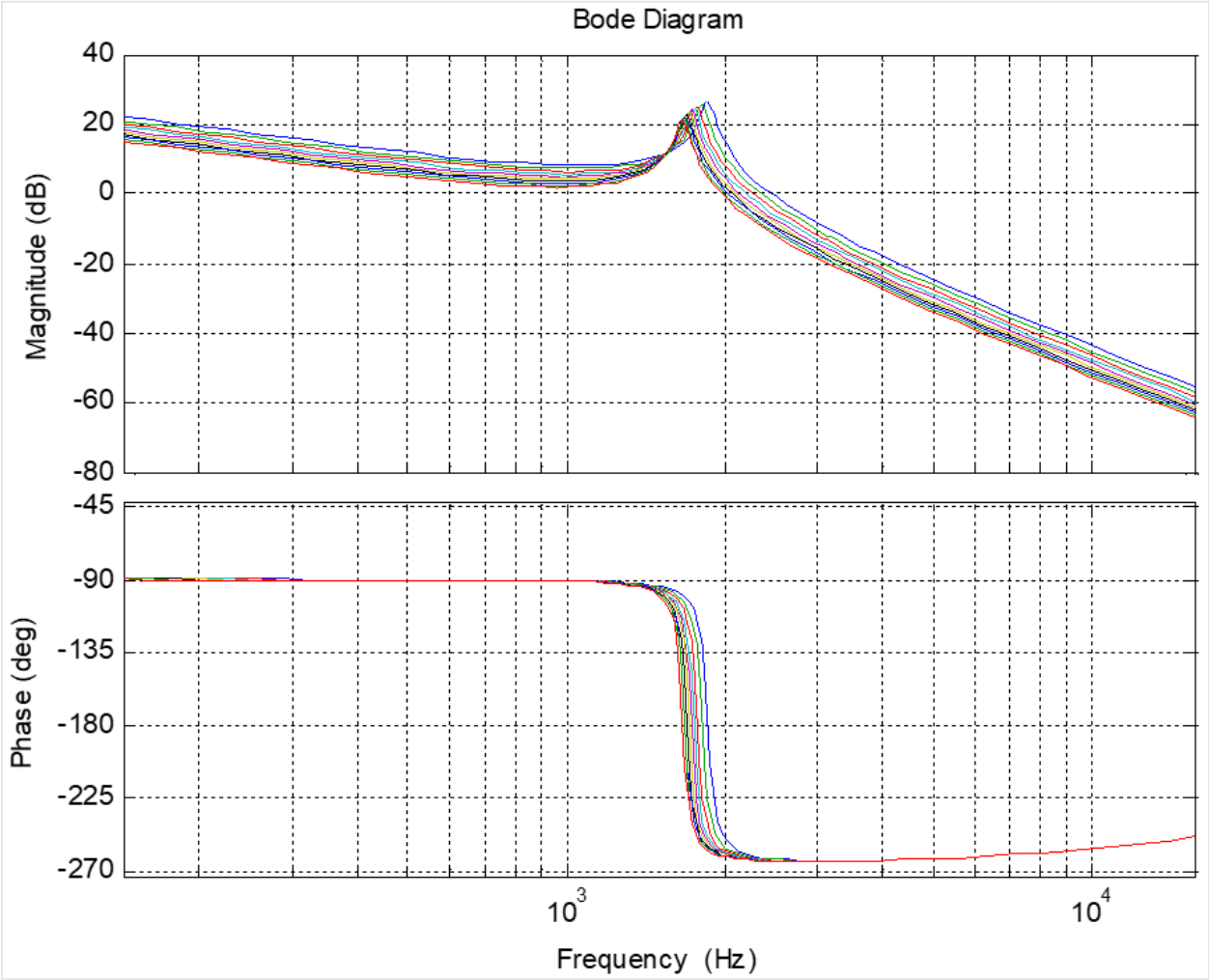


Figure 3. 10. Bode plot of transfer function $G_i(s)$ for filter inductance L_1 variation

Regarding $G_o(s)$ in Figure 3.11., the low frequency range attenuation gets influenced with the higher inductance leading to higher attenuation. Both resonant and antiresonant frequency

decrease with the rise in inductance. As opposed to capacitor variation case in figure 3.9., Figure 3.11. shows the antiresonant peak value being lower, leading to higher attenuation.

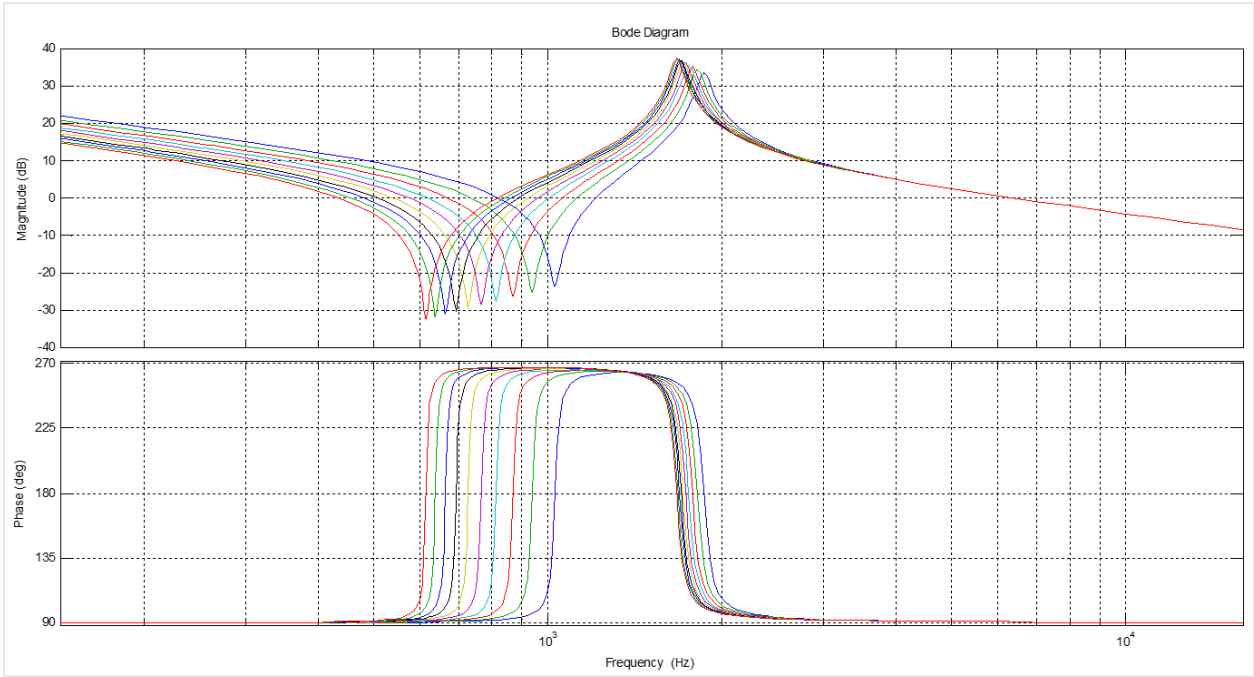


Figure 3. 11. Bode plot of transfer function $G_g(s)$ for filter inductance L_1 variation

Figures 3.12. and 3.13. correspond to the filter inductance L_2 variation between 1% and 10% with 1% increments. For $G_i(s)$ in Figure 3.12., both in low frequency and high frequency range higher inductance leads to higher attenuation. Resonance frequency drops with the inductance increase.

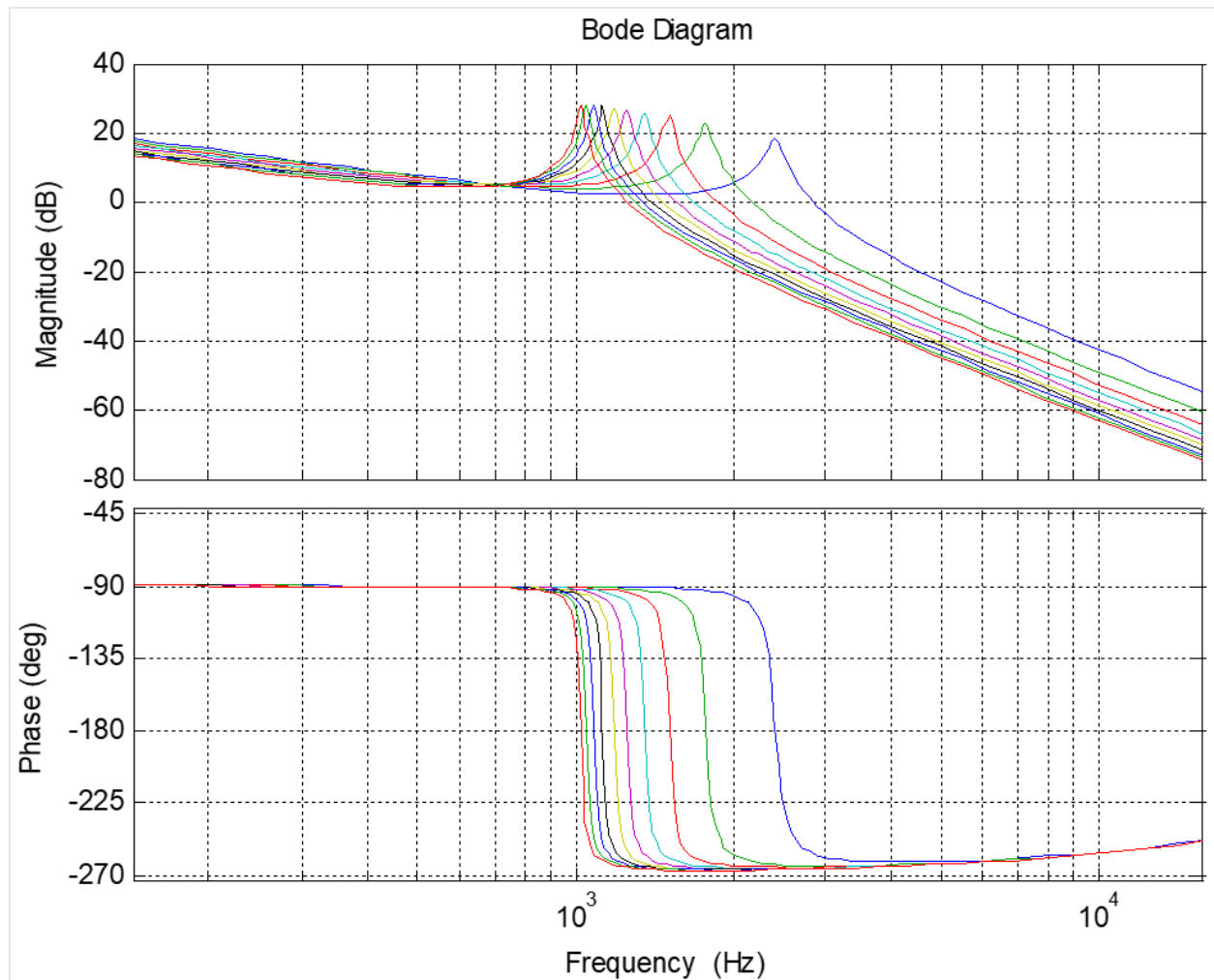


Figure 3. 12. Bode plot of transfer function $G_i(s)$ for filter inductance L_2 variation

Regarding $G_g(s)$ in Figure 3.13., both the low frequency and high frequency range attenuation gets influenced with the higher inductance L_2 leading to higher attenuation. Also increase in L_2 leads to higher resonance damping, and does not have the effect on antiresonant frequency.

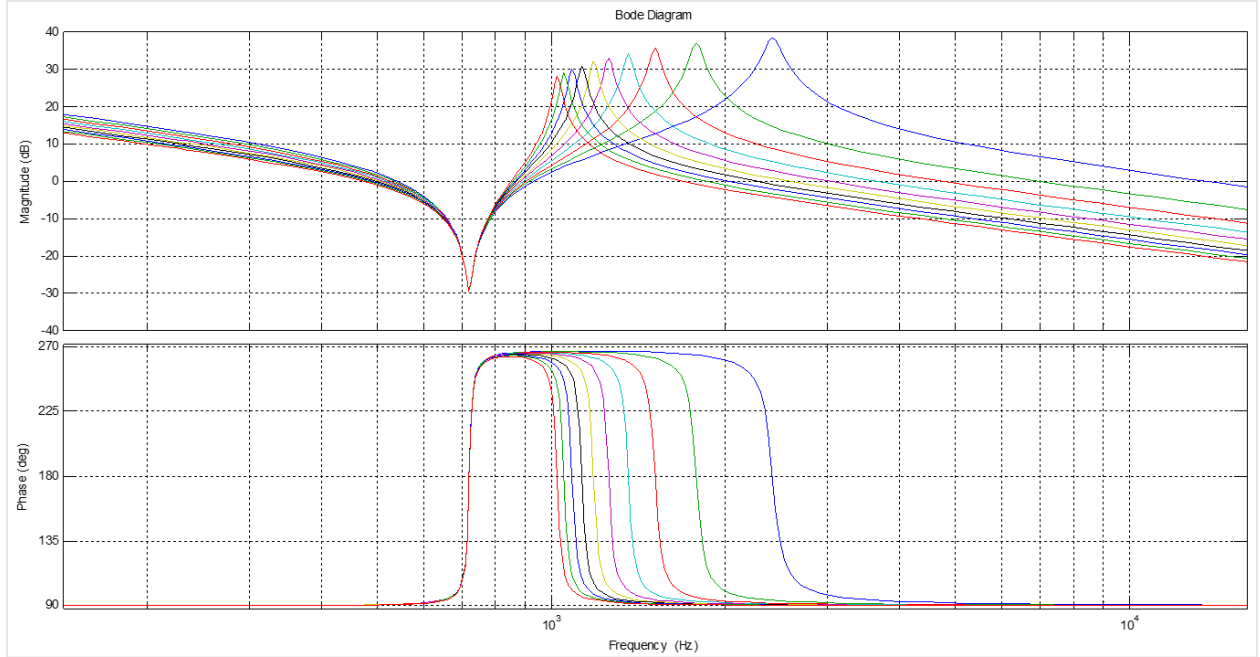


Figure 3. 13. Bode plot of transfer function $G_g(s)$ for filter inductance L_2 variation

3.1.4. Influence of Parasitic Filter Parameters

In order to address some of the unique phenomena occurring in MTI, it is important to fully analyze the effect that variation of parasitic filter parameters R_1 , R_2 and R_f have on the filter performance. These parameters are named parasitic, due to the fact that they are naturally present in the filter, but are often not considered in the filter design as one of the targeted design parameters, mostly due to low impact on filter performance.

Figures 3.14. – 3.19. show the family of curves for the bode plot of transfer functions $G_i(s)$ and $G_g(s)$ for variation of main filter parameters R_1 , R_2 and R_f correspondingly, with same initial values as per chapter 3.1.1.

R_1 represents an equivalent series resistance on the inverter side that produces the amount of losses equivalent to all the losses on the input side. Input losses are primarily the inductor

winding and core losses and wiring losses. In standard design, R_1 should represent only a small fraction of the L_1 inductor impedance. Figures 3.14. and 3.15. correspond to the input series resistance variation between 1% and 10% with 1% increments. There is very little effect of the R_1 on the overall filter performance, except the reduction of the attenuation at antiresonant frequency, which is undesirable. Due to that fact, and the overall requirement for loss reduction and increased efficiency, it is highly recommended to minimize R_1 parameter as part of the design.

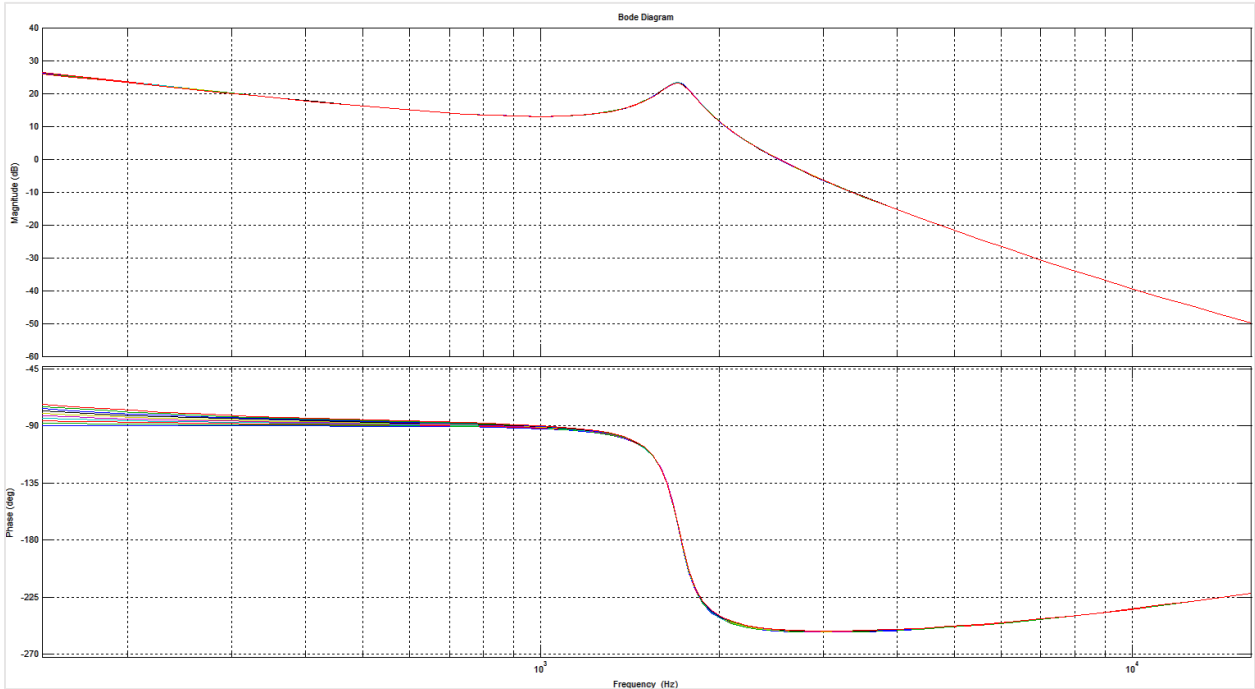


Figure 3. 14. Bode plot of transfer function $G_I(s)$ for input resistance R_1 variation

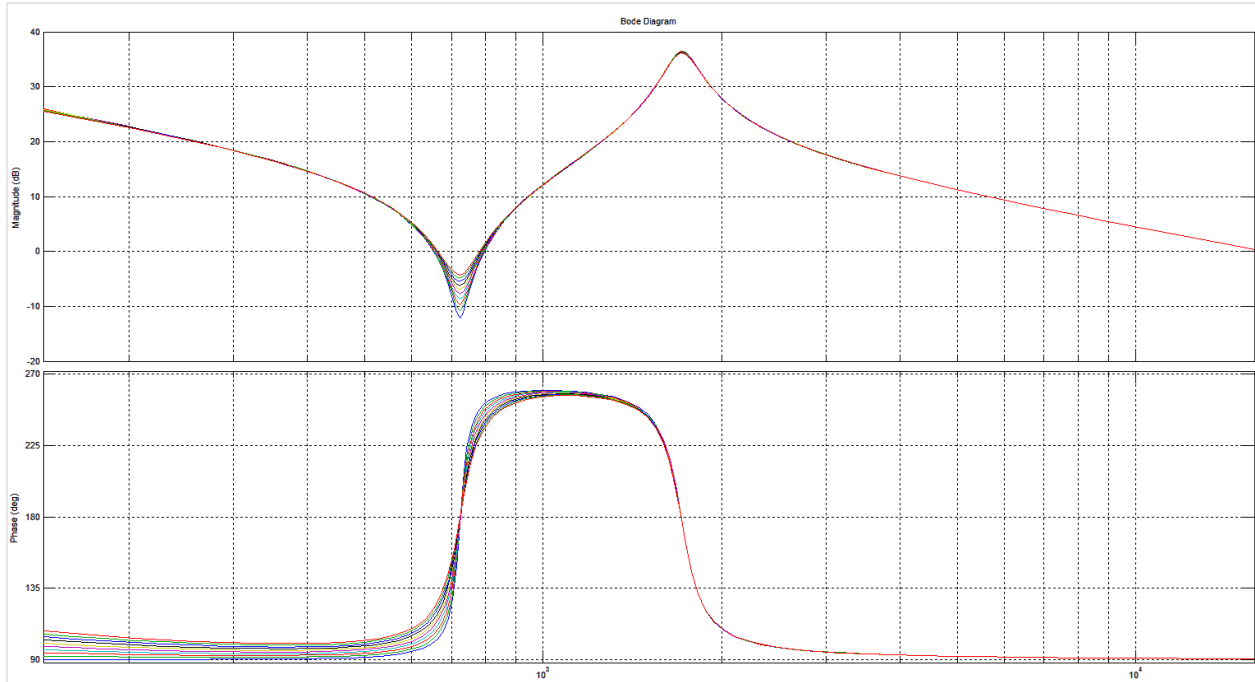


Figure 3. 15. Bode plot of transfer function $G_g(s)$ for input resistance R_1 variation

R_2 represents an equivalent series resistance on the grid side that produces the amount of losses equivalent to all the losses on the output side. Output losses are primarily the inductor or isolation transformer winding and core losses and wiring losses. Equivalent resistance on the microgrid side can vary dramatically, depending on the microgrid structure. This will be analyzed separately in chapter 3.3.1.2, and will not be considered here. In standard design, R_2 should represent only a small fraction of the L_2 inductor impedance. Figures 3.16. and 3.17. correspond to the input series resistance variation between 1% and 10% with 1% increments. Similar to previous R_1 case analysis, there is very little effect of the R_2 on the overall filter performance, with positive effect of resonance damping. However, the total equivalent resistance required to provide sufficient damping effect has to be significantly larger than L_2 impedance in per unit value. That would cause excessive losses, heat dissipation problems and decreased efficiency and

therefore, similar to R_1 case, it is highly recommended to minimize R_2 parameter as part of the design.

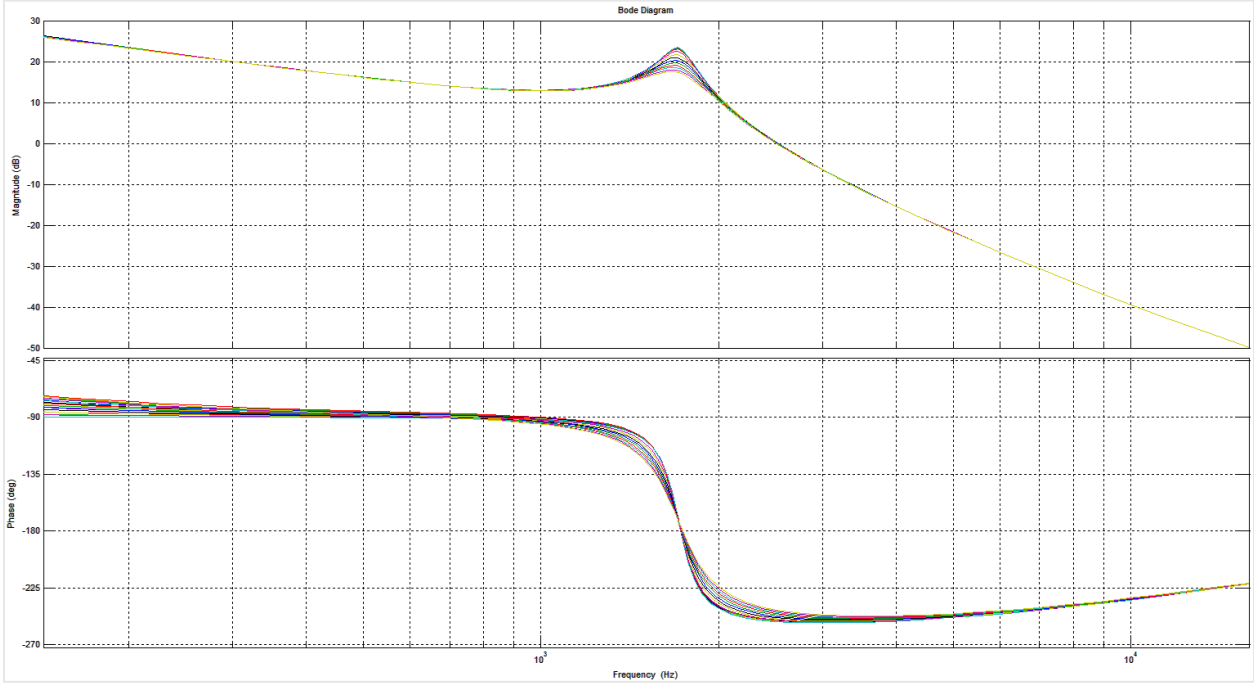


Figure 3. 16. Bode plot of transfer function $G_i(s)$ for output resistance R_2 variation

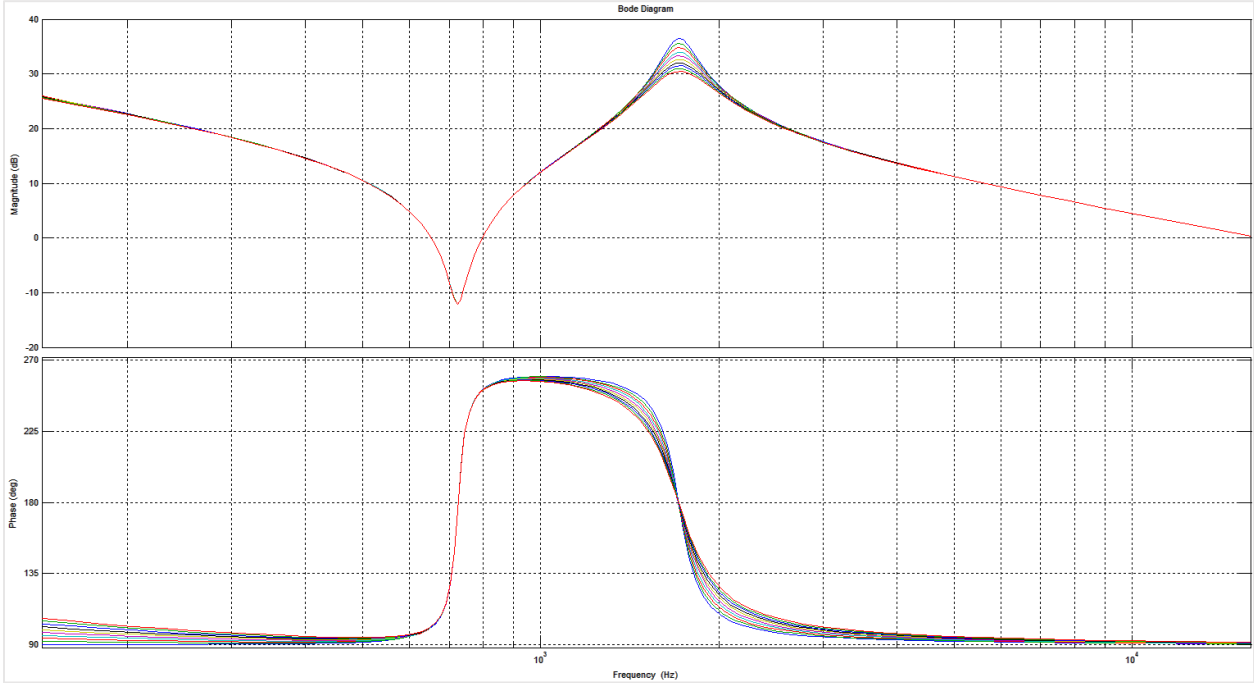


Figure 3. 17. Bode plot of transfer function $G_g(s)$ for output resistance R_2 variation

R_c represents an equivalent series resistance of the filter capacitor branch which is typically a summation of the capacitor equivalent series resistance and wiring resistance. A typical GTI will most often have an added damping resistor in series with the filter capacitors, which will increase the value of designed R_c . However, this will not be part of the current analysis, and will be addressed in chapter 4.6.1. Figures 3.18. and 3.19. correspond to the capacitor branch series resistance variation between 0% and 10% with 1% increments. R_c has almost no effect on the overall filter performance, except for the dampening effects at resonance and antiresonance frequencies. As per Figure 3.18. and 3.19., very little additional resistance in the capacitor branch makes a huge difference on the resonance damping. Also, the amount of current flowing thru the capacitor branch is at least order of magnitude lower than thru the main inductor L_1 . These two factors ensure low losses in capacitor branch and make series resistor a solution of choice for passive resonance damping in LCL filters.

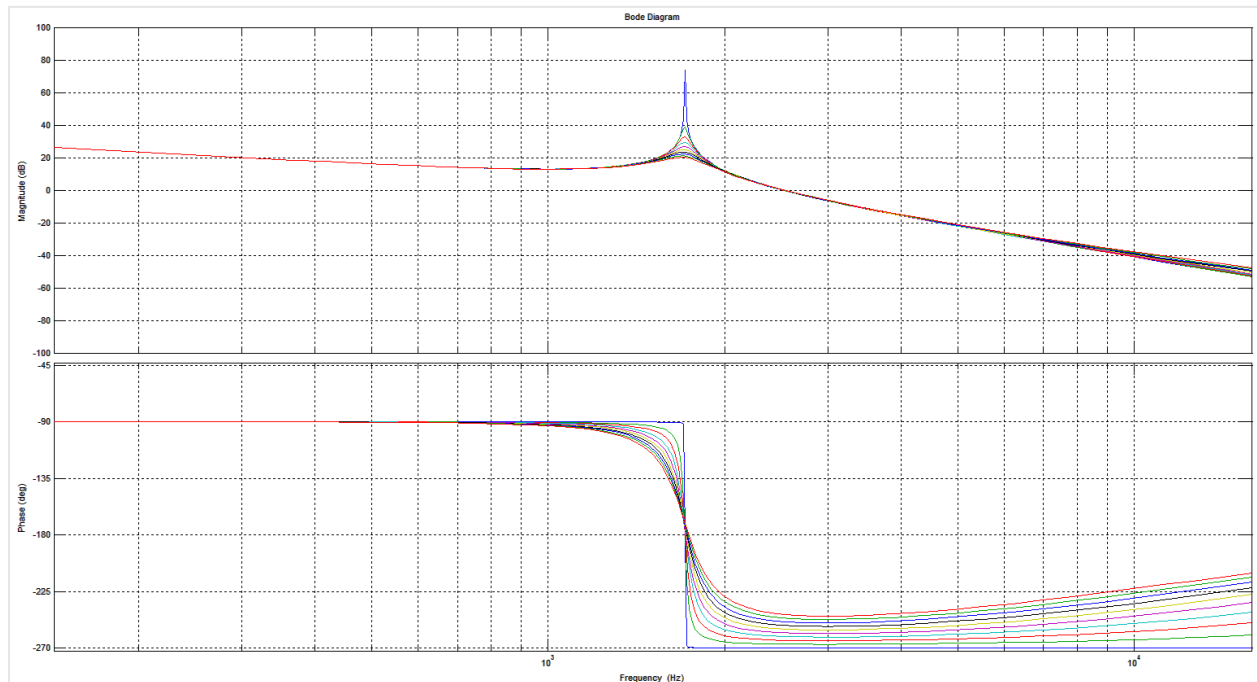


Figure 3. 18. Bode plot of transfer function $G_i(s)$ for capacitor resistance R_c variation

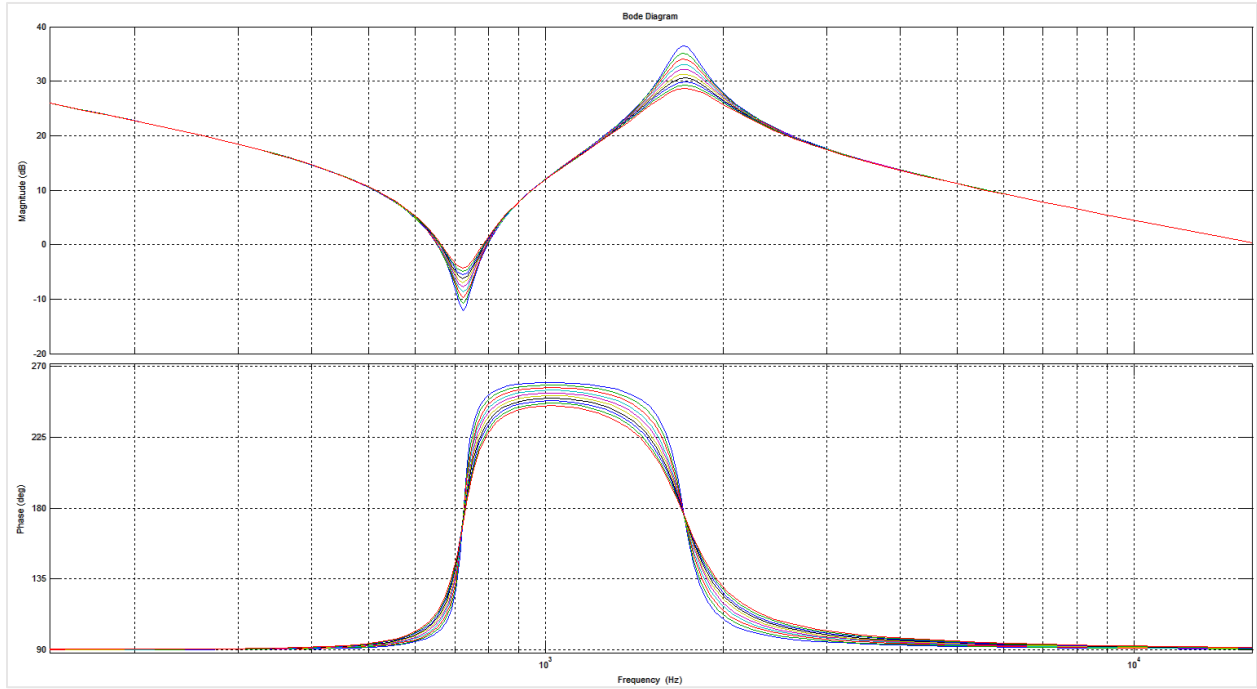


Figure 3. 19. Bode plot of transfer function $G_g(s)$ for capacitor resistance R_c variation

3.2. Impedance and Circuit Based Analysis

3.2.1. Filter Input and Output Impedance

Operating requirement for MTI is to be able to provide varying active and reactive power support, which reflects into varying apparent power requirement at varying power factors. At rated voltage condition that translates into varying fundamental current amplitude and power factor requirement at the PCC. The simplest way to analyze effect of varying active and reactive power requirements on MTI operation is by using an equivalent impedance model by calculation of the converter side Z_{conv} equivalent load impedance based on the microgrid side equivalent load impedance Z_{grid} at fundamental frequency f_n . Single phase representation without any parasitic elements is adopted. By assuming rated voltage condition, equivalent microgrid side load impedance Z_{grid} will vary both in terms of magnitude and angle. This impedance in combination with filter parameters will dictate input converter impedance value Z_{conv} . Since microgrid voltage is sensed and the microgrid current is controlled by the inverter on the microgrid side, Figure 3.20. shows the equivalent circuit for calculation of the Z_{conv} and Z_{grid} .

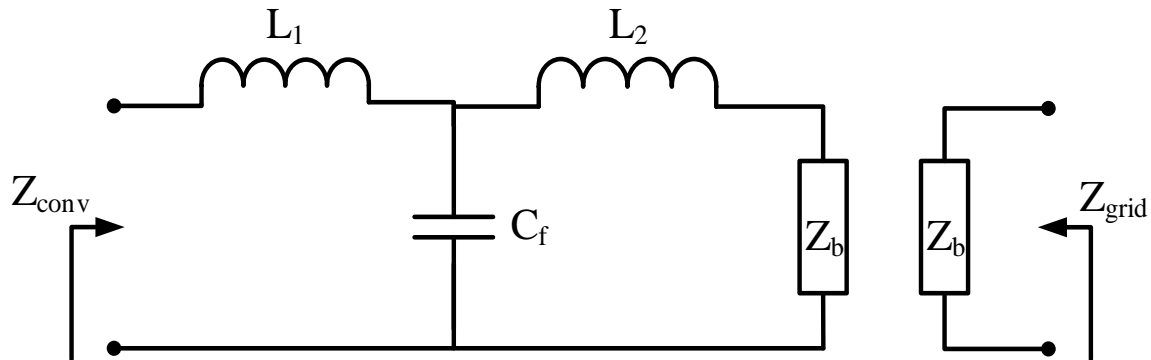


Figure 3. 20. Equivalent circuit for a current controlled MTI with voltage and current sensed on the MTI side

Based on Figure 3.20. the following equations can be derived:

$$Z_{grid} = Z_b = R_b + jX_b \quad (3.17.)$$

$$Z_{conv}$$

$$= \frac{R_b X_c + j[(X_c X_2 - X_1 X_2 + X_1 X_c)(X_c - X_2 - 2X_b) + X_b X_c^2 + (R_b^2 + X_b^2)(X_1 - X_c)]}{R_b^2 + (X_b - X_2 - X_c)^2} \quad (3.18.)$$

When using previously calculated LCL filter design parameters in chapter 3.1.1, figure 3.21. shows the magnitude ratio between Z_{conv} and Z_{grid} in respect to Z_{grid} phase angle. Z_{grid} angle represents a load angle in a sense, since it's variation dictates output power factor variation.

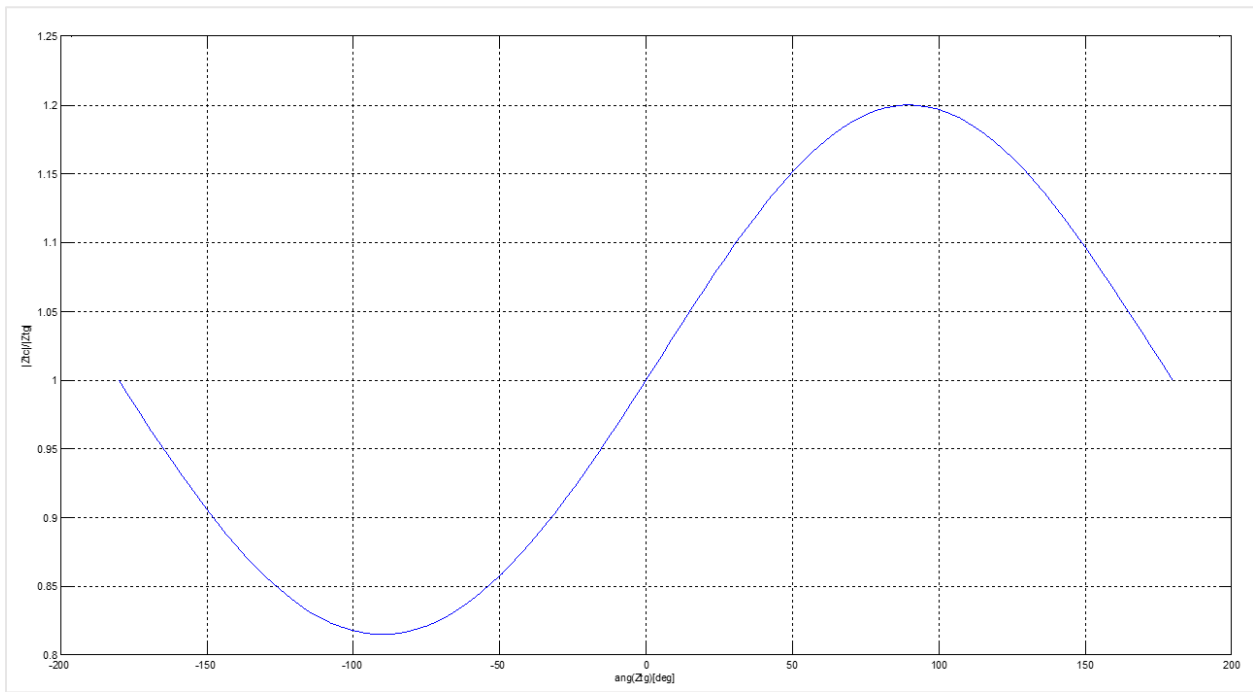


Figure 3. 21. Z_{conv}/Z_{grid} ratio dependency to Z_{grid} phase angle.

It is important to notice that while the impedance magnitudes of Z_{conv} and Z_{grid} are almost matching at active power conditions (-180° and 0°), it is not the case with reactive power ($\mp 90^\circ$). At pure reactive power import condition, Z_{grid} is represented as equivalent capacitor and

equivalent input converter impedance Z_{conv} significantly drops in magnitude. On the other hand, under pure reactive power injection condition, Z_{grid} is represented as equivalent inductor and equivalent input converter impedance Z_{conv} significantly drops in magnitude.

For a same set of precalculated set of LCL filter parameters, figure 3.22. shows the angle difference between Z_{conv} and Z_{grid} in respect to Z_{grid} angle.

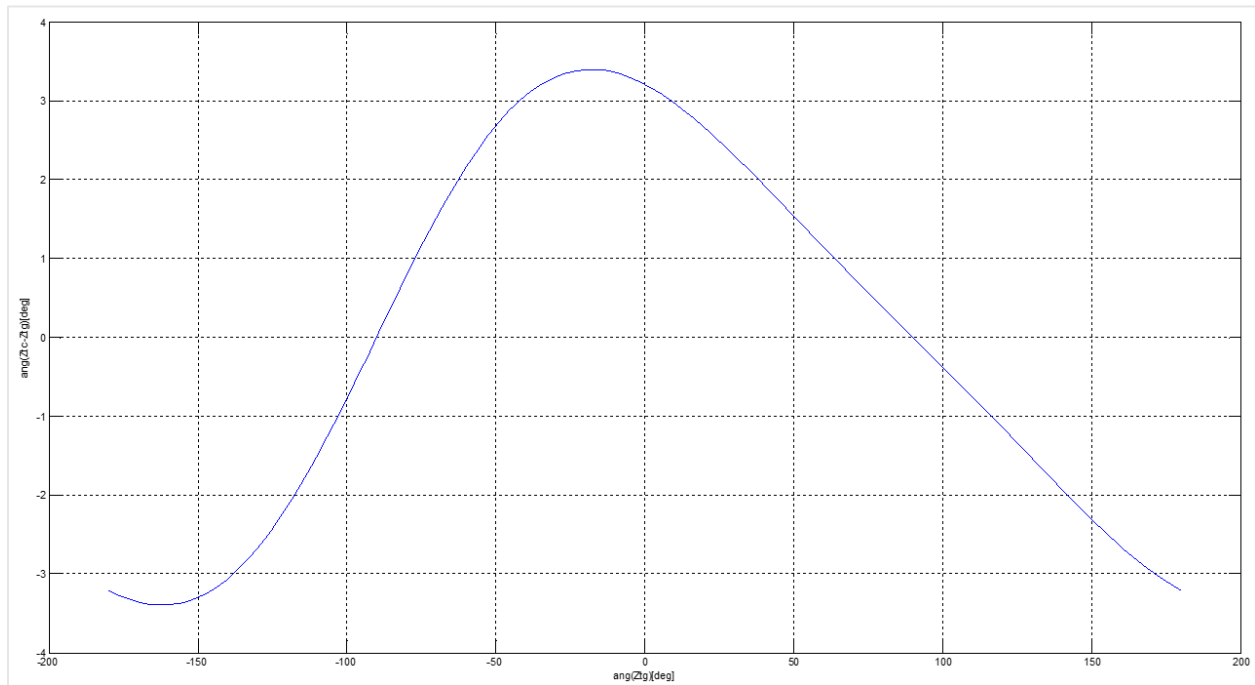


Figure 3. 22. Phase Angle difference ($Z_{conv} - Z_{grid}$) dependency to Z_{grid} phase angle.

As per figure 3.22., angle difference between Z_{conv} and Z_{grid} is either positive or negative at active power conditions (-180° and 0°), depending on the sign of the impedance, which represents power flow direction. At reactive power flow condition ($\mp 90^\circ$), angle difference is close to zero value.

Microgrid side and converter side equivalent impedances Z_{grid} and Z_{conv} provide a simple set of parameters for qualitative analysis of the operating conditions on the converter side. However, due to a shunt capacitance present in the filter design, converter side and microgrid side

currents and voltages cannot be fully analyzed using an impedance model, thus providing a limitation in case of using equivalent impedance comparison. That leads to using actual circuit analysis as a proper tool for quantitative analysis of the microgrid tie inverter.

3.2.2. Filter Circuit Analysis

Due to the limitations of the filter impedance analysis method described in previous section, detailed circuit analysis of the filter will be performed. Circuit analysis will be performed under the following assumptions:

- Analysis is based on the fundamental frequency analysis only.
- Higher order frequencies will be analyzed separately in later chapters.
- Parasitic parameters in the circuit are neglected.
- Microgrid active and reactive power load is represented as a constant base impedance Z_b with varying phase angle and base voltage V_b with 0 phase angle.
- Circuit is analyzed on a single-phase basis, and symmetry between phases is assumed.

Equivalent circuit of the MTI used for analysis is shown in Figure 3.23.

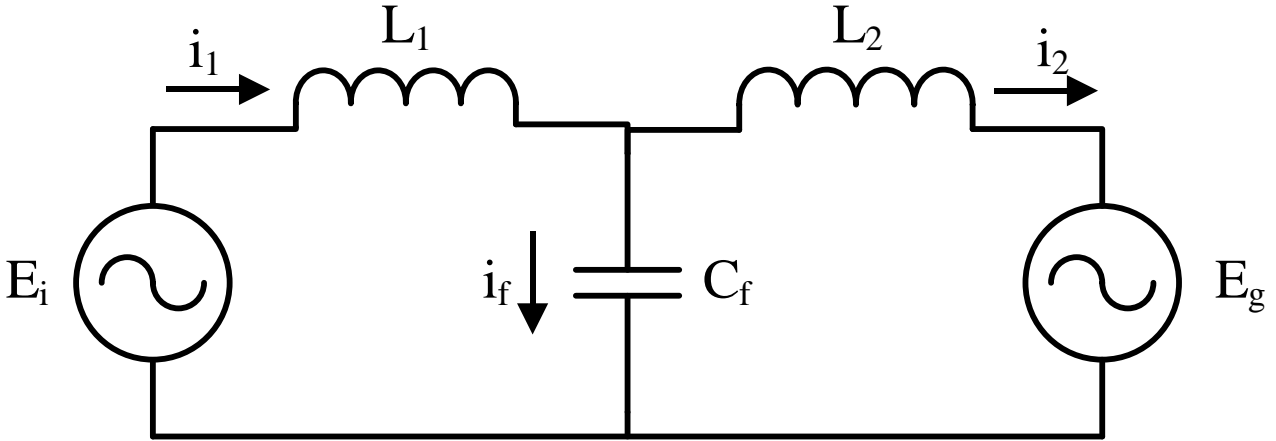


Figure 3. 23. Equivalent circuit for a current controlled MTI with voltage and current sensed on the MTI side

Basic circuit equations are derived as:

$$i_2 = \frac{E_g}{Z_b} \quad (3.19.)$$

$$V_f = E_g \left(1 + \frac{j\omega L_2}{Z_b} \right) \quad (3.20.)$$

$$i_f = E_g \omega C_f \left(j - \frac{\omega L_2}{Z_b} \right) \quad (3.21.)$$

$$i_1 = E_g \left(j\omega C_f + \frac{1 - \omega^2 C_f L_2}{Z_b} \right) \quad (3.22.)$$

$$E_i = E_g \left(1 - \omega^2 C_f L_1 + \frac{j\omega(L_2 + L_1(1 - \omega^2 C_f L_2))}{Z_b} \right) \quad (3.23.)$$

Phasor diagrams are drawn in figure 3.24. for four distinct rated operating conditions: active power injection/import, and reactive power injection/import.

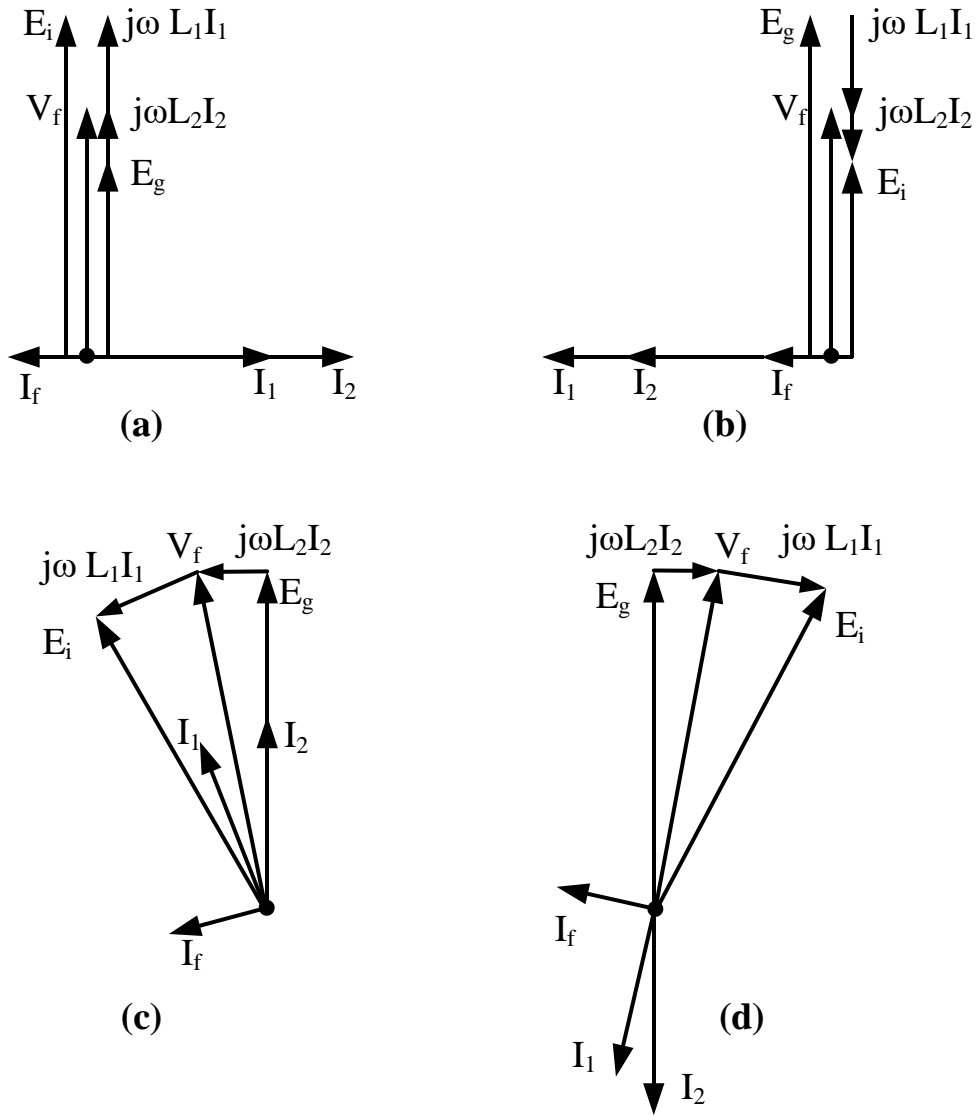


Figure 3. 24. Phasor diagrams for four distinct operating conditions a) Q=Sb b) Q=-Sb c) P=Sb d) P=-Sb

In order to quantify the circuit values, previously calculated LCL filter design parameters are used. Figure 3.25. shows the magnitude ratio between E_i and E_g in respect to power load phase angle.

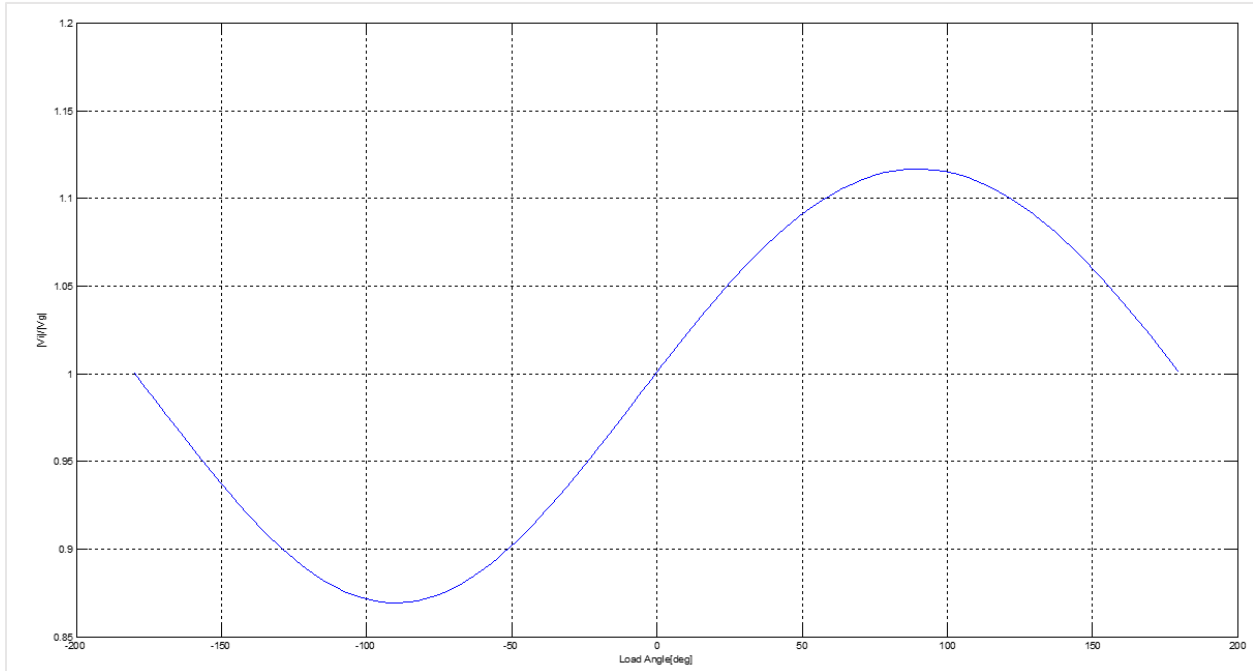


Figure 3. 25. E_i/E_g ratio dependency to power load phase angle.

At active power conditions ratio between inverter and microgrid voltage magnitudes is close to 1, but at reactive power conditions that is not the case. At reactive power import condition E_i significantly drops in magnitude, while at reactive power injection condition E_i significantly rises. Necessity for having higher E_i in order to provide reactive power support requires higher DC bus value. Higher V_{dc} requirement has a major impact on the LCL filter parameter and component selection due to higher current ripple magnitude. It also has a major impact on the switching losses of the power module device. As compared to impedance based analysis in previous section, circuit analysis performed in this section shows that the actual voltage magnitude difference on converter and microgrid side is lower than impedance magnitude difference between the two expressed in percent's.

Figure 3.26. shows a phase angle difference between E_i and E_g in respect to power load phase angle.

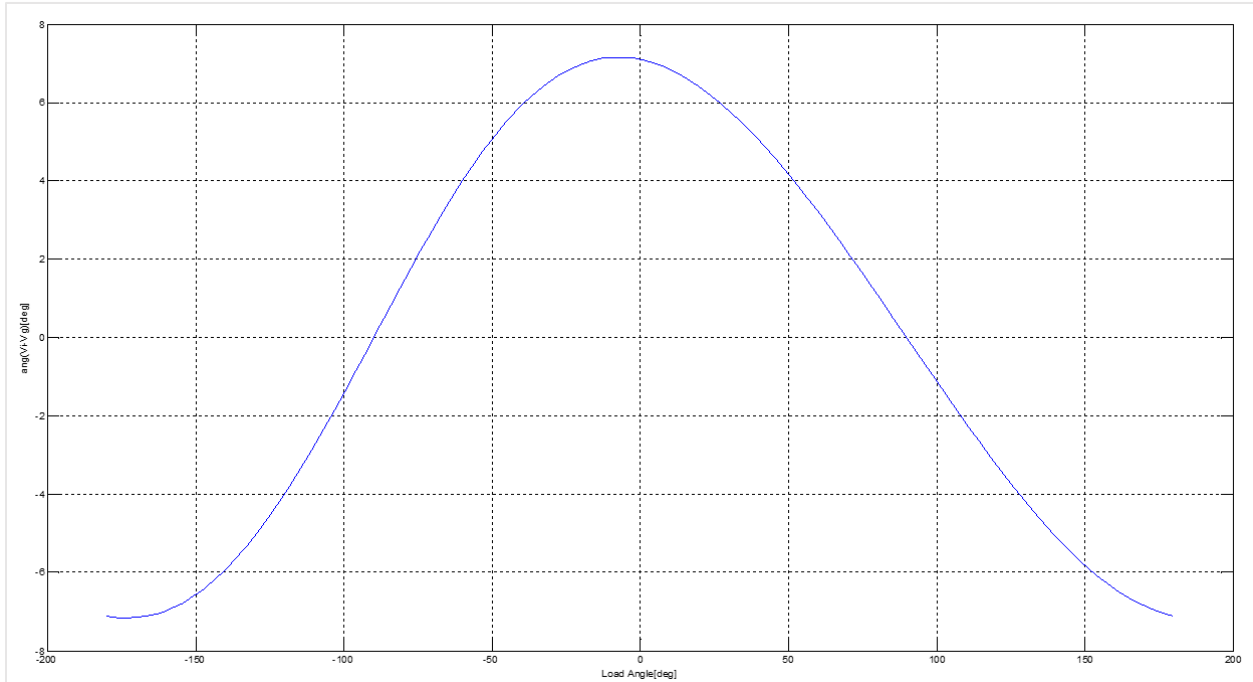


Figure 3. 26. Phase Angle difference $E_i - E_g$ in respect to power load phase angle.

Angle difference between E_i and E_g shown in Figure 3.26. changes polarity and magnitude based on the active power flow direction. When reactive power flow condition is analyzed, angle difference is close to zero. Based on results shown in figures 3.25. and 3.26., it can be simplified that E_i and E_g magnitude difference controls reactive power flow, while E_i and E_g phase difference controls active power flow.

Finally, in order to define complete set of operating requirements of the MTI, Figure 3.27. represents a converter power factor in respect to power load phase angle. It is clear that converter needs to be able to operate under power factor value range from -1 to 1 in both leading and lagging conditions.

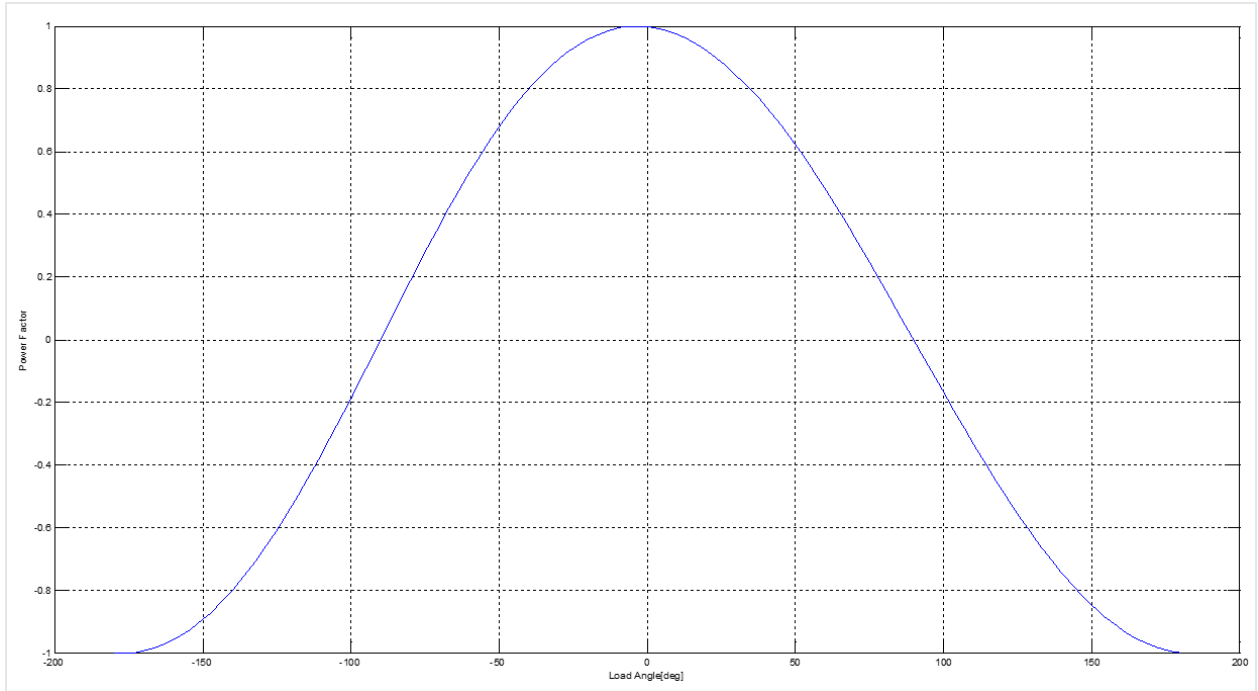


Figure 3. 27. Converter power factor in respect to power load phase angle.

3.3. Equivalent modeling of an LCL Filter

3.3.1. Single phase model

3.3.1.1. Basic Model

The initial LCL filter model is to be analyzed based on a single phase equivalent circuit as shown in Figure 3.28.

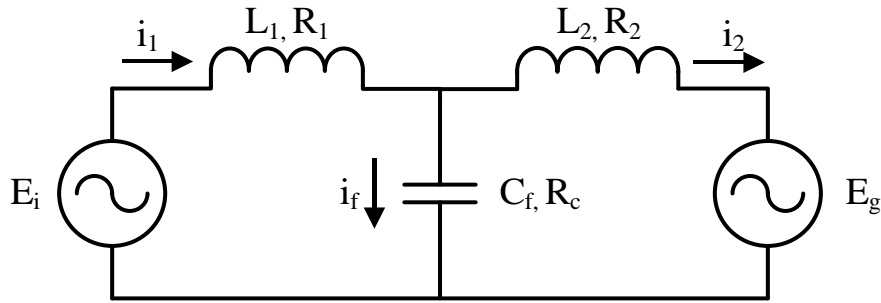


Figure 3. 28. Single phase equivalent circuit

In *LCL* filter model L_1 is the inverter side inductor, L_2 is the output side inductor, C_f is a capacitor with a series R_c resistor, R_1 and R_2 are inductor equivalent series resistances, and voltages E_i and E_g are the inverter voltage and output system voltage. Currents i_1 , i_f , and i_2 are the inverter output current, the capacitor current, and the grid current.

Applying the Kirchoff's law on the equivalent circuit gives a following set of equations:

$$E_i - L_1 \frac{di_1}{dt} - R_1 i_1 - V_f - R_c C_f \frac{dV_f}{dt} = 0 \quad (3.24.)$$

$$V_f + R_c i_f - L_2 \frac{di_2}{dt} - R_2 i_2 - E_g = 0 \quad (3.25.)$$

$$i_1 - C_f \frac{dV_f}{dt} - i_2 = 0 \quad (3.26.)$$

The LCL filter state-space model is derived from the single phase model shown in figure

3.28. as:

$$\frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \\ V_f \end{bmatrix} = \begin{bmatrix} -\frac{R_1 + R_c}{L_1} & \frac{R_c}{L_1} & -\frac{1}{L_1} \\ \frac{R_c}{L_2} & -\frac{R_2 + R_c}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ V_f \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{L_1} \\ -\frac{1}{L_2} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} E_g \\ E_i \end{bmatrix} \quad (3.27.)$$

3.3.1.2. Grid/Microgrid Effect

Equivalent model of a grid/microgrid on the output side can become very complicated based on the overall system level topology and its operating state, but most often it can be simplified to a first order model using a simple equivalent Thevenin circuit with parameters E_g , L_g , R_g as shown in figure 3.29.

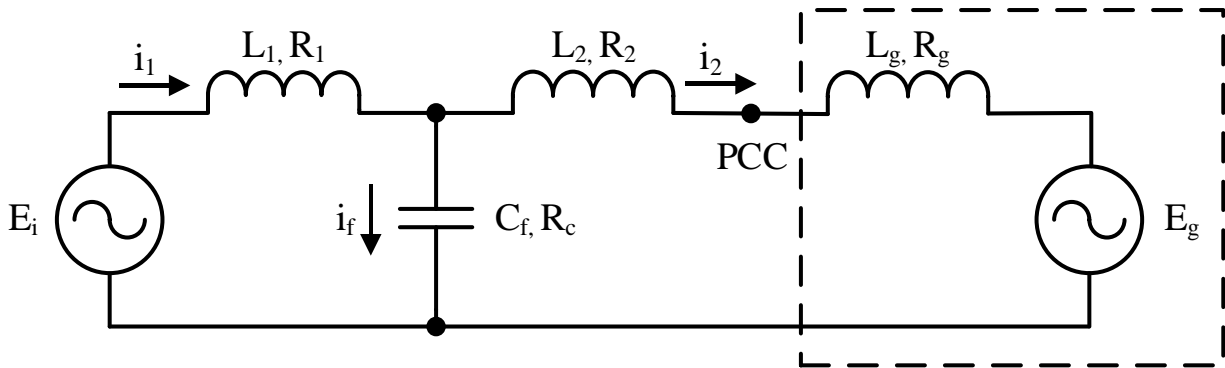


Figure 3. 29. Single phase equivalent circuit including grid model

These parameters can be merged into a following single phase LCL filter state-space model:

$$\frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \\ V_f \end{bmatrix} = \begin{bmatrix} -\frac{R_1 + R_c}{L_1} & \frac{R_c}{L_1} & -\frac{1}{L_1} \\ \frac{R_c}{L_2 + L_g} & -\frac{R_2 + R_g + R_c}{L_2 + L_g} & \frac{1}{L_2 + L_g} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ V_f \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{L_1} \\ -\frac{1}{L_2 + L_g} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} E_g \\ E_i \end{bmatrix} \quad (3.28.)$$

From the state space model it is clear that i_1 , i_2 and V_f represent three states corresponding to the only three elements in the circuit, L_1 , L_2 and C_f , that possess energy storing capability.

To study the effect of the choice of L_1 , L_2 and C_f on filter characteristics, a set of transfer functions needs to be derived.

- Transfer function from the inverter voltage E_i to the grid current i_2 :

$$G_i(s) = \frac{i_2(s)}{E_i(s)} = \frac{sC_f R_c + 1}{s^3 C_f L_1 (L_2 + L_g) + s^2 C_f [L_1 (R_2 + R_g + R_c) + (L_2 + L_g)(R_1 + R_c)] + s [C_f (R_1 R_c + (R_2 + R_g)(R_1 + R_c)) + L_1 + L_2 + L_g] + R_1 + R_2 + R_g} \quad (3.29.)$$

- Transfer function from the inverter voltage E_i to the inverter current i_1 :

$$\frac{i_1(s)}{E_i(s)} = \frac{s^2 C_f (L_2 + L_g) + s C_f (R_2 + R_g + R_c) + 1}{s^3 C_f L_1 (L_2 + L_g) + s^2 C_f [L_1 (R_2 + R_g + R_c) + (L_2 + L_g)(R_1 + R_c)] + s [C_f (R_1 R_c + (R_2 + R_g)(R_1 + R_c)) + L_1 + L_2 + L_g] + R_1 + R_2 + R_g} \quad (3.30.)$$

- Transfer function from the inverter voltage E_i to the capacitor voltage V_f :

$$\frac{V_f(s)}{E_i(s)} = \frac{s(L_2 + L_g) + R_2 + R_g}{s^3 C_f L_1 (L_2 + L_g) + s^2 C_f [L_1 (R_2 + R_g + R_c) + (L_2 + L_g)(R_1 + R_c)] + s [C_f (R_1 R_c + (R_2 + R_g)(R_1 + R_c)) + L_1 + L_2 + L_g] + R_1 + R_2 + R_g} \quad (3.31.)$$

- Transfer function from the grid voltage E_g to the grid current i_2 :

$$G_g(s) = \frac{i_2(s)}{E_g(s)} = \frac{-(s^2 C_f L_1 + s C_f (R_1 + R_c) + 1)}{s^3 C_f L_1 (L_2 + L_g) + s^2 C_f [L_1 (R_2 + R_g + R_c) + (L_2 + L_g)(R_1 + R_c)] + s [C_f (R_1 R_c + (R_2 + R_g)(R_1 + R_c)) + L_1 + L_2 + L_g] + R_1 + R_2 + R_g} \quad (3.32.)$$

- Transfer function from the grid voltage E_g to the inverter current i_1 :

$$\frac{i_1(s)}{E_g(s)} = \frac{-(s C_f R_c + 1)}{s^3 C_f L_1 (L_2 + L_g) + s^2 C_f [L_1 (R_2 + R_g + R_c) + (L_2 + L_g)(R_1 + R_c)] + s [C_f (R_1 R_c + (R_2 + R_g)(R_1 + R_c)) + L_1 + L_2 + L_g] + R_1 + R_2 + R_g} \quad (3.33.)$$

- Transfer function from the grid voltage E_g to the capacitor voltage V_f :

$$\frac{V_f(s)}{E_g(s)} = \frac{sL_1 + R_1}{s^3 C_f L_1 (L_2 + L_g) + s^2 C_f [L_1 (R_2 + R_g + R_c) + (L_2 + L_g)(R_1 + R_c)] + s [C_f (R_1 R_c + (R_2 + R_g)(R_1 + R_c)) + L_1 + L_2 + L_g] + R_1 + R_2 + R_g} \quad (3.34.)$$

- Transfer function from the inverter voltage E_i to the capacitor current i_f :

$$\frac{i_f(s)}{E_i(s)} = \frac{s^2 C_f (L_2 + L_g) + s C_f (R_2 + R_g)}{s^3 C_f L_1 (L_2 + L_g) + s^2 C_f [L_1 (R_2 + R_g + R_c) + (L_2 + L_g)(R_1 + R_c)] + s [C_f (R_1 R_c + (R_2 + R_g)(R_1 + R_c)) + L_1 + L_2 + L_g] + R_1 + R_2 + R_g} \quad (3.35.)$$

- Transfer function from the inverter current i_1 to the grid current i_2 :

$$\frac{i_2(s)}{i_1(s)} = \frac{s C_f R_c + 1}{s^2 C_f (L_2 + L_g) + s C_f (R_2 + R_g + R_c) + 1} \quad (3.36.)$$

- Transfer function from the inverter voltage E_i to the point of common coupling voltage V_{cc} :

$$\frac{V_{cc}(s)}{E_i(s)} = \frac{-s^2 C_f R_c L_2 + s(L_g - C_f R_c R_2) + R_g}{s^3 C_f L_1 (L_2 + L_g) + s^2 C_f [L_1 (R_2 + R_g + R_c) + (L_2 + L_g)(R_1 + R_c)] + s [C_f (R_1 R_c + (R_2 + R_g)(R_1 + R_c)) + L_1 + L_2 + L_g] + R_1 + R_2 + R_g} \quad (3.37.)$$

- Transfer function from the grid voltage E_g to the point of common coupling voltage V_{cc} :

$$\frac{V_{cc}(s)}{E_g(s)} = \frac{s^3 C_f L_1 L_2 + s^2 C_f (L_1 R_2 + L_2 (R_1 + R_c)) + s(L_1 + L_2 + C_f R_2 (R_1 + R_c)) + R_1 + R_2}{s^3 C_f L_1 (L_2 + L_g) + s^2 C_f [L_1 (R_2 + R_g + R_c) + (L_2 + L_g)(R_1 + R_c)] + s [C_f (R_1 R_c + (R_2 + R_g)(R_1 + R_c)) + L_1 + L_2 + L_g] + R_1 + R_2 + R_g} \quad (3.38.)$$

It is important to take into consideration the effect that line impedance has on the filter performance. Figure 3.30. and Figure 3.31. show the family of curves for the bode plot of transfer functions $G_i(s)$ and $G_g(s)$. Family of curves correspond to the line inductance variation between 0% and 40% with 1% increments. It is noticeable that for both low and high frequency range filter attenuation increases with the increase in line inductance, which generally means better filtering performance. However that means that filter has a longer time constant and response time of the filter increases. Also higher line inductance requires higher inverter output voltage in order to be able to push enough current thru the filter during the reactive power support phase. One important characteristic of the filter changes with line impedance increase, which is that the resonance frequency shifts lower in the frequency range. In the case of our LCL filter design, a 40% line impedance results in 1001 Hz resonant frequency. In the case of $G_i(s)$, line inductance does not have any impact on the magnitude at resonance frequency. Low order voltage harmonics produced by the inverter DDPWM based switching are lower at lower frequencies, thus will provide less excitation of the resonance in this case. On the other hand, low order harmonics produced by nonlinearities defined in chapter 2.5.3 are more likely to excite resonance at lower frequencies. However, in the case of $G_g(s)$, shifting to lower resonance frequencies also results in additional resonance damping. This means that low harmonics naturally present in a microgrid, may not be sufficiently high to cause resonance at low frequencies due to additional damping of the filter.

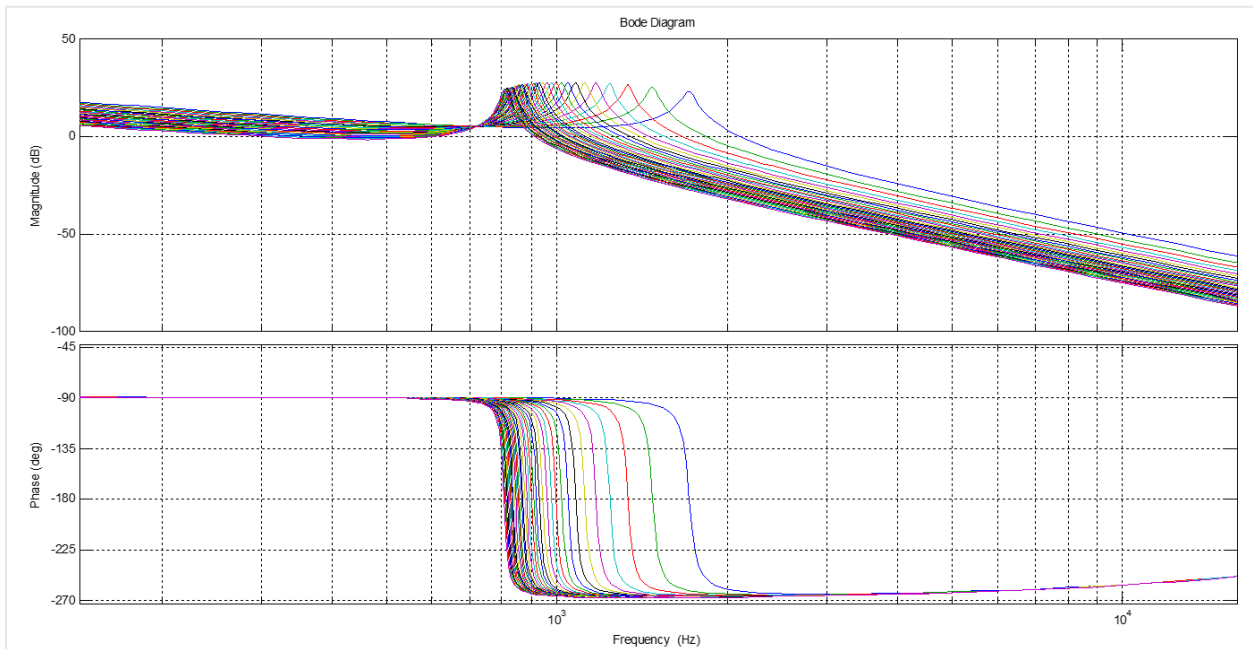


Figure 3. 30. Bode plot of transfer function $G_i(s)$ for line inductance variation

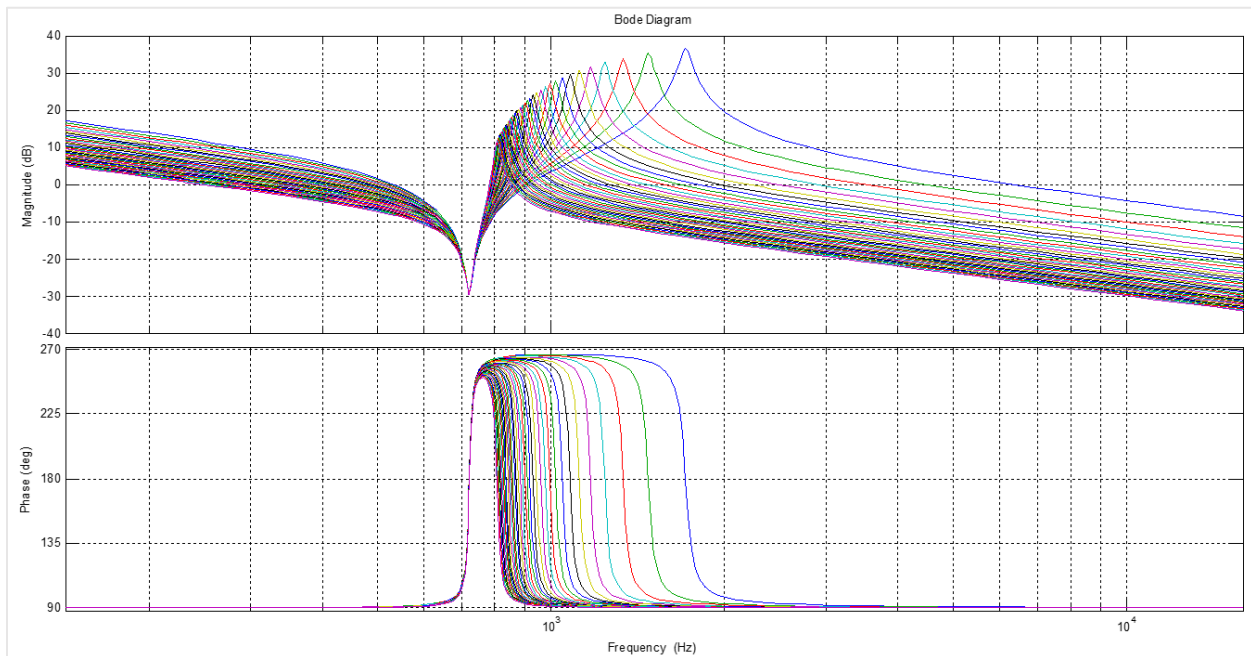


Figure 3. 31. Bode plot of transfer function $G_g(s)$ for line inductance variation

Figure 3.32. and Figure 3.33. show the family of curves for the bode plot of transfer functions $G_i(s)$ and $G_g(s)$. Family of curves correspond to the line resistance variation between 0% and 40% with 1% increments. It is noticeable that the line resistance has a dominant influence in low frequency range where the filter attenuation increases with the increase in line resistance.

Also there is an influence on the phase in the low frequency domain, meaning that the filter does not have a dominant inductive component any more. There is almost no effect of the line resistance on filter performance in the high frequency range, since reactance become dominant in the circuit. The resonance frequency value also does not change, but there is a noticeable damping effect that smooths out the resonant peak at resonant frequency.

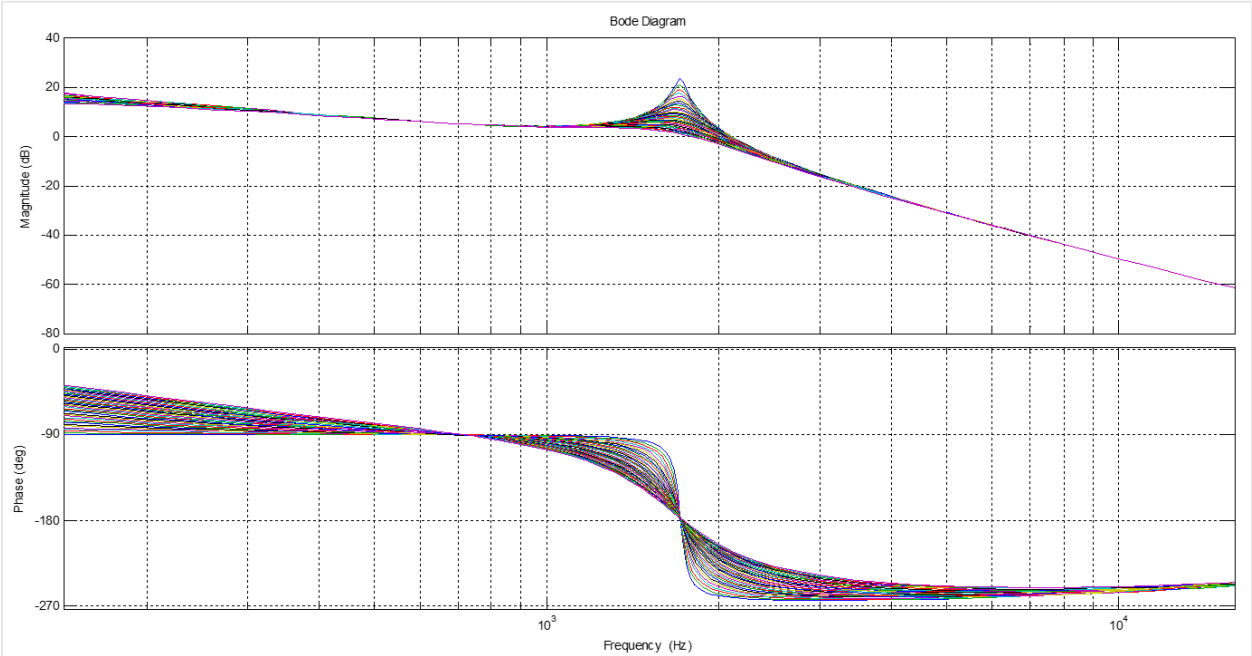


Figure 3. 32. Bode plot of transfer function $G_t(s)$ for line resistance variation

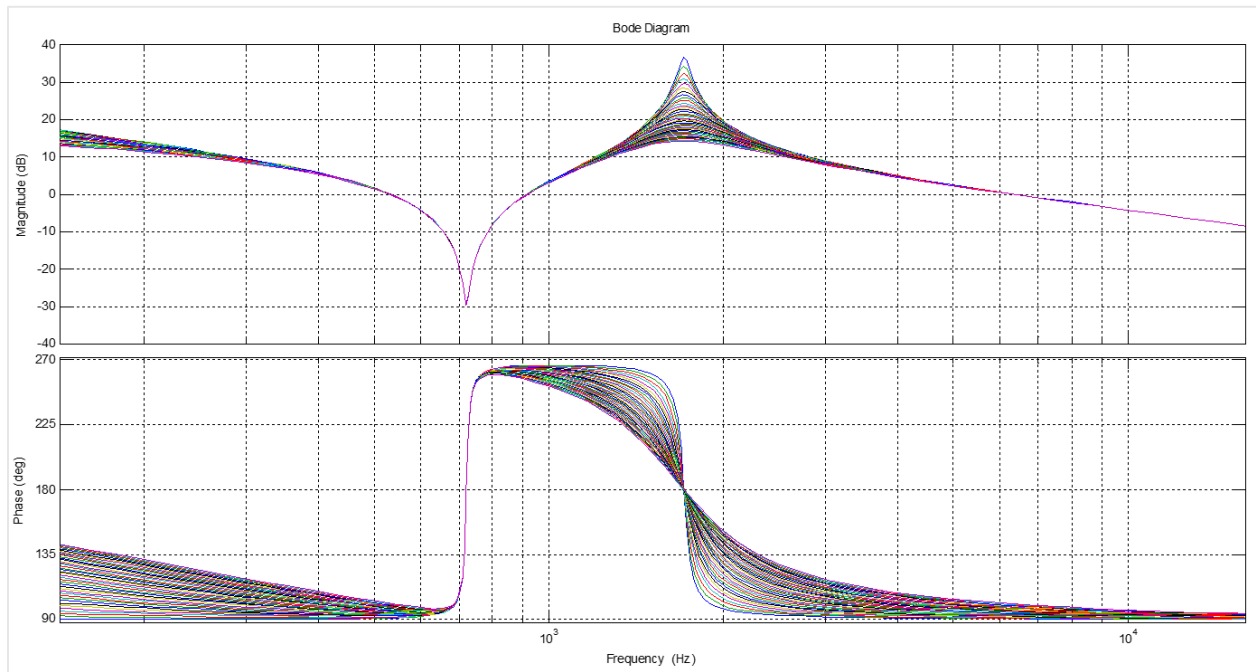


Figure 3. 33. Bode plot of transfer function $G_g(s)$ for line resistance variation

3.3.1.3. Inductor Coupling Effect

LCL passive filters are quite bulky and represent one of the most expensive components in inverter system design. In order to reduce the cost and improve the power density, magnetic integration technique is often adopted by means of utilizing a single integrated inductor solution, resulting in minimized magnetic core design [11][12].

In cases of inverter designs that are not using isolation transformer as part of the filter, coupling effect between two filter inductors can be achieved in two different ways:

- 1) Positive Coupling
- 2) Negative Coupling

An example of the typical positive coupled configuration of two filter inductors is shown in following figure:

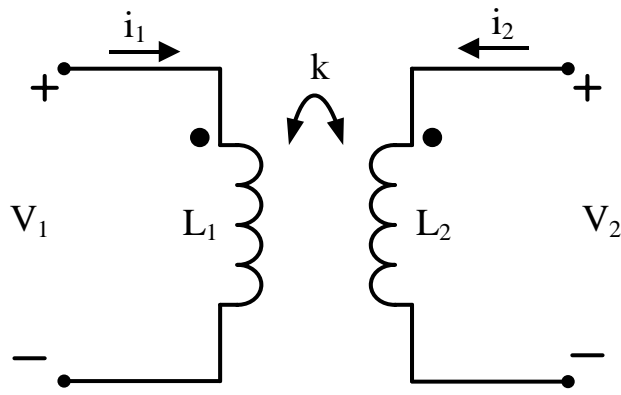


Figure 3. 34. Positive coupled filter inductor symbols

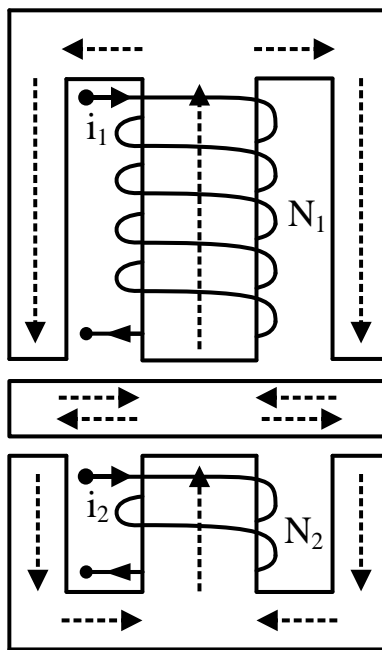


Figure 3. 35. Typical Positive coupled filter inductor configuration

An example of the typical negative coupled configuration of two filter inductors is shown in following figure:

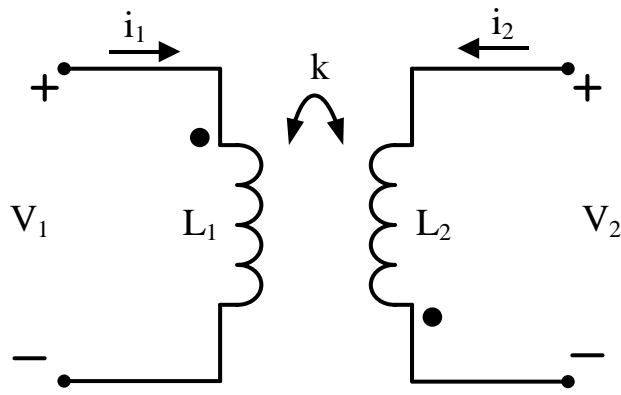


Figure 3. 36. Negatively coupled filter inductor symbol

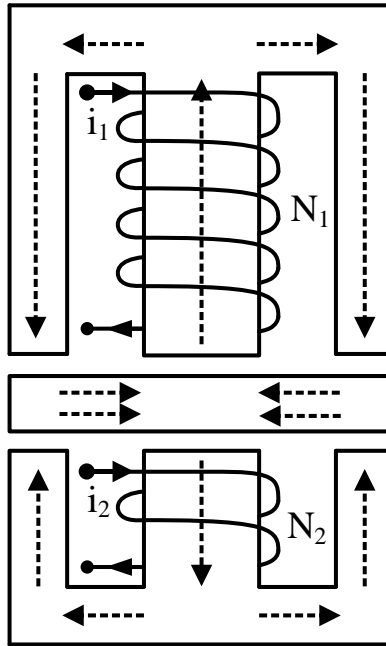


Figure 3. 37. Typical Negative coupled filter inductor configuration

A set of equations explaining the coupling effect between the two filter inductors becomes:

$$V_{l1} = R_{l1}i_1 + L_1 \frac{di_1}{dt} + L_M \frac{di_2}{dt} \quad (3.39)$$

$$V_{l2} = R_{l2}i_2 + L_M \frac{di_1}{dt} + L_2 \frac{di_2}{dt} \quad (3.40.)$$

The mutual inductance between the two coils L_M can be expressed in terms of the self inductance of each of the coils L_1 and L_2 , the amount of inductive coupling between the coils expressed via coefficient of coupling K and its sign representing either positive or negative coupling between the coils:

$$L_M = K\sqrt{L_1L_2} \quad (3.41.)$$

Generally, if $|K| = 1$ the two coils are perfectly coupled, if $|K| > 0.5$ the coils are said to be tightly coupled, and if $|K| < 0.5$ the coils are said to be loosely coupled.

In a typical coupled inductor configuration, like the one shown in figures 3.35. and 3.37., inductors are loosely coupled in order to preserve the overall performance of the filter.

Considering the coupling effect between the filter inductors, three phase filter is represented by a following linear state space model:

$$\frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} -\frac{(L_2 + L_g)R_1 + (L_2 + L_g + L_M)R_c}{(L_1(L_2 + L_g) - L_M^2)} & \frac{L_MR_2 + (L_2 + L_g + L_M)R_c}{(L_1(L_2 + L_g) - L_M^2)} & -\frac{L_2 + L_g + L_M}{(L_1(L_2 + L_g) - L_M^2)} \\ \frac{L_MR_1 + (L_1 + L_M)R_c}{(L_1(L_2 + L_g) - L_M^2)} & -\frac{L_1R_2 + (L_1 + L_M)R_c}{(L_1(L_2 + L_g) - L_M^2)} & \frac{L_1 + L_M}{(L_1(L_2 + L_g) - L_M^2)} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ V_f \end{bmatrix} + \begin{bmatrix} \frac{L_M}{(L_1(L_2 + L_g) - L_M^2)} & \frac{L_2}{(L_1(L_2 + L_g) - L_M^2)} \\ -\frac{L_1}{(L_1(L_2 + L_g) - L_M^2)} & -\frac{L_M}{(L_1(L_2 + L_g) - L_M^2)} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} E_g \\ E_i \end{bmatrix} \quad (3.42.)$$

The equivalent circuit models describing the coupling effect between inductors is shown in following figure:

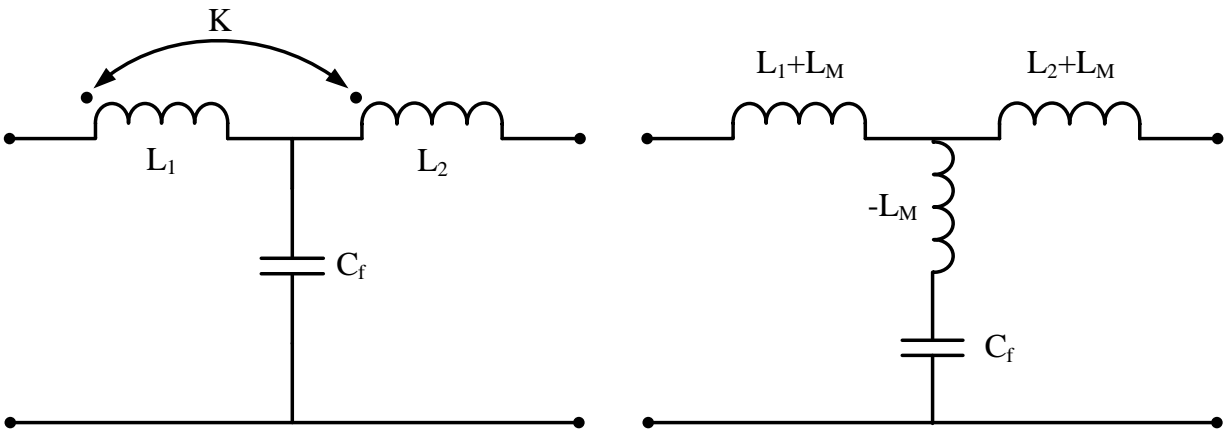


Figure 3. 38. Equivalent circuit model for Positive coupled filter inductor

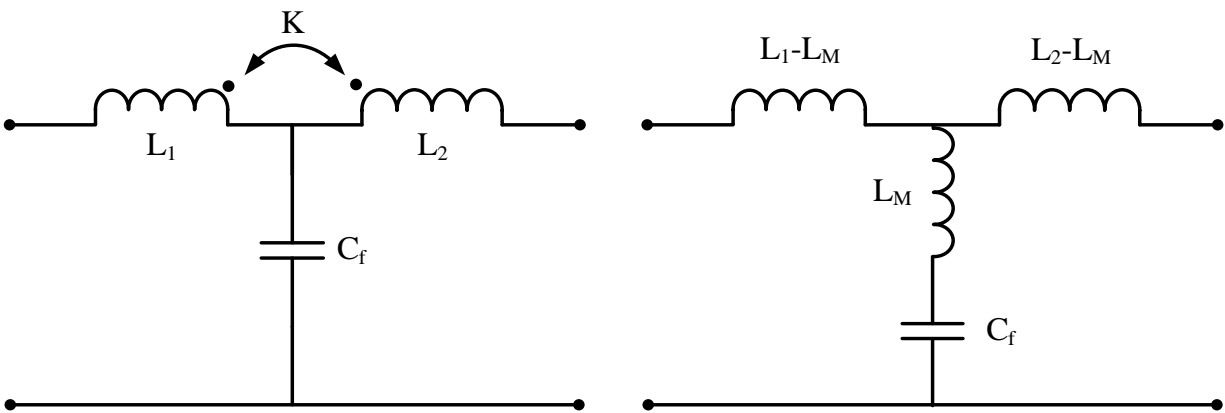


Figure 3. 39. Equivalent circuit model for Negative coupled filter inductor

In order to properly optimize filter design, it is important to understand the effect that variation of coupling factor K has on the filter performance. Figures 3.40. – 3.43. show the family of curves for the bode plot of transfer functions $G_i(s)$ and $G_g(s)$ for variation of coupling factor K for both positive and negative coupling correspondingly. Filter parameters used for the analysis are based on values from chapter 3.1.1, and summarized in table 3.11.

Figures 3.40. and 3.41. correspond to the coupling factor K variation between 0 and 1 with 0.025 increments, meaning positive coupling. Regarding $G_i(s)$ in Figure 3.40., for low frequency range filter attenuation rate has an almost constant attenuation rate of $-20dB/dec$, however the attenuation gets increased with the increase in coupling factor K . Observing the equivalent model for positive coupling in figure 3.38., it is noticeable that the overall series inductance gets increased

due to mutual inductance adding to each of the self-inductances. Knowing that the equivalent series inductance has the dominant effect in the low frequency range, higher attenuation is expected with higher levels of K . Higher attenuation means better filter performance in low frequency range. Resonance frequency significantly increases with the coupling factor increase, but the resonance magnitude does not get affected. Formula used for resonance frequency calculation is:

$$f_{res\ pc} = \frac{1}{2\pi \sqrt{\left(\frac{(L_1+L_M)(L_2+L_M)}{(L_1+L_M)+(L_2+L_M)} - L_M\right) C_f}} \quad (3.43.)$$

High frequency range provides attenuation rate of only $-20dB/dec$ after a break frequency f_{br} , which is substantially lower than $-60dB/dec$ found in standard LCL filter with discrete inductors. That leads to decreased attenuation at frequencies higher than f_{br} which is a sign of degraded filtering performance. f_{br} can be calculated as:

$$f_{br} = \frac{1}{2\pi} \sqrt{\frac{L_1 L_2 + 2L_M(L_1 + L_2) + 3L_M^2}{(L_1 L_2 - L_M^2) L_M C_f}} \quad (3.44.)$$

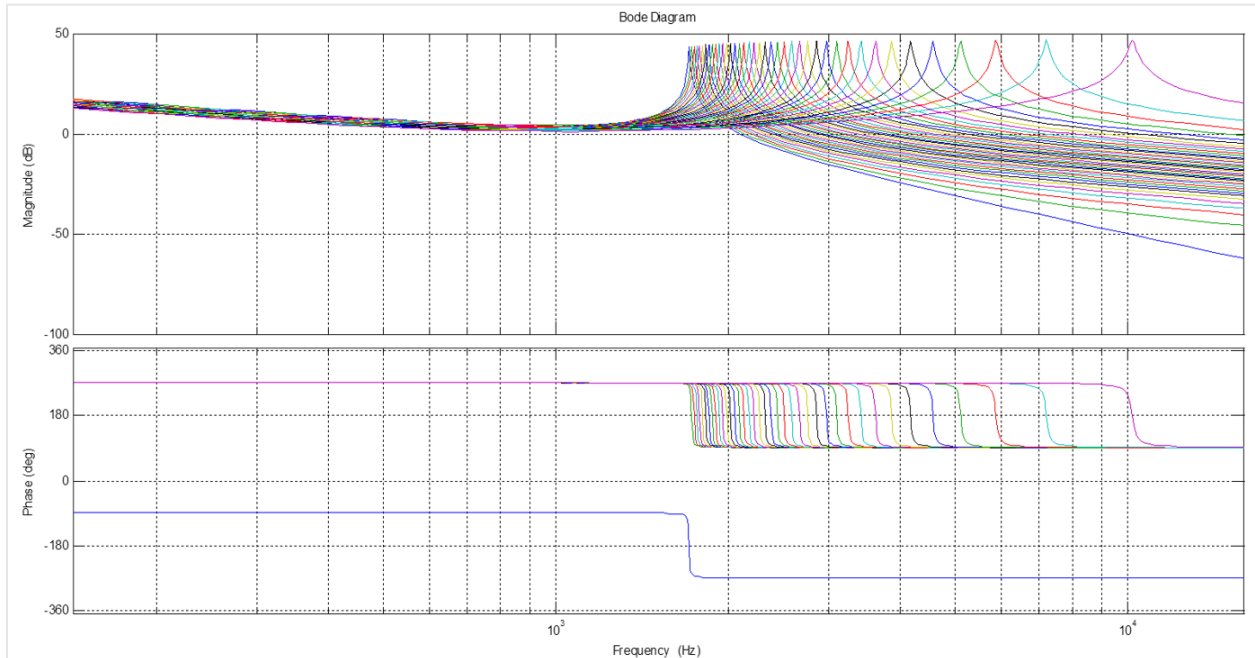


Figure 3. 40. Bode plot of transfer function $G_i(s)$ for coupling factor K variation

For $G_g(s)$ in Figure 3.41., It is noticeable that higher levels of K leads to higher attenuation at low frequency, while preserving an almost constant attenuation rate of $-20dB/dec$. Also, resonant frequency gets increased. Both of these parameters get affected in the same manner as described in the case of $G_i(s)$. Antiresonant frequency does not get affected with the coupling factor increase. Filter overall high frequency behavior gets degraded.

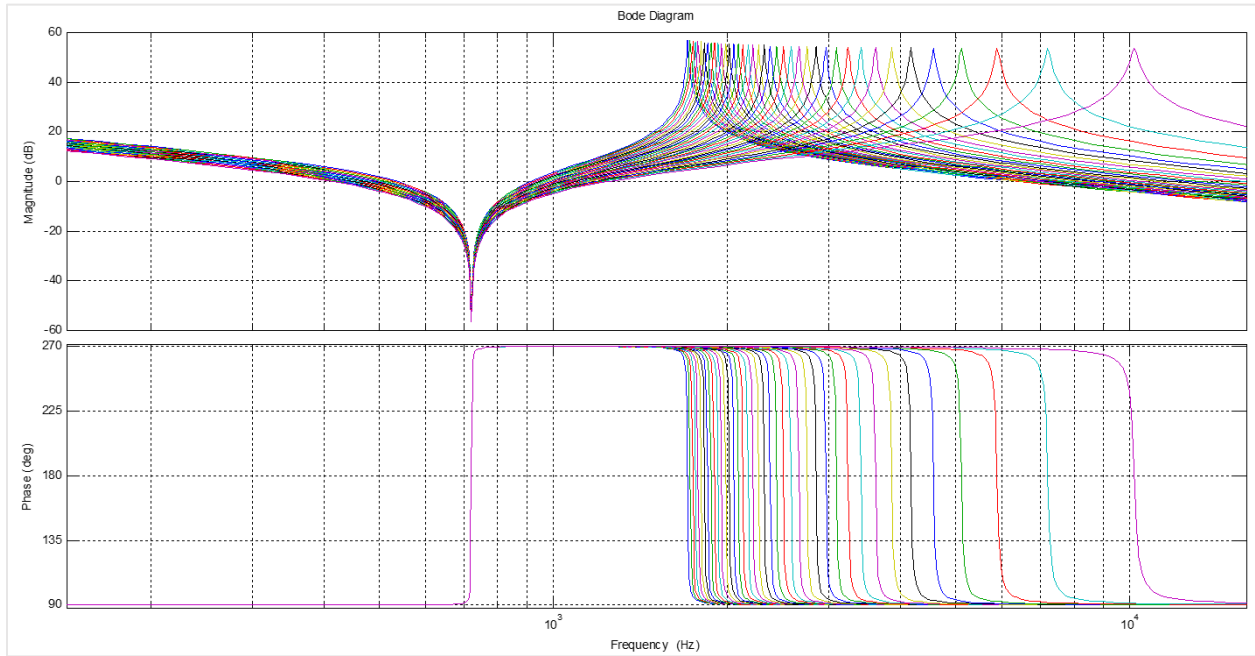


Figure 3. 41. Bode plot of transfer function $G_g(s)$ for coupling factor K variation

Figures 3.42. and 3.43. correspond to the coupling factor K variation between 0 and -1 with -0.025 increments, meaning negative coupling. For $G_i(s)$ in Figure 3.42., it is obvious that the bode plot has a form characteristic for trap filter. By observing the equivalent model for negative coupling in figure 3.39., equivalent circuit of a trap filter is recognized. It is noticeable that the overall series inductance gets decreased due to mutual inductance being subtracted from each of the self-inductances, leading to lower attenuation at lower frequencies. Resonance frequency gets

increased with the coupling factor increase and becomes less damped. Trap frequency significantly decreases with the coupling factor increase, but the resonance magnitude does not get affected. Following equations describe the resonance and trap frequency equations:

$$f_{res\ nc} = \frac{1}{2\pi\sqrt{L_M C_f}} \quad (3.45.)$$

$$f_{trap} = \frac{1}{2\pi\sqrt{\left(\frac{(L_1-L_M)(L_2-L_M)}{(L_1-L_M)+(L_2-L_M)} + L_M\right) C_f}} \quad (3.46.)$$

The Q factor for the trap filter can be taken as follows:

$$Q = \frac{\sqrt{\frac{L_M}{C_f}}}{R_n} \quad (3.47.)$$

In standard trap filter design equations, R_n represents the sum of the equivalent series inductor resistance and the equivalent series capacitor resistance. In this particular case of coupled inductors, there is no physical connections for the capacitor branch inductor, so equivalent series inductor resistance does not exist. This provides a huge advantage, because the inductor equivalent series resistance provides additional damping at the trap frequency, thus reducing filter performance.

Same as in positively coupled case, filter provides attenuation rate of only $-20dB/dec$ in high frequency range due to increase of inductance in filter capacitor branch. Increased inductance minimizes the filtering performance in high frequency range, due to increased impedance, thus minimizing filtering performance.

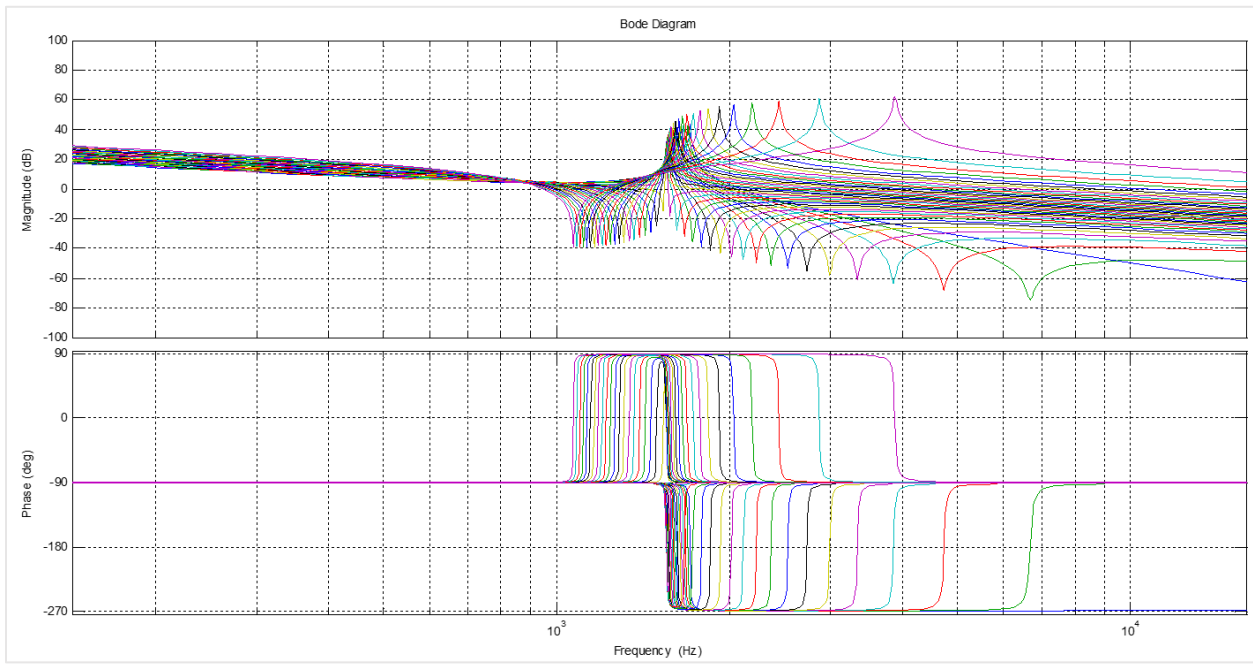


Figure 3. 42. Bode plot of transfer function $G_t(s)$ for coupling factor K variation

Regarding $G_g(s)$ in Figure 3.43., the low frequency range attenuation gets influenced with the coupling factor K leading to lower attenuation. Similar to positive coupling case shown in Figure 3.41., Resonant frequency gets increased, and antiresonant frequency does not get affected with the coupling factor increase. High frequency attenuation gets decreased, leading to poor filter performance in high frequency range.

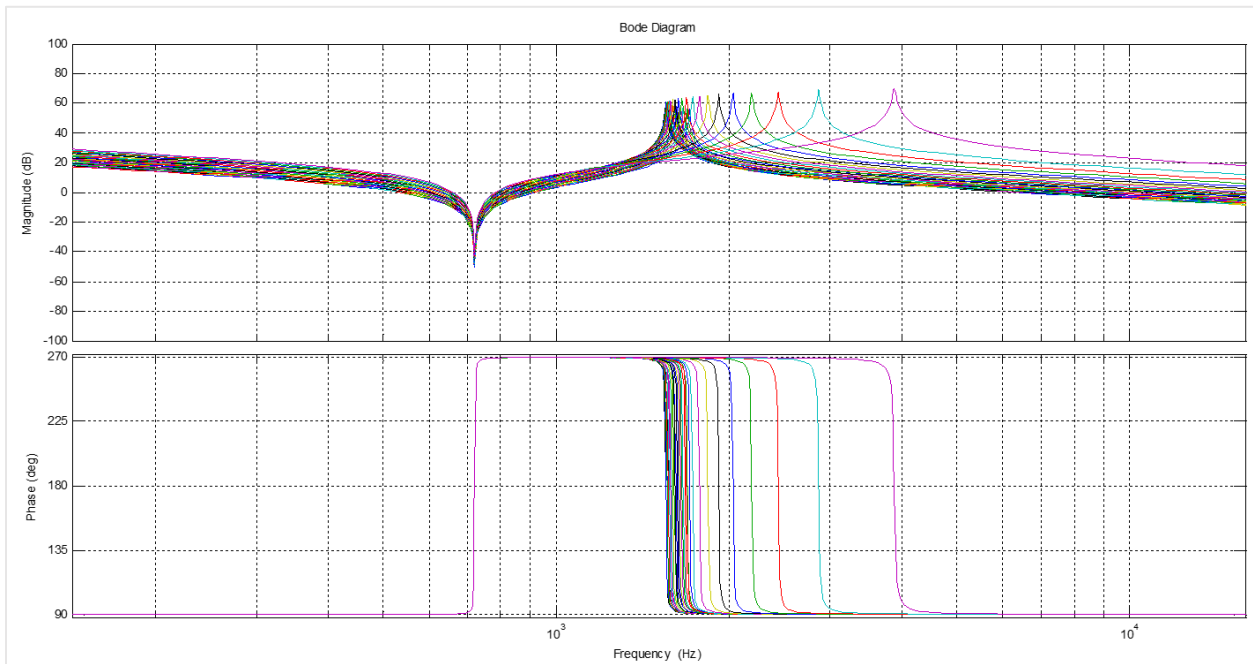


Figure 3. 43. Bode plot of transfer function $G_g(s)$ for coupling factor K variation

Positively coupled filter inductor provides a significant reduction in core material as compared to the standard two inductor solution. Material reduction is proportional to the decrease in coupling factor, meaning that lower coupling factors lead to higher material reduction. In order to explain that better, a magnetic circuit model is shown in figure 3.44. to represent positively coupled inductors shown in Figure 3.35.

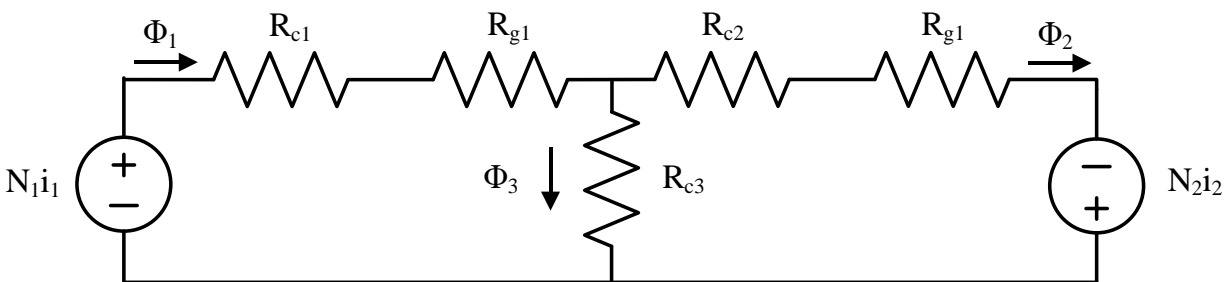


Figure 3. 44. Equivalent magnetic circuit model for Positive coupled filter inductor

- A set of equations describing differential equation for generic coupled magnetic circuit are:

$$V_1 = N_1 \frac{d\Phi_1}{dt} = L_1 \frac{di_1}{dt} + L_M \frac{di_2}{dt} \quad (3.48.)$$

$$V_2 = N_2 \frac{d\Phi_2}{dt} = L_2 \frac{di_2}{dt} + L_M \frac{di_1}{dt} \quad (3.49.)$$

- Flux equations for each of the magnetic branches are:

$$\Phi_1 = N_1 i_1 \frac{R_2 + R_{c3}}{R_1 R_2 + R_{c3}(R_1 + R_2)} \pm N_2 i_2 \frac{R_{c3}}{R_1 R_2 + R_{c3}(R_1 + R_2)} \approx \frac{N_1 i_1}{R_1} \quad (3.50.)$$

$$\Phi_2 = N_2 i_2 \frac{R_1 + R_{c3}}{R_1 R_2 + R_{c3}(R_1 + R_2)} \pm N_1 i_1 \frac{R_{c3}}{R_1 R_2 + R_{c3}(R_1 + R_2)} \approx \frac{N_2 i_2}{R_2} \quad (3.51.)$$

$$\Phi_3 = N_1 i_1 \frac{R_2}{R_1 R_2 + R_{c3}(R_1 + R_2)} \pm N_2 i_2 \frac{R_1}{R_1 R_2 + R_{c3}(R_1 + R_2)} \quad (3.52.)$$

- Self and mutual inductances in magnetic circuit are:

$$L_1 = N_1^2 \frac{R_2 + R_{c3}}{R_1 R_2 + R_{c3}(R_1 + R_2)} \approx \frac{N_1^2}{R_1} \quad (3.53.)$$

$$L_2 = N_2^2 \frac{R_1 + R_{c3}}{R_1 R_2 + R_{c3}(R_1 + R_2)} \approx \frac{N_2^2}{R_2} \quad (3.54.)$$

$$L_M = \pm \frac{R_{c3}}{R_1 R_2 + R_{c3}(R_1 + R_2)} N_1 N_2 \quad (3.55.)$$

- Coupling factor K is derived as:

$$K = \frac{L_M}{\sqrt{L_1 L_2}} = \pm \frac{R_{c3}}{\sqrt{R_1 R_2 + R_{c3}(R_1 + R_2)}} \quad (3.56.)$$

Coupling factor basically depends on the ratio between the reluctance of the common core and the square root of the product of airgap reluctances, and sign is determined based on coupling polarity.

The major goal for material saving is minimization of flux flowing thru the middle branch Φ_3 . Theoretically, by assuming no flux thru middle branch, a rough design guideline can be derived as:

$$\Phi_3 = 0 \rightarrow \frac{N_1 i_1}{N_2 i_2} = \frac{R_1}{R_2} \approx \frac{N_1}{R_1} = \frac{N_2}{R_2} \quad (3.57.)$$

In order to implement positively coupled inductor solution, the effect on the filter performance needs to be investigated first. A comparison of performance between the standard LCL and positively coupled filter design is shown in figure 3.45. for $G_i(s)$ and figure 3.46. for $G_g(s)$. Coupled inductor assumes coupling factor of 0.01 which represents coupling of only 1%. Low coupling has shown to have the most significant effect on the overall material reduction. To ensure effective attenuation of switching harmonics, f_{br} must be significantly higher than the dominant switching harmonics, which was calculated at 10849 Hz.

Two characteristics look almost identical in both cases, except for the difference in high frequency performance of $G_i(s)$.

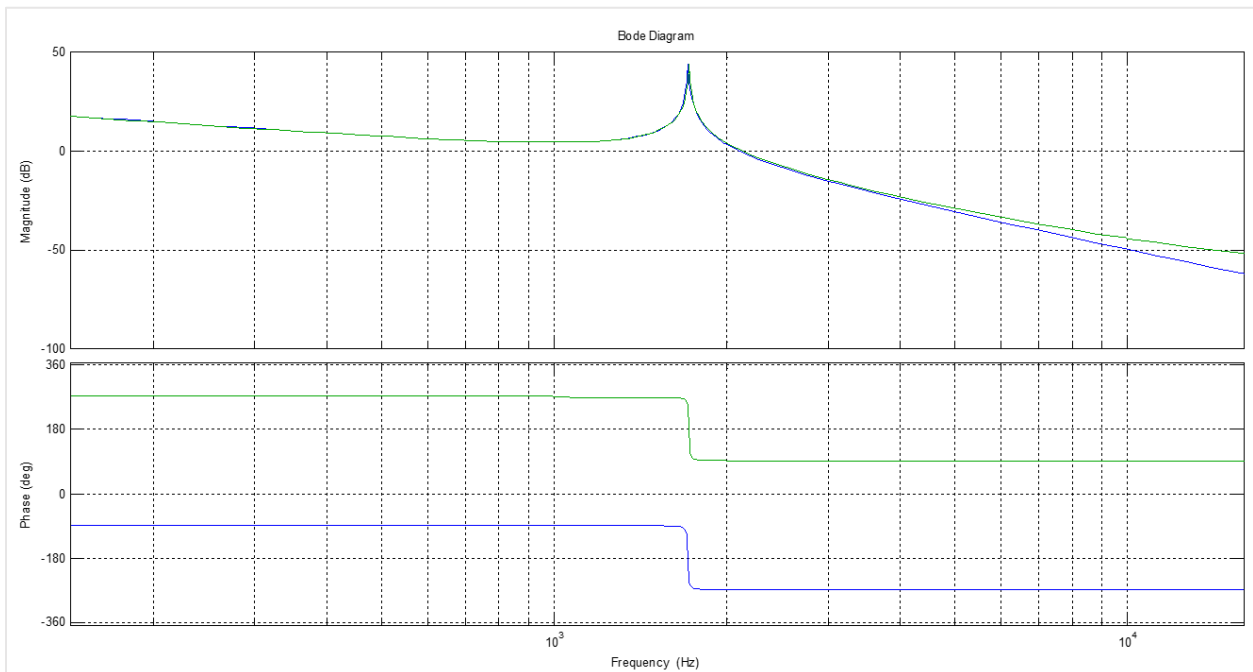


Figure 3. 45. A comparison of $G_i(s)$ between the standard LCL and positively coupled filter for $K = 0.01$

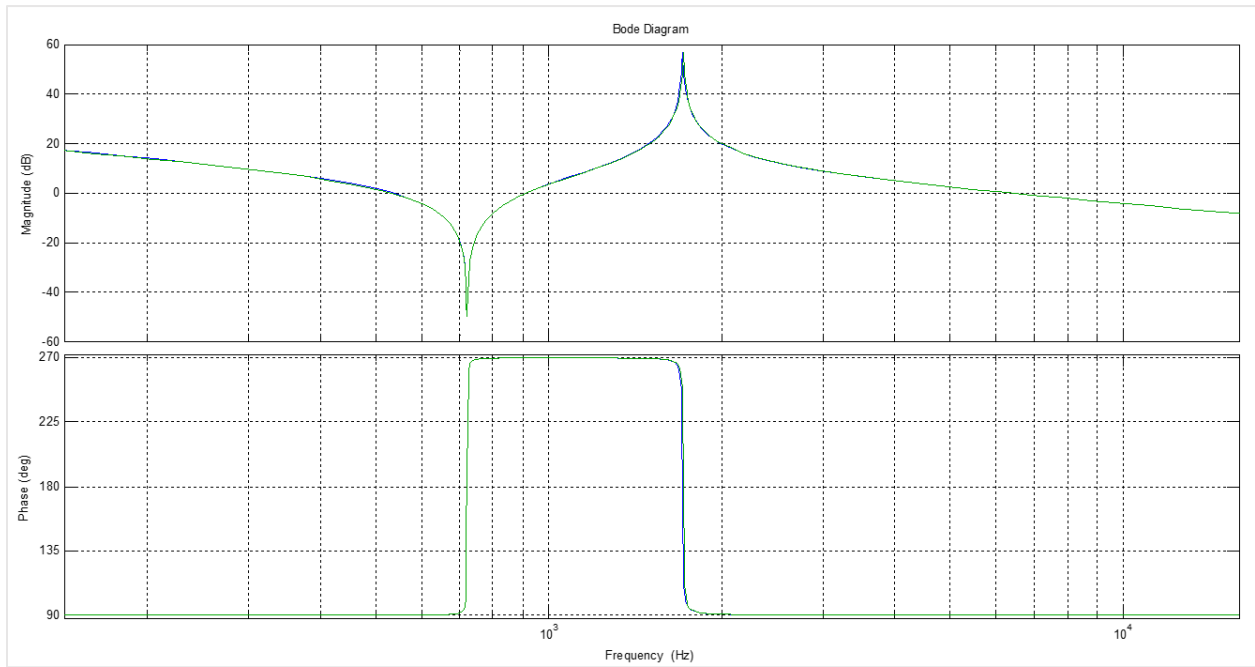


Figure 3. 46. A comparison of $G_g(s)$ between the standard LCL and positively coupled filter for $K = 0.01$

Negatively coupled filter inductor provides better discrete high frequency filtering performance as compared to the standard two inductor solution. Better filtering performance is associated only to targeted trap frequency, which is typically chosen to match the switching frequency. Trap frequency reduction is proportional to the increase in coupling factor, meaning that higher coupling factors lead to lower trap frequencies. Representative magnetic circuit model for the negatively coupled inductor is shown in figure 3.47. matching inductors shown in Figure 3.39.

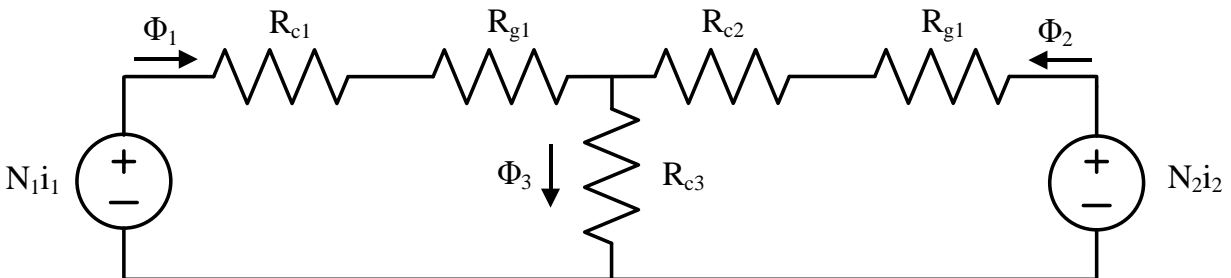


Figure 3. 47. Equivalent magnetic circuit model for Negatively coupled filter inductor

By going thru the similar set of equations as for the positively coupled case, coupling factor K is derived as:

$$K = \frac{L_m}{\sqrt{L_1 L_2}} = -\frac{R_{c3}}{\sqrt{R_1 R_2 + R_{c3}(R_1 + R_2)}} \quad (3.58.)$$

A comparison of performance between the standard LCL and negatively coupled filter design is shown in figure 3.48. for $G_i(s)$ and figure 3.49. for $G_g(s)$. Coupled inductor assumes coupling factor of -0.065 which represents negative coupling of 6.5%. 6.5% coupling is selected to target the switching frequency of $4.14kHz$ for trap filter, which results in trap frequency of $3997 Hz$. Resonant frequency is also slightly reduced to $1668 Hz$. Difference in high frequency performance of $G_i(s)$ exists, with coupled filter providing lower attenuation levels and rates. Regarding $G_g(s)$, except for the resonance frequency, two characteristics look almost identical in both cases.

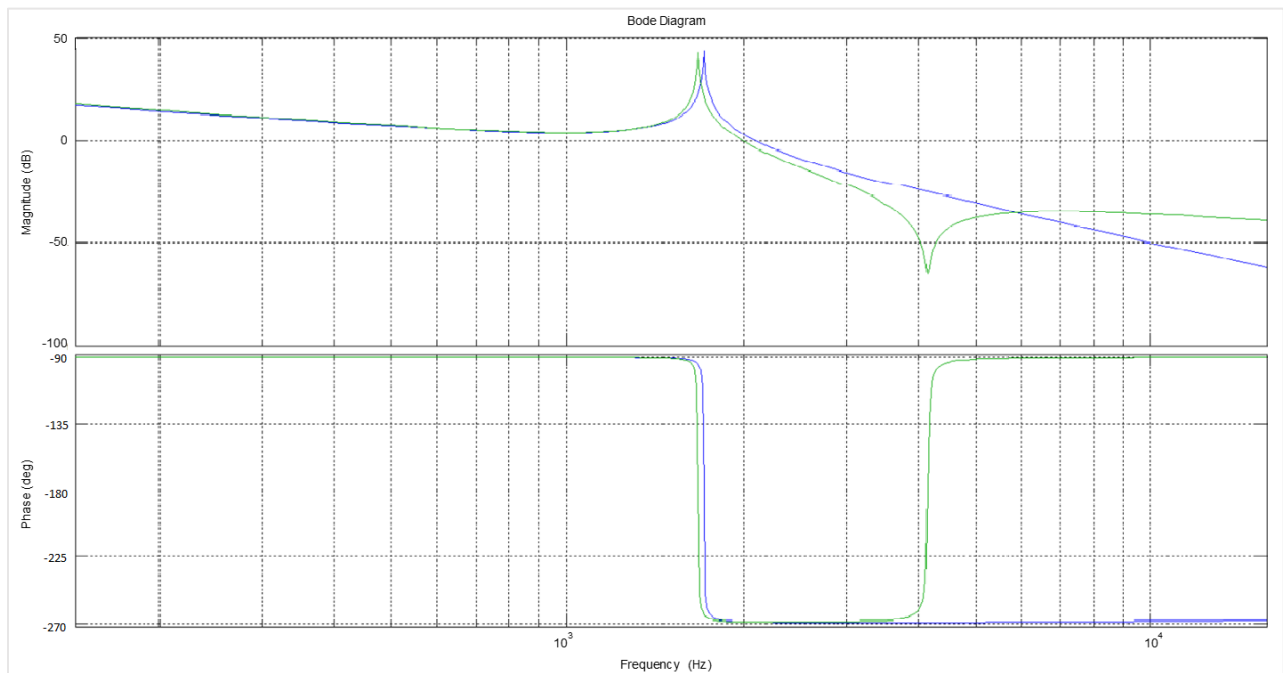


Figure 3. 48. A comparison of $G_i(s)$ between the standard LCL and negatively coupled filter for $K = -0.065$

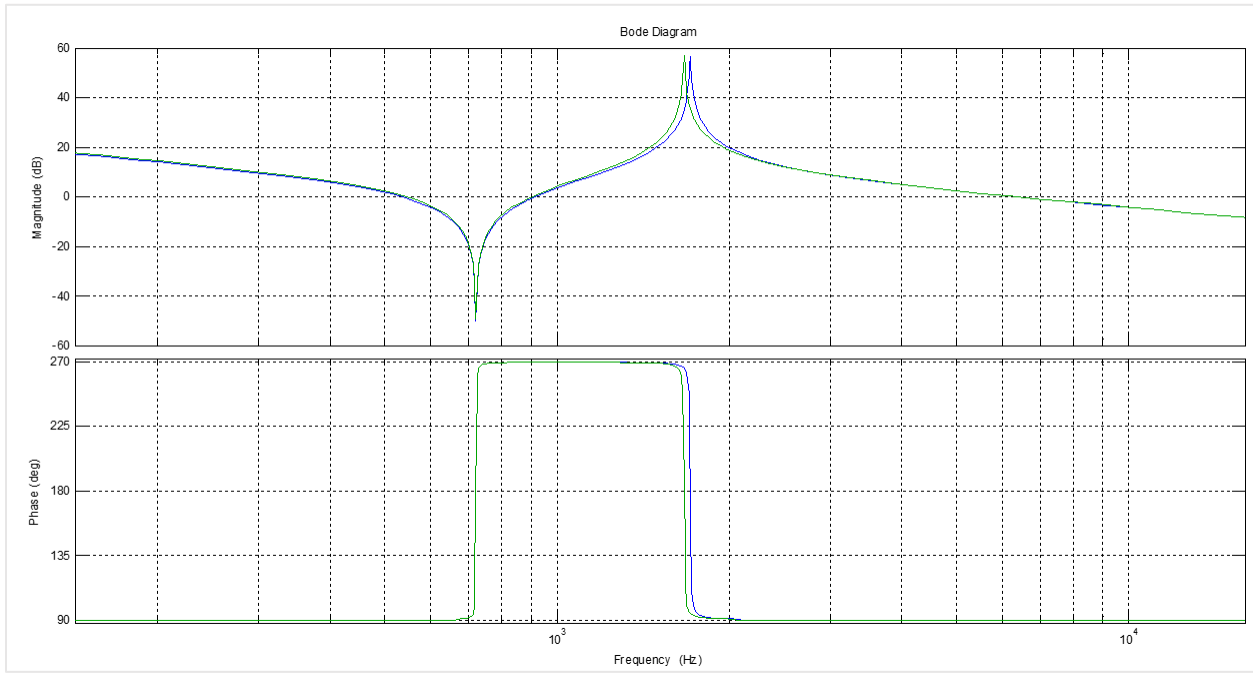


Figure 3. 49. A comparison of $G_r(s)$ between the standard LCL and negatively coupled filter for $K = -0.065$

The comparison between standard MTI inverter parameters and positively and negatively coupled inductor examples is summarized in table below:

	L_1 [%]	L_2 [%]	C_f [%]	K	L_m [%]	f_{res} [Hz]	f_{br} [Hz]	f_{trap} [Hz]
Standard MTI filter	10.19	2.2	6.8			1787.18		
Positively Coupled filter	10.24	2.25	6.8	0.01	0.047	1717.16	10848.84	
Negatively Coupled filter	9.88	1.89	6.8	-0.065	0.3	1671		4147.6

Table 3. 11. Comparison between standard MTI inverter parameters and positively and negatively coupled inductor

3.3.2. Three phase model in abc stationary reference frame

3.3.2.1. Wye Connected Filter Capacitors

A three phase LCL filter model is a natural extension to a single phase model. Simple filter model with a wye connected capacitor bank is represented in figure 3.50.

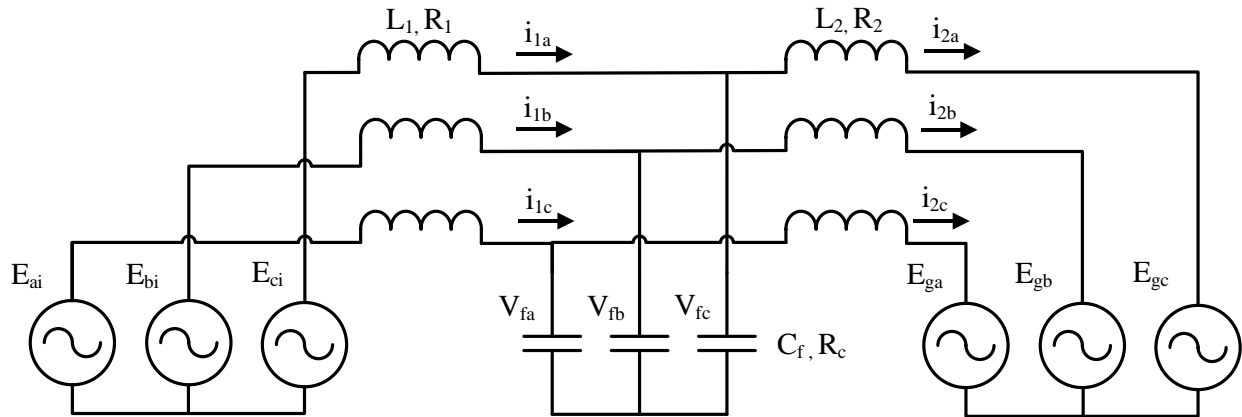


Figure 3. 50. three phase equivalent circuit

Three phase filter is represented by a following linear state space model:

$$\frac{d}{dt} \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \\ i_{2a} \\ i_{2b} \\ i_{2c} \\ V_{fa} \\ V_{fb} \\ V_{fc} \end{bmatrix} = A \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \\ i_{2a} \\ i_{2b} \\ i_{2c} \\ V_{fa} \\ V_{fb} \\ V_{fc} \end{bmatrix} + B \begin{bmatrix} E_{agt} \\ E_{bgt} \\ E_{cgt} \\ E_{ai} \\ E_{bi} \\ E_{ci} \end{bmatrix} \quad (3.59.)$$

Where:

$$A = \begin{bmatrix} -\frac{R_1 + R_c}{L_1} & 0 & 0 & \frac{R_c}{L_1} & 0 & 0 & -\frac{1}{L_1} & 0 & 0 \\ 0 & -\frac{R_1 + R_c}{L_1} & 0 & 0 & \frac{R_c}{L_1} & 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & -\frac{R_1 + R_c}{L_1} & 0 & 0 & \frac{R_c}{L_1} & 0 & 0 & -\frac{1}{L_1} \\ \frac{R_c}{L_2} & 0 & 0 & -\frac{R_2 + R_c}{L_2} & 0 & 0 & \frac{1}{L_2} & 0 & 0 \\ 0 & \frac{R_c}{L_2} & 0 & 0 & -\frac{R_2 + R_c}{L_2} & 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & \frac{R_c}{L_2} & 0 & 0 & -\frac{R_2 + R_c}{L_2} & 0 & 0 & \frac{1}{L_2} \\ \frac{1}{C} & 0 & 0 & -\frac{1}{C} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{C} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{C} & 0 & 0 & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_1} \\ -\frac{1}{L_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{L_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

3.3.2.2. Delta Connected Filter Capacitors

Delta connected capacitors require lower capacitance for the same filter performance, lower current rating, and higher voltage rating. Due to those reasons, sometimes there is a design requirement to have capacitors connected in delta configuration. Simple filter model with a delta connected capacitor bank is represented in figure 3.51.

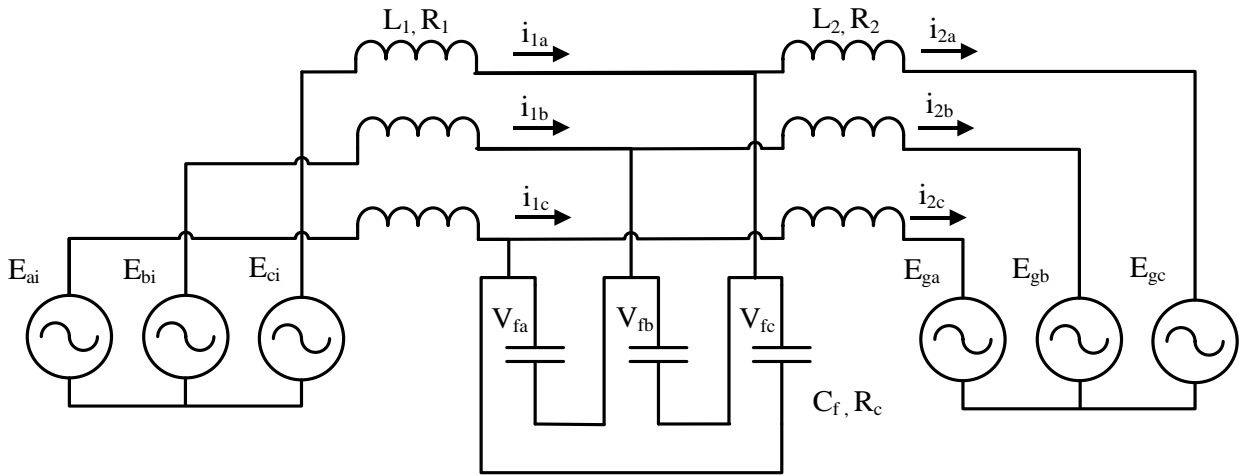


Figure 3. 51. Three phase equivalent circuit

Applying the Kirchoff's law on the equivalent circuit for a single phase gives a following set of equations:

$$E_{ai} - E_{bi} - L_1 \frac{di_{a1}}{dt} + L_1 \frac{di_{b1}}{dt} - R_1 i_{a1} + R_1 i_{b1} - V_{fab} - R_c i_{fab} = 0 \quad (3.60.)$$

$$V_{fab} + R_c i_{fab} - L_2 \frac{di_{a2}}{dt} + L_2 \frac{di_{b2}}{dt} - R_2 i_{a2} + R_2 i_{b2} - E_{ga} + E_{gb} = 0 \quad (3.61.)$$

$$i_{a1} - C_f \frac{dV_{fab}}{dt} + C_f \frac{dV_{fca}}{dt} - i_{a2} = 0 \quad (3.62.)$$

Considering the symmetry between the phases and expanding the previous set of equations

to all three phases, three phase filter is represented by a following linear state space model:

$$\frac{d}{dt} \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \\ i_{2a} \\ i_{2b} \\ i_{2c} \\ V_{fab} \\ V_{fbc} \\ V_{fca} \end{bmatrix} = A \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \\ i_{2a} \\ i_{2b} \\ i_{2c} \\ V_{fab} \\ V_{fbc} \\ V_{fca} \end{bmatrix} + B \begin{bmatrix} E_{agt} \\ E_{bgt} \\ E_{cgt} \\ E_{ai} \\ E_{bi} \\ E_{ci} \end{bmatrix} \quad (3.63.)$$

Where

$$A = \begin{bmatrix} -\frac{3R_1 + R_c}{3L_1} & 0 & 0 & \frac{R_c}{3L_1} & 0 & 0 & -\frac{1}{3L_1} & 0 & \frac{1}{3L_1} \\ 0 & -\frac{3R_1 + R_c}{3L_1} & 0 & 0 & \frac{R_c}{3L_1} & 0 & \frac{1}{3L_1} & -\frac{1}{3L_1} & 0 \\ 0 & 0 & -\frac{3R_1 + R_c}{3L_1} & 0 & 0 & \frac{R_c}{3L_1} & 0 & \frac{1}{3L_1} & -\frac{1}{3L_1} \\ \frac{R_c}{3L_2} & 0 & 0 & -\frac{3R_2 + R_c}{3L_2} & 0 & 0 & \frac{1}{3L_2} & 0 & -\frac{1}{3L_2} \\ 0 & \frac{R_c}{3L_2} & 0 & 0 & -\frac{3R_2 + R_c}{3L_2} & 0 & -\frac{1}{3L_2} & \frac{1}{3L_2} & 0 \\ 0 & 0 & \frac{R_c}{3L_2} & 0 & 0 & -\frac{3R_2 + R_c}{3L_2} & 0 & -\frac{1}{3L_2} & \frac{1}{3L_2} \\ \frac{1}{3C_f} & -\frac{1}{3C_f} & 0 & -\frac{1}{3C_f} & \frac{1}{3C_f} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{3C_f} & -\frac{1}{3C_f} & 0 & -\frac{1}{3C_f} & \frac{1}{3C_f} & 0 & 0 & 0 \\ -\frac{1}{3C_f} & 0 & \frac{1}{3C_f} & \frac{1}{3C_f} & 0 & -\frac{1}{3C_f} & 0 & 0 & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_1} \\ -\frac{1}{L_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{L_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

3.3.2.3. Filter Phase Coupling Effect

Instead of using separate inductors per each phase, inductors can often be built on the same core. Necessity for having inductors built on a common core is usually cost, weight and volume reduction driven, but it also introduces a coupling effect between the phases. Common core inductor provides a significant reduction in core material as compared to a solution consisting of 3 discrete inductors. A simple symbol showing three phase inductor on a common core is shown in figure 3.52. below:

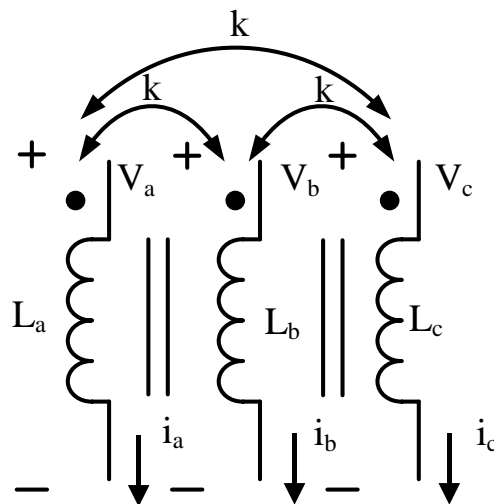


Figure 3. 52. Three phase coupled inductor symbol

An example of the two typical common core configurations, three limb and five limbs, are shown in figure 3.53. and figure 3.54. respectively.

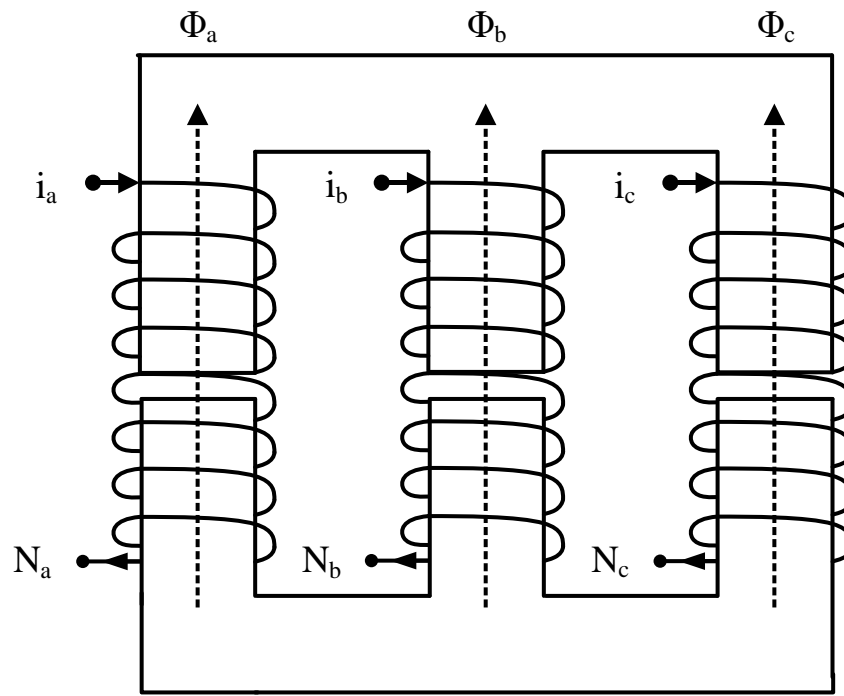


Figure 3. 53. Typical three limb inductor configuration

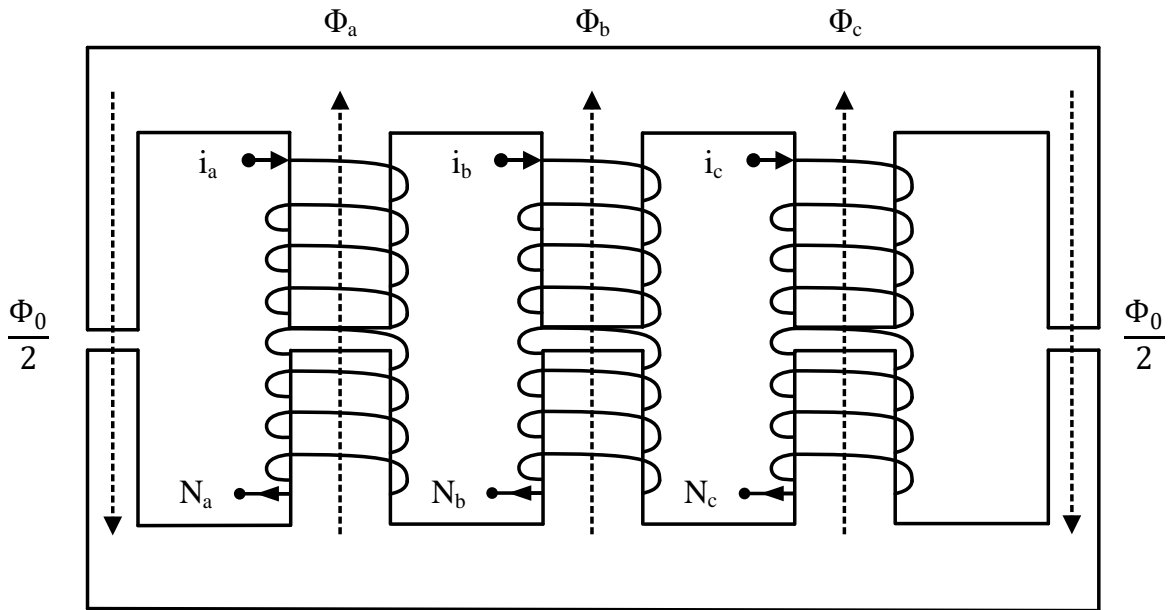


Figure 3. 54. Typical five limb inductor configuration

A set of equations explaining three phase inductor on a common core becomes:

$$V_{la} = R_{la}i_a + L_{saa} \frac{di_a}{dt} + L_{mab} \frac{di_b}{dt} + L_{mac} \frac{di_c}{dt} \quad (3.64.)$$

$$V_{lb} = R_{lb}i_b + L_{mba} \frac{di_a}{dt} + L_{sbb} \frac{di_b}{dt} + L_{mbc} \frac{di_c}{dt} \quad (3.65.)$$

$$V_{lc} = R_{lc}i_c + L_{mca} \frac{di_a}{dt} + L_{mcb} \frac{di_b}{dt} + L_{scc} \frac{di_c}{dt} \quad (3.66.)$$

In a typical common core inductor configuration, phase coupling (mutual) inductance between the phases L_m represents a fraction of the self-inductance L_s , so a coupling factor k is considered. Also since the effect from the phase coupling is such that the flux produced in each phase acts subtractive on other two phases, the sign of the coupling coefficient is negative:

$$L_m = kL_s \quad (3.67.)$$

Magnetic circuit model shown in figure 3.55 represents three limb common core inductor shown in Figure 3.53.

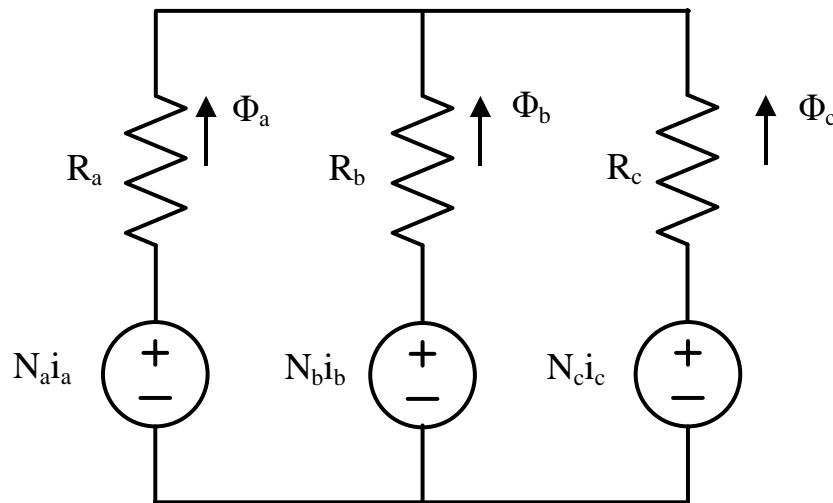


Figure 3. 55. Equivalent magnetic circuit model for three limb inductor

A set of equations describing differential equation for the magnetic circuit are:

$$V_a = N_a \frac{d\Phi_a}{dt} \quad (3.68.)$$

$$V_b = N_b \frac{d\Phi_b}{dt} \quad (3.69.)$$

$$V_c = N_c \frac{d\Phi_c}{dt} \quad (3.70.)$$

Flux equations for each of the magnetic branches are:

$$\Phi_a = N_a i_a \frac{R_b + R_c}{R_a(R_b + R_c) + R_b R_c} - N_b i_b \frac{R_c}{R_b(R_a + R_c) + R_a R_c} - N_c i_c \frac{R_b}{R_c(R_a + R_b) + R_a R_c} \quad (3.71)$$

$$\Phi_b = N_b i_b \frac{R_a + R_c}{R_b(R_a + R_c) + R_a R_c} - N_a i_a \frac{R_c}{R_a(R_b + R_c) + R_b R_c} - N_c i_c \frac{R_a}{R_c(R_a + R_b) + R_a R_c} \quad (3.72.)$$

$$\Phi_c = N_c i_c \frac{R_a + R_b}{R_c(R_a + R_b) + R_a R_c} - N_b i_b \frac{R_a}{R_b(R_a + R_c) + R_a R_c} - N_a i_a \frac{R_b}{R_a(R_b + R_c) + R_b R_c} \quad (3.73.)$$

Self and mutual inductances in magnetic circuit are

$$L_{saa} = N_a^2 \frac{R_b + R_c}{R_a R_b + R_a R_c + R_b R_c} \approx \frac{2N^2}{3R} \quad (3.74.)$$

$$L_{mab} = -N_a N_b \frac{R_c}{R_a R_b + R_a R_c + R_b R_c} \approx -\frac{N^2}{3R} \quad (3.75.)$$

$$L_{mac} = -N_a N_c \frac{R_b}{R_a R_b + R_a R_c + R_b R_c} \approx -\frac{N^2}{3R} \quad (3.76.)$$

Coupling factor k is derived as:

$$k_{ab} = \frac{L_{mab}}{L_{saa}} = -\frac{N_b}{N_a} \frac{R_c}{R_b R_c} \quad (3.77.)$$

In case of ideal symmetrical three limb inductor, where stray inductances are ignored, coupling factor is equal to -0.5.

Assuming the total symmetry between all three phases in terms of number of winding turns, core and airgap design, equivalent total flux and inductance per phase can be calculated as:

$$k = -\frac{1}{2}$$

$$\Phi_a = Ni_a \frac{2}{3R} + Ni_a \frac{1}{3R} = \frac{Ni_a}{R} \quad (3.78.)$$

$$L_{saa} = \frac{\Phi_a N}{i_a} = \frac{N^2}{R} \quad (3.79.)$$

Typically, three limb inductor is an inductor of choice in majority of cases due to reduction in required core material. The major disadvantages of three limb inductors are large coupling between phases and very low common mode inductance. Low common mode inductance is a consequence of the lack of limb in the core thru which the common mode flux could close. That leads to common mode flux closure thru the air, which is rather uncontrolled and leads to high reluctance values, thus producing low common mode inductance. In order to address previously mentioned disadvantages of three limb inductor, five limb inductor is used.

Magnetic circuit model shown in figure 3.56. represents five limb common core inductor shown in Figure 3.54.

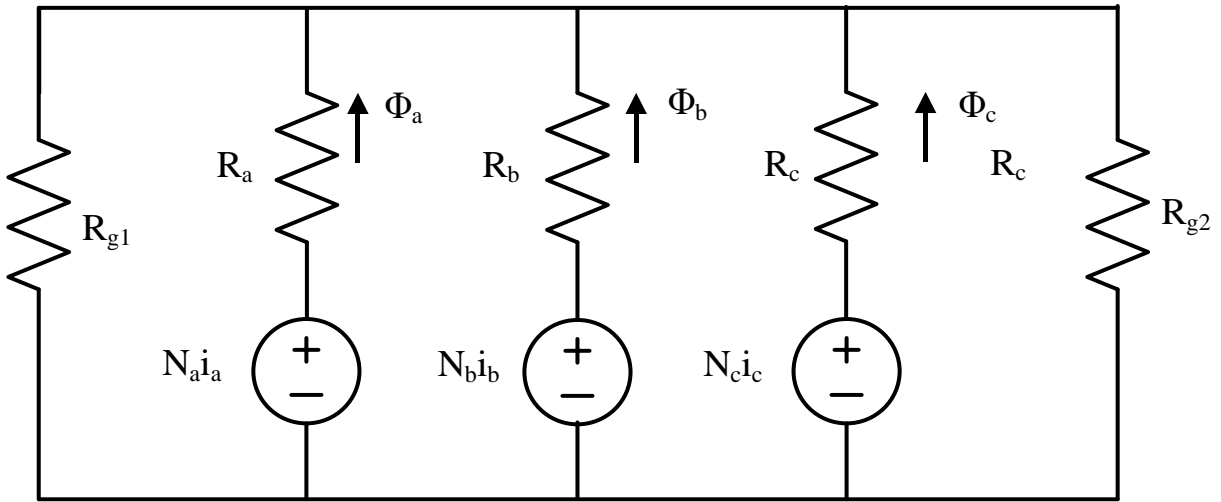


Figure 3. 56. Equivalent magnetic circuit model for five limb inductors

A set of differential equations for the magnetic circuit are:

$$V_a = N_a \frac{d\Phi_a}{dt} \quad (3.80.)$$

$$V_b = N_b \frac{d\Phi_b}{dt} \quad (3.81.)$$

$$V_c = N_c \frac{d\Phi_c}{dt} \quad (3.82.)$$

Flux equations for each of the magnetic branches are:

$$\begin{aligned} \Phi_a &= N_a i_a \frac{1}{R_a + R_g \parallel R_b \parallel R_c} \\ &- N_b i_b \frac{R_c \parallel R_g}{R_a + R_c \parallel R_g} \frac{1}{R_b + R_g \parallel R_a \parallel R_c} - N_c i_c \frac{R_b \parallel R_g}{R_a + R_b \parallel R_g} \frac{1}{R_c + R_g \parallel R_a \parallel R_b} \quad (3.83.) \end{aligned}$$

$$\begin{aligned} \Phi_b &= N_b i_b \frac{1}{R_b + R_g \parallel R_a \parallel R_c} \\ &- N_a i_a \frac{R_c \parallel R_g}{R_b + R_c \parallel R_g} \frac{1}{R_a + R_g \parallel R_b \parallel R_c} - N_c i_c \frac{R_a \parallel R_g}{R_b + R_a \parallel R_g} \frac{1}{R_c + R_g \parallel R_a \parallel R_b} \quad (3.84.) \end{aligned}$$

Φ_c

$$= N_c i_c \frac{1}{R_c + R_g \parallel R_a \parallel R_b} - N_a i_a \frac{R_b \parallel R_g}{R_c + R_b \parallel R_g} \frac{1}{R_a + R_g \parallel R_b \parallel R_c} - N_b i_b \frac{R_a \parallel R_g}{R_c + R_a \parallel R_g} \frac{1}{R_b + R_g \parallel R_a \parallel R_c} \quad (3.85.)$$

Where $R_g = R_{g1} \parallel R_{g2}$

Self and mutual inductances in magnetic circuit are:

$$L_{saa} = N_a^2 \frac{R_g R_b + R_g R_c + R_b R_c}{R_a R_g R_b + R_a R_g R_c + R_a R_b R_c + R_g R_b R_c} \quad (3.86.)$$

$$L_{mab} = N_a N_b \frac{R_c R_g}{R_a R_g R_b + R_a R_g R_c + R_a R_b R_c + R_g R_b R_c} \quad (3.87.)$$

$$L_{mac} = N_a N_c \frac{R_b R_g}{R_a R_g R_b + R_a R_g R_c + R_a R_b R_c + R_g R_b R_c} \quad (3.88.)$$

Coupling factor k is derived as:

$$k_{ab} = \frac{L_{mab}}{L_{saa}} = -\frac{N_b}{N_c} \frac{R_c R_g}{R_g (R_c + R_b) + R_c R_b} \Rightarrow -\frac{R R_g}{2R R_g + R^2} = k_{bc} = k_{ca} \quad (3.89.)$$

In case of ideal symmetrical five limb inductor, where stray inductances are ignored, coupling factor is equal to the ratio of additional limb reluctances to phase limb reluctance, which is typically a small number.

Assuming the total symmetry between all three phases, equivalent total flux and inductance per phase can be calculated as:

$$\Phi_a = Ni_a \frac{1}{R} \quad (3.90.)$$

$$L_{saa} = \frac{\Phi_a N}{i_a} = \frac{N^2}{R} \quad (3.91.)$$

The common mode inductance is calculated as:

$$\Phi_0 = \Phi_a + \Phi_b + \Phi_c = 3NI_0 \frac{R^2}{3R^2R_g + R^3} = \frac{3NI_0}{3R_g + R} \quad (3.92.)$$

$$L_0 = \frac{\Phi_0 N}{3I_0} = \frac{N^2}{3R_g + R} \quad (3.93.)$$

Considering the inductor coupling effect between the phases on both filter inductors with corresponding coupling coefficients k_1 and k_2 , three phase filter is represented by a following linear state space model:

$$\frac{d}{dt} \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \\ i_{2a} \\ i_{2b} \\ i_{2c} \\ V_{fab} \\ V_{fbc} \\ V_{fca} \end{bmatrix} = A \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \\ i_{2a} \\ i_{2b} \\ i_{2c} \\ V_{fab} \\ V_{fbc} \\ V_{fca} \end{bmatrix} + B \begin{bmatrix} E_{agt} \\ E_{bgt} \\ E_{cgt} \\ E_{ai} \\ E_{bi} \\ E_{ci} \end{bmatrix} \quad (3.94.)$$

Where:

$$A = \begin{bmatrix} -\frac{3R_1 + R_c}{3L_1(1 - k_1)} & 0 & 0 & \frac{R_c}{3L_1(1 - k_1)} & 0 & 0 & -\frac{1}{3L_1(1 - k_1)} & 0 & \frac{1}{3L_1(1 - k_1)} \\ 0 & -\frac{3R_1 + R_c}{3L_1(1 - k_1)} & 0 & 0 & \frac{R_c}{3L_1(1 - k_1)} & 0 & \frac{1}{3L_1(1 - k_1)} & -\frac{1}{3L_1(1 - k_1)} & 0 \\ 0 & 0 & -\frac{3R_1 + R_c}{3L_1(1 - k_1)} & 0 & 0 & \frac{R_c}{3L_1(1 - k_1)} & 0 & \frac{1}{3L_1(1 - k_1)} & -\frac{1}{3L_1(1 - k_1)} \\ \frac{R_c}{3(L_2(1 - k_2) + L_g)} & 0 & 0 & -\frac{3R_2 + R_c}{3(L_2(1 - k_2) + L_g)} & 0 & 0 & \frac{1}{3(L_2(1 - k_2) + L_g)} & 0 & -\frac{1}{3(L_2(1 - k_2) + L_g)} \\ 0 & \frac{R_c}{3(L_2(1 - k_2) + L_g)} & 0 & 0 & -\frac{3R_2 + R_c}{3(L_2(1 - k_2) + L_g)} & 0 & -\frac{1}{3(L_2(1 - k_2) + L_g)} & \frac{1}{3(L_2(1 - k_2) + L_g)} & 0 \\ 0 & 0 & \frac{R_c}{3(L_2(1 - k_2) + L_g)} & 0 & 0 & -\frac{3R_2 + R_c}{3(L_2(1 - k_2) + L_g)} & 0 & -\frac{1}{3(L_2(1 - k_2) + L_g)} & \frac{1}{3(L_2(1 - k_2) + L_g)} \\ \frac{1}{3C_f} & -\frac{1}{3C_f} & 0 & -\frac{1}{3C_f} & \frac{1}{3C_f} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{3C_f} & -\frac{1}{3C_f} & 0 & -\frac{1}{3C_f} & \frac{1}{3C_f} & 0 & 0 & 0 \\ -\frac{1}{3C_f} & 0 & \frac{1}{3C_f} & \frac{1}{3C_f} & 0 & -\frac{1}{3C_f} & 0 & 0 & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{L_1(1 - k_1)} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_1(1 - k_1)} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_1(1 - k_1)} \\ -\frac{1}{L_2(1 - k_2) + L_g} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{L_2(1 - k_2) + L_g} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L_2(1 - k_2) + L_g} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

One important thing to observe from the filter state space model is that despite physical coupling between the phases, there is no coupling present in the actual model. The reason behind it is that the model is built assuming that the summation of phase currents is always equal to zero, thus allowing decoupling.

3.3.2.4. Coupling Effect between Filter Inductors

In order to further reduce cost, weight and volume, for MTI designs that do not include isolation transformer, instead of using a separate set of inductors on the converter and line side, unique filter inductor can be designed using a single magnetic core.

In addition to phase coupling effect, it also introduces a coupling effect between the inductors of the same phase on the opposing sides of the filter capacitor.

A simple symbol showing the coupled three phase inductor is shown in figure 3.57. below:

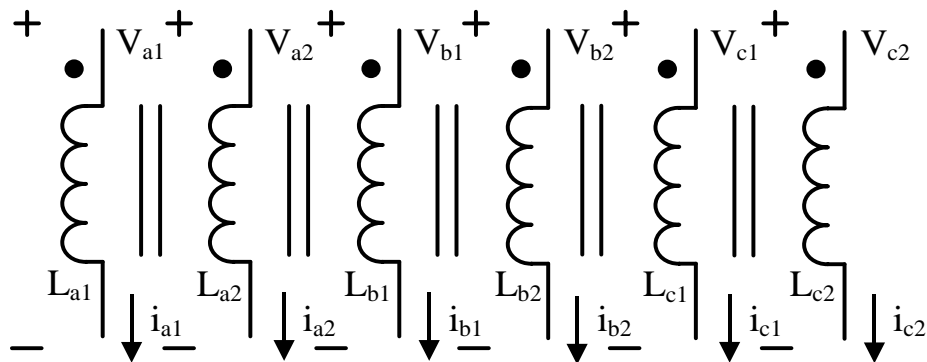


Figure 3. 57. Fully coupled three phase filter inductor symbol

An example of the typical coupled configuration of a positively coupled three phase filter inductors is shown in figures 3.58. and 3.59.:

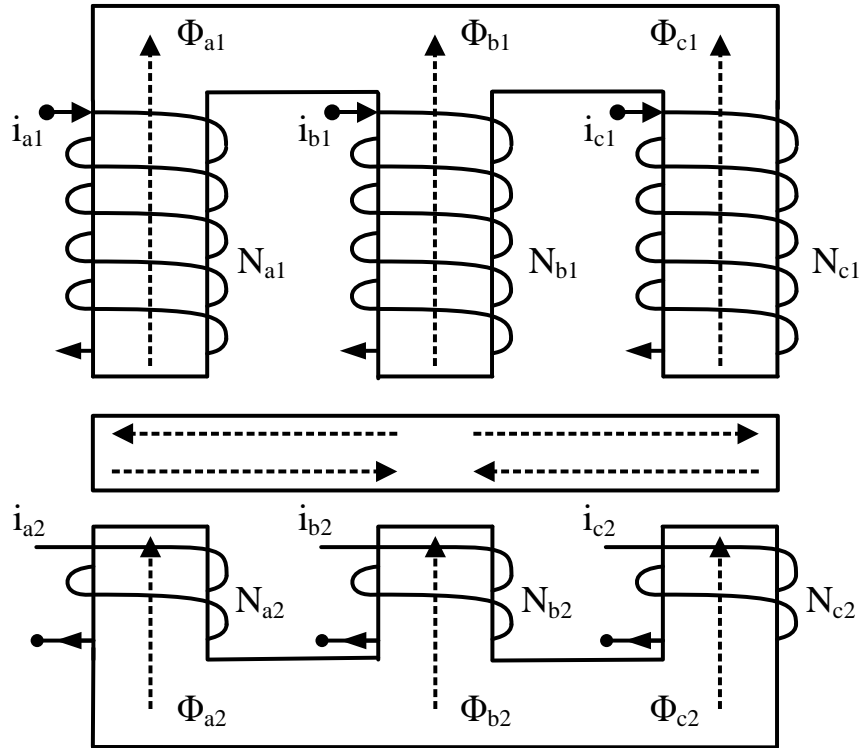


Figure 3. 58. Positively coupled three phase filter inductor configurations

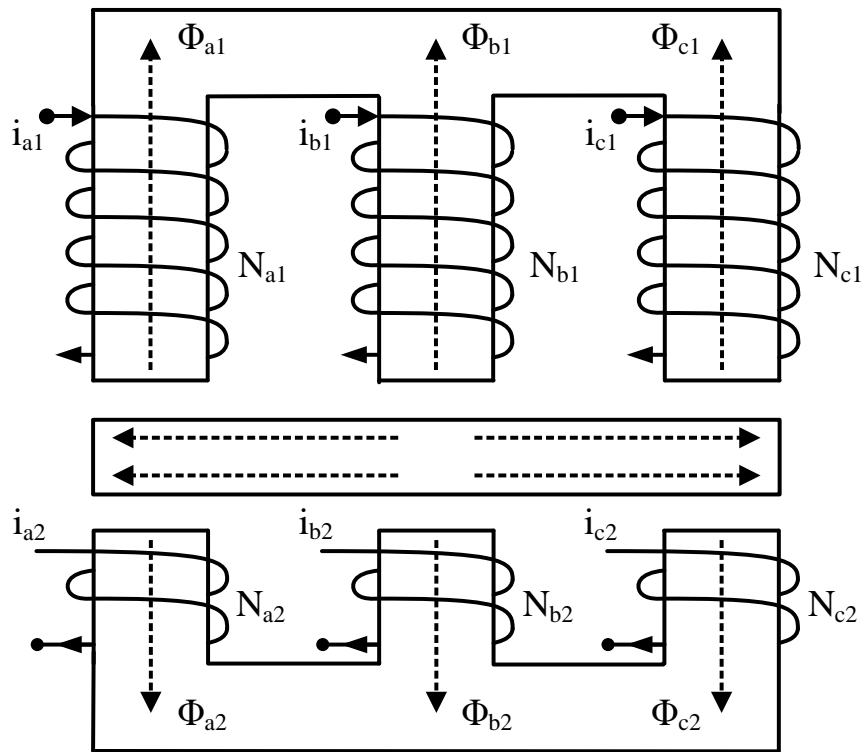


Figure 3. 59. Negatively coupled three phase filter inductor configurations

A set of equations explaining the coupling effect between the inductors of the same phase in a fully coupled three phase inductor becomes:

$$V_{la1} = R_{la1}i_{a1} + L_{s1aa}\frac{di_{a1}}{dt} + L_{m1ab}\frac{di_{b1}}{dt} + L_{m1ac}\frac{di_{c1}}{dt} + L_{Maa}\frac{di_{a2}}{dt} + L_{Mab}\frac{di_{b2}}{dt} + L_{Mac}\frac{di_{c2}}{dt} \quad (3.95.)$$

$$V_{lb1} = R_{lb1}i_{b1} + L_{m1ba}\frac{di_{a1}}{dt} + L_{s1bb}\frac{di_{b1}}{dt} + L_{m1bc}\frac{di_{c1}}{dt} + L_{Mba}\frac{di_{a2}}{dt} + L_{Mbb}\frac{di_{b2}}{dt} + L_{Mbc}\frac{di_{c2}}{dt} \quad (3.96.)$$

$$V_{lc1} = R_{lc1}i_{c1} + L_{m1ca}\frac{di_{a1}}{dt} + L_{m1cb}\frac{di_{b1}}{dt} + L_{s1cc}\frac{di_{c1}}{dt} + L_{Mca}\frac{di_{a2}}{dt} + L_{Mcb}\frac{di_{b2}}{dt} + L_{Mcc}\frac{di_{c2}}{dt} \quad (3.97.)$$

$$V_{la2} = R_{la2}i_{a2} + L_{Maa}\frac{di_{a1}}{dt} + L_{Mab}\frac{di_{b1}}{dt} + L_{Mac}\frac{di_{c1}}{dt} + L_{s2aa}\frac{di_{a2}}{dt} + L_{m2ab}\frac{di_{b2}}{dt} + L_{m2ac}\frac{di_{c2}}{dt} \quad (3.98.)$$

$$V_{lb2} = R_{lb2}i_{b2} + L_{Mba}\frac{di_{a1}}{dt} + L_{Mbb}\frac{di_{b1}}{dt} + L_{Mbc}\frac{di_{c1}}{dt} + L_{m2ba}\frac{di_{a2}}{dt} + L_{s2bb}\frac{di_{b2}}{dt} + L_{m2bc}\frac{di_{c2}}{dt} \quad (3.99.)$$

$$V_{lc2} = R_{lc2}i_{c2} + L_{Mca}\frac{di_{a1}}{dt} + L_{Mcb}\frac{di_{b1}}{dt} + L_{Mcc}\frac{di_{c1}}{dt} + L_{m2ca}\frac{di_{a2}}{dt} + L_{m2cb}\frac{di_{b2}}{dt} + L_{s2cc}\frac{di_{c2}}{dt} \quad (3.100.)$$

The mutual inductance between the two coils of the same phase L_{Mxx} can be expressed in terms of the self-inductance of each of the coils L_{s1xx} and L_{s2xx} and the amount of inductive coupling between the coils expressed via coefficient of coupling K , and its sign representing either positive or negative coupling between the coils:

$$L_{Mxx} = K\sqrt{L_{s1xx}L_{s2xx}} \quad (3.101.)$$

In a typical fully coupled three phase inductor configuration, like the one shown in figure 3, coupling (mutual) inductance between the two inductors of the different phase L_{Mxy} represents a fraction of the coupling (mutual) inductance between the two inductors of the same phase L_{Mxx} , so a same coupling factor k , as in phase coupling case is considered. Also, since the effects from the couplings are such that the flux produced in each phase acts subtractive on other phases, the sign in of coupling coefficient is negative:

$$L_{Mxy} = kL_{Mxx} \quad (3.102)$$

Magnetic circuit models shown in figure 3.60. and figure 3.61. represent positively and negatively coupled three phase inductors.

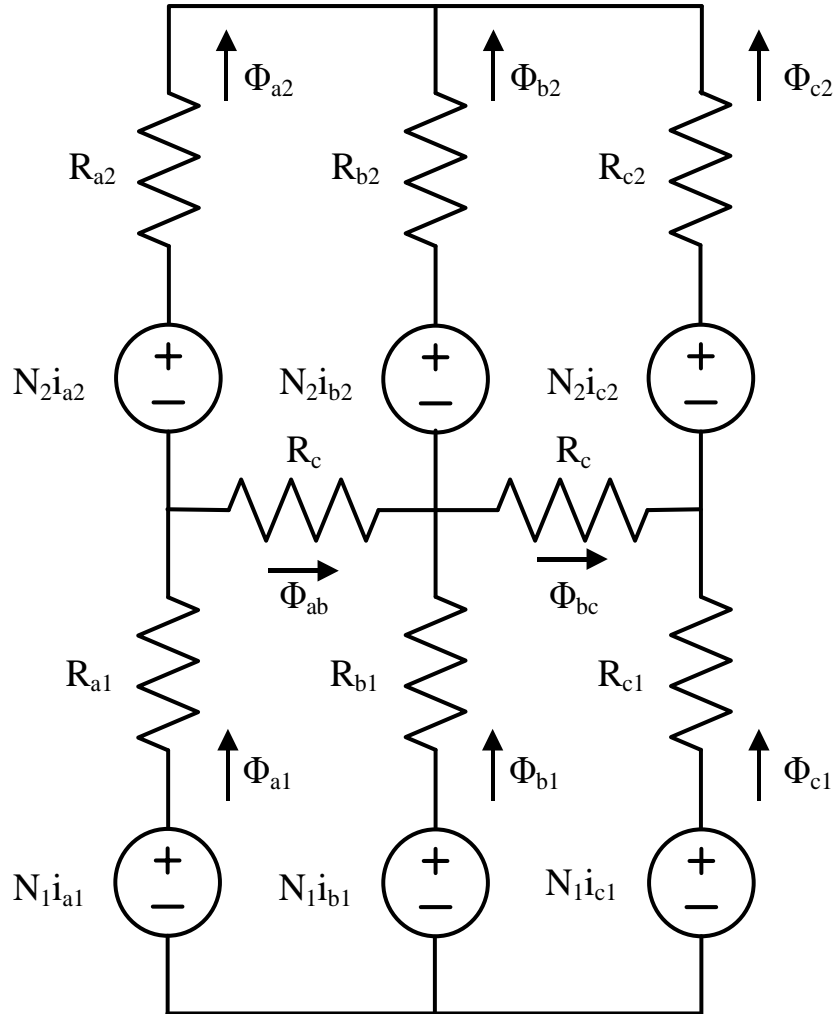


Figure 3. 60. Equivalent magnetic circuit model for positively coupled three phase inductors

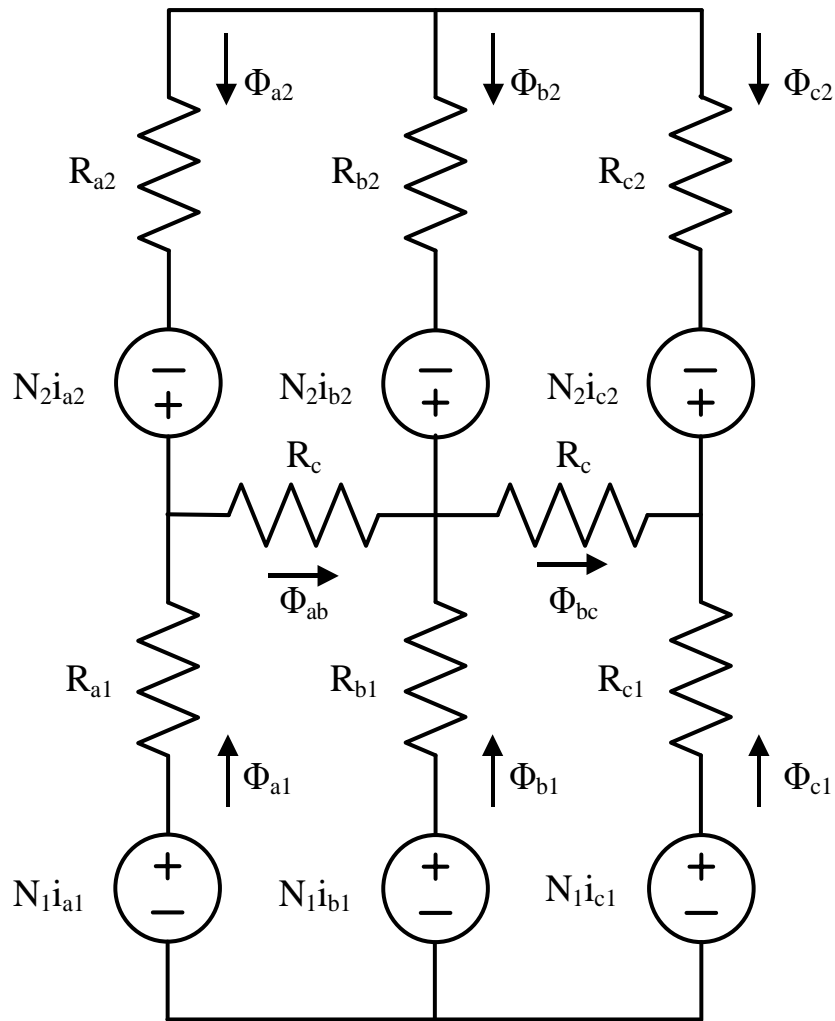


Figure 3. 61. Equivalent magnetic circuit model for negatively coupled three phase inductors

In order to simplify derivation process, couple of assumptions need to be made. Firstly, inductor is treated as ideal, meaning stray inductances are ignored. Secondly, reluctance of the common yoke is significantly lower than the reluctance of the limb, thus allowing it to be neglected in certain portions of the equations.

A set of differential equations describing magnetic circuit are:

$$V_{a1} = N_1 \frac{d\Phi_{a1}}{dt} \quad (3.103.)$$

$$V_{b1} = N_1 \frac{d\Phi_{b1}}{dt} \quad (3.104.)$$

$$V_{c1} = N_1 \frac{d\Phi_{c1}}{dt} \quad (3.105.)$$

$$V_{a2} = N_2 \frac{d\Phi_{a2}}{dt} \quad (3.106.)$$

$$V_{b2} = N_2 \frac{d\Phi_{b2}}{dt} \quad (3.107.)$$

$$V_{c2} = N_2 \frac{d\Phi_{c2}}{dt} \quad (3.108.)$$

Flux equations for each of the magnetic branches are:

$$\Phi_{a1} = \frac{1}{\frac{3}{2}(R_1R_2 + R_1R_c + R_2R_c)} (N_1i_{a1}\left(R_c + \frac{3}{2}R_2\right) + N_1i_{b1}k\left(R_c + \frac{3}{2}R_2\right) + N_1i_{c1}k\left(R_c + \frac{3}{2}R_2\right)) \pm (N_2i_{a2}R_c + kN_2i_{b2}R_c + kN_2i_{c2}R_c) \quad (3.109.)$$

$$\Phi_{b1} = \frac{1}{\frac{3}{2}(R_1R_2 + R_1R_c + R_2R_c)} (N_1i_{a1}\left(R_c + \frac{3}{2}R_2\right) + N_1i_{b1}k\left(R_c + \frac{3}{2}R_2\right) + N_1i_{c1}k\left(R_c + \frac{3}{2}R_2\right)) \pm (N_2i_{a2}R_c + kN_2i_{b2}R_c + kN_2i_{c2}R_c) \quad (3.110.)$$

$$\Phi_{c1} = \frac{1}{\frac{3}{2}(R_1R_2 + R_1R_c + R_2R_c)} (N_1i_{a1}\left(R_c + \frac{3}{2}R_2\right) + N_1i_{b1}k\left(R_c + \frac{3}{2}R_2\right) + N_1i_{c1}k\left(R_c + \frac{3}{2}R_2\right)) \pm (N_2i_{a2}R_c + kN_2i_{b2}R_c + kN_2i_{c2}R_c) \quad (3.111.)$$

$$\Phi_{a2} = \frac{1}{\frac{3}{2}(R_1R_2 + R_1R_c + R_2R_c)} \pm (N_1i_{a1}R_c + kN_1i_{b1}R_c + kN_1i_{c1}R_c) + \left(N_2i_{a2}\left(R_c + \frac{3}{2}R_1\right) + kN_2i_{b2}\left(R_c + \frac{3}{2}R_1\right) + kN_2i_{c2}\left(R_c + \frac{3}{2}R_1\right)\right) \quad (3.112.)$$

$$\Phi_{b2} = \frac{1}{\frac{3}{2}(R_1R_2 + R_1R_c + R_2R_c)} \pm (N_1i_{a1}R_c + kN_1i_{b1}R_c + kN_1i_{c1}R_c) \\ + \left(N_2i_{a2}\left(R_c + \frac{3}{2}R_1\right) + kN_2i_{b2}\left(R_c + \frac{3}{2}R_1\right) + kN_2i_{c2}\left(R_c + \frac{3}{2}R_1\right) \right) \quad (3.113.)$$

$$\Phi_{c2} = \frac{1}{\frac{3}{2}(R_1R_2 + R_1R_c + R_2R_c)} \pm (N_1i_{a1}R_c + kN_1i_{b1}R_c + kN_1i_{c1}R_c) \\ + \left(N_2i_{a2}\left(R_c + \frac{3}{2}R_1\right) + kN_2i_{b2}\left(R_c + \frac{3}{2}R_1\right) + kN_2i_{c2}\left(R_c + \frac{3}{2}R_1\right) \right) \quad (3.114.)$$

Self and mutual inductances in magnetic circuit are:

$$L_{s1} = N_1^2 \frac{R_c + \frac{3}{2}R_2}{\frac{3}{2}(R_1R_2 + R_1R_c + R_2R_c)} \quad (3.115.)$$

$$L_{s2} = N_2^2 \frac{R_c + \frac{3}{2}R_2}{\frac{3}{2}(R_1R_2 + R_1R_c + R_2R_c)} \quad (3.116.)$$

$$L_{Mxx} = \pm N_1N_2 \frac{R_c}{\frac{3}{2}(R_1R_2 + R_1R_c + R_2R_c)} \quad (3.117.)$$

$$L_{Mxy} = \pm N_1N_2k \frac{R_c}{\frac{3}{2}(R_1R_2 + R_1R_c + R_2R_c)} \quad (3.118.)$$

$$L_{Mxy1} = \pm N_1^2k \frac{R_c + \frac{3}{2}R_2}{\frac{3}{2}(R_1R_2 + R_1R_c + R_2R_c)} \quad (3.119.)$$

$$L_{Mxy2} = \pm N_2^2k \frac{R_c + \frac{3}{2}R_1}{\frac{3}{2}(R_1R_2 + R_1R_c + R_2R_c)} \quad (3.120.)$$

Coupling factors K and k are derived as:

$$K = \frac{L_{Mxx}}{\sqrt{L_{s1}L_{s2}}} = \frac{R_c}{\sqrt{\left(R_c + \frac{3}{2}R_1\right)\left(R_c + \frac{3}{2}R_2\right)}} \quad (3.121.)$$

$$k = \frac{L_{Mxy}}{L_{Mxx}} = \frac{L_{Mxy1}}{L_{s1}} = \frac{L_{Mxy2}}{L_{s2}} \quad (3.122.)$$

Assuming the total symmetry between all three phases in terms of number of winding turns, core and airgap design, equivalent total flux and inductance per phase can be calculated as:

$$\Phi_{a1} \approx N_1 \frac{i_{a1} (1 - k)}{R_1 \frac{3}{2}} \quad (3.123.)$$

$$\Phi_{a2} \approx N_2 \frac{i_{a2} (1 - k)}{R_2 \frac{3}{2}} \quad (3.124.)$$

$$L_{a1} = \frac{N_1^2 (1 - k)}{R_1 \frac{3}{2}} \quad (3.125.)$$

$$L_{a2} = \frac{N_2^2 (1 - k)}{R_2 \frac{3}{2}} \quad (3.126.)$$

It is obvious that great similarity exists between coupled single phase and coupled three phase inductors. However, one major difference exists between two cases. For cases where higher levels of inductor coupling factor K are required, reluctance of the common yoke becomes high enough that it causes asymmetry between the fluxes in middle vs the outer two limbs. That leads to different value of coupling factor k between phases. Negatively coupled inductor with 6.5% coupling tuned for 4.14 kHz trap frequency, similar to single phase version shown in figure 3.37, would be one such case. In

order to avoid that, a middle limb can be designed to have higher reluctance than the other two phases such that:

$$R_{1middle} = R_{1side} + R_c \quad (3.127.)$$

$$R_{2middle} = R_{2side} + R_c \quad (3.128.)$$

For the positively coupled inductor case, lower coupling factor K is required, so asymmetry between phases does not exist. That allows to use three phase positively coupled inductor in a same manner as the single phase inductor, but even with more material savings due to integration on a single vs three separate cores.

Considering the corresponding coupling coefficient k between the phases of each filter inductor to be the same $k_1 = k_2 = k$, three phase filter is represented by a following linear state space model:

$$\frac{d}{dt} \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \\ i_{2a} \\ i_{2b} \\ i_{2c} \\ V_{fab} \\ V_{fbc} \\ V_{fca} \end{bmatrix} = A \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \\ i_{2a} \\ i_{2b} \\ i_{2c} \\ V_{fab} \\ V_{fbc} \\ V_{fca} \end{bmatrix} + B \begin{bmatrix} E_{agt} \\ E_{bgt} \\ E_{cgt} \\ E_{ai} \\ E_{bi} \\ E_{ci} \end{bmatrix} \quad (3.129.)$$

Where:

$$A = \begin{bmatrix} -a & 0 & 0 & e & 0 & 0 & -f & 0 & f \\ 0 & -a & 0 & 0 & e & 0 & f & -f & 0 \\ 0 & 0 & -a & 0 & 0 & e & 0 & f & -f \\ b & 0 & 0 & -d & 0 & 0 & g & 0 & -f \\ 0 & b & 0 & 0 & -d & 0 & -g & g & 0 \\ 0 & 0 & b & 0 & 0 & -d & 0 & -g & g \\ c & -c & 0 & -c & c & 0 & 0 & 0 & 0 \\ 0 & c & -c & 0 & -c & c & 0 & 0 & 0 \\ -c & 0 & c & c & 0 & -c & 0 & 0 & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} h & 0 & 0 & j & 0 & 0 \\ 0 & h & 0 & 0 & j & 0 \\ 0 & 0 & h & 0 & 0 & j \\ -i & 0 & 0 & -h & 0 & 0 \\ 0 & -i & 0 & 0 & -h & 0 \\ 0 & 0 & -i & 0 & 0 & -h \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Where:

$$a = \frac{3L_2R_1 + (L_2(1 + \frac{Lg}{1-k}) + L_M)R_c}{3(1-k)(L_1L_2(1 + \frac{Lg}{1-k}) - L_M^2)}$$

$$b = \frac{3L_MR_1 + (L_1 + L_M)R_c}{3(1-k)(L_1L_2(1 + \frac{Lg}{1-k}) - L_M^2)}$$

$$c = \frac{1}{3C_f}$$

$$d = \frac{3L_MR_2 + (L_1 + L_M)R_c}{3(1-k)(L_1L_2(1 + \frac{Lg}{1-k}) - L_M^2)}$$

$$e = \frac{3L_MR_2 + (L_2(1 + \frac{Lg}{1-k}) + L_M)R_c}{3(1-k)(L_1L_2(1 + \frac{Lg}{1-k}) + L_M)R_c - L_M^2}$$

$$f = \frac{L_2(1 + \frac{Lg}{1-k}) + L_M}{3(1-k)(L_1L_2(1 + \frac{Lg}{1-k}) - L_M^2)}$$

$$g = \frac{L_1 + L_M}{3(1-k)(L_1L_2(1 + \frac{Lg}{1-k}) - L_M^2)}$$

$$h = \frac{L_M}{(1-k)(L_1L_2(1 + \frac{Lg}{1-k}) - L_M^2)}$$

$$i = \frac{L_1}{(1-k)(L_1L_2(1 + \frac{Lg}{1-k}) - L_M^2)}$$

$$j = \frac{L_2(1 + \frac{Lg}{1-k})}{(1-k)(L_1L_2(1 + \frac{Lg}{1-k}) - L_M^2)}$$

3.3.3. Three phase model in dqo rotational reference frame

The dqo (direct-quadrature-zero) transformation is a tensor that rotates the reference frame of a three-element vector or a three-by-three element matrix in an effort to simplify mathematical analysis. The goal of transformation is to rotate the reference frames of ac waveforms such that they become dc signals [13, 14, 15, 16]. That way simplified calculations can then be carried out, before performing the inverse transformation to recover the actual three-phase ac results. In grid tie inverter applications, dqo transformation represents a common method used in order to simplify calculations for the control of three-phase inverters [14, 17, 18]. Using DC signals is practical since rotational frame regulators can achieve zero steady-state error just by using a simple proportional-integral (PI) control [17, 19, 20]. Also, transmission of DC parameters needs lower communication bandwidth which is a preference for higher level of control.

In order to migrate into a rotational reference frame and back, a following transformation matrix and its inverse will be used:

$$T = \frac{2}{3} \begin{bmatrix} \cos(\delta) & \cos(\delta - \frac{2\pi}{3}) & \cos(\delta - \frac{4\pi}{3}) \\ \sin(\delta) & \sin(\delta - \frac{2\pi}{3}) & \sin(\delta - \frac{4\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (3.130.)$$

$$T^{-1} = \begin{bmatrix} \cos(\delta) & \sin(\delta) & 1 \\ \cos(\delta - \frac{2\pi}{3}) & \sin(\delta - \frac{2\pi}{3}) & 1 \\ \cos(\delta - \frac{4\pi}{3}) & \sin(\delta - \frac{4\pi}{3}) & 1 \end{bmatrix} \quad (3.131.)$$

Where:

$$X_{dqo} = TX_{abc}$$

$$X_{abc} = T^{-1}X_{dqo}$$

Out of the many different variations of dqo transformations, this particular one preserves the same magnitudes in either reference frame, is power invariant, and uses the vector sequence represented as shown in figure 3.62.:

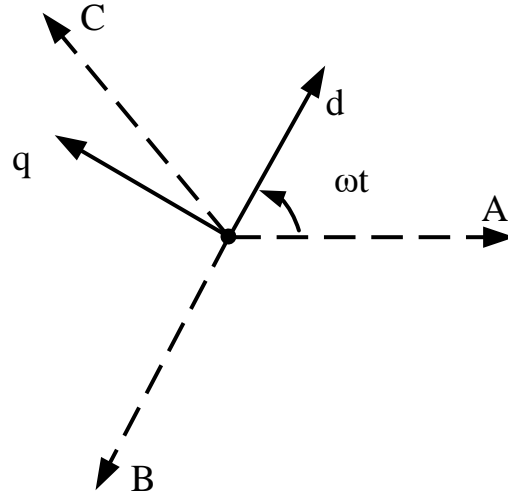


Figure 3. 62. Combined vector representation for dqo transformation

In order to derive a model for a filter in the rotational dqo frame, we are starting from a linear state space model in stationary abc frame derived in chapter 3.3.2:

$$\frac{d}{dt} \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \\ i_{2a} \\ i_{2b} \\ i_{2c} \\ V_{fab} \\ V_{fbc} \\ V_{fca} \end{bmatrix} = A \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \\ i_{2a} \\ i_{2b} \\ i_{2c} \\ V_{fab} \\ V_{fbc} \\ V_{fca} \end{bmatrix} + B \begin{bmatrix} E_{agt} \\ E_{bgt} \\ E_{cgt} \\ E_{ai} \\ E_{bi} \\ E_{ci} \end{bmatrix} \quad (3.132.)$$

Using a reference frame matrix transformation, the equation becomes:

$$\frac{d}{dt} \left(T_1^{-1} T_1 \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \\ i_{2a} \\ i_{2b} \\ i_{2c} \\ V_{fab} \\ V_{fbc} \\ V_{fca} \end{bmatrix} \right) = AT_1^{-1} T_1 \begin{bmatrix} i_{1a} \\ i_{1b} \\ i_{1c} \\ i_{2a} \\ i_{2b} \\ i_{2c} \\ V_{fab} \\ V_{fbc} \\ V_{fca} \end{bmatrix} + BT_2^{-1} T_2 \begin{bmatrix} E_{agt} \\ E_{bgt} \\ E_{cgt} \\ E_{ai} \\ E_{bi} \\ E_{ci} \end{bmatrix} \quad (3.133.)$$

Where:

T_1

$$= \frac{2}{3} \begin{bmatrix} \cos(\delta) & \cos(\delta - \frac{2\pi}{3}) & \cos(\delta - \frac{4\pi}{3}) & 0 & 0 & 0 & 0 & 0 & 0 \\ \sin(\delta) & \sin(\delta - \frac{2\pi}{3}) & \sin(\delta - \frac{4\pi}{3}) & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \cos(\delta) & \cos(\delta - \frac{2\pi}{3}) & \cos(\delta - \frac{4\pi}{3}) & 0 & 0 & 0 \\ 0 & 0 & 0 & \sin(\delta) & \sin(\delta - \frac{2\pi}{3}) & \sin(\delta - \frac{4\pi}{3}) & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \cos(\delta) & \cos(\delta - \frac{2\pi}{3}) & \cos(\delta - \frac{4\pi}{3}) \\ 0 & 0 & 0 & 0 & 0 & 0 & \sin(\delta) & \sin(\delta - \frac{2\pi}{3}) & \sin(\delta - \frac{4\pi}{3}) \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$

$$T_1^{-1} = \begin{bmatrix} \cos(\delta) & \sin(\delta) & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ \cos(\delta - \frac{2\pi}{3}) & \sin(\delta - \frac{2\pi}{3}) & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ \cos(\delta - \frac{4\pi}{3}) & \sin(\delta - \frac{4\pi}{3}) & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \cos(\delta) & \sin(\delta) & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \cos(\delta - \frac{2\pi}{3}) & \sin(\delta - \frac{2\pi}{3}) & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \cos(\delta - \frac{4\pi}{3}) & \sin(\delta - \frac{4\pi}{3}) & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \cos(\delta) & \sin(\delta) & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & \cos(\delta - \frac{2\pi}{3}) & \sin(\delta - \frac{2\pi}{3}) & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & \cos(\delta - \frac{4\pi}{3}) & \sin(\delta - \frac{4\pi}{3}) & 1 \end{bmatrix}$$

$$T_2 = \frac{2}{3} \begin{bmatrix} \cos(\delta) & \cos(\delta - \frac{2\pi}{3}) & \cos(\delta - \frac{4\pi}{3}) & 0 & 0 & 0 \\ \sin(\delta) & \sin(\delta - \frac{2\pi}{3}) & \sin(\delta - \frac{4\pi}{3}) & 0 & 0 & 0 \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & 0 & 0 & 0 \\ 0 & 0 & 0 & \cos(\delta) & \cos(\delta - \frac{2\pi}{3}) & \cos(\delta - \frac{4\pi}{3}) \\ 0 & 0 & 0 & \sin(\delta) & \sin(\delta - \frac{2\pi}{3}) & \sin(\delta - \frac{4\pi}{3}) \\ 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$

$$T_2^{-1} = \begin{bmatrix} \cos(\delta) & \sin(\delta) & 1 & 0 & 0 & 0 \\ \cos(\delta - \frac{2\pi}{3}) & \sin(\delta - \frac{2\pi}{3}) & 1 & 0 & 0 & 0 \\ \cos(\delta - \frac{4\pi}{3}) & \sin(\delta - \frac{4\pi}{3}) & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \cos(\delta) & \sin(\delta) & 1 \\ 0 & 0 & 0 & \cos(\delta - \frac{2\pi}{3}) & \sin(\delta - \frac{2\pi}{3}) & 1 \\ 0 & 0 & 0 & \cos(\delta - \frac{4\pi}{3}) & \sin(\delta - \frac{4\pi}{3}) & 1 \end{bmatrix}$$

After performing derivation operation on the left side of the state equation, the equation becomes:

$$\frac{d}{dt} T_1^{-1} \begin{bmatrix} i_{1d} \\ i_{1q} \\ i_{1o} \\ i_{2d} \\ i_{2q} \\ i_{2o} \\ V_{cd} \\ V_{cq} \\ V_{co} \end{bmatrix} + T_1^{-1} \frac{d}{dt} \begin{bmatrix} i_{1d} \\ i_{1q} \\ i_{1o} \\ i_{2d} \\ i_{2q} \\ i_{2o} \\ V_{cd} \\ V_{cq} \\ V_{co} \end{bmatrix} = A T_1^{-1} \begin{bmatrix} i_{1d} \\ i_{1q} \\ i_{1o} \\ i_{2d} \\ i_{2q} \\ i_{2o} \\ V_{cd} \\ V_{cq} \\ V_{co} \end{bmatrix} + B T_2^{-1} \begin{bmatrix} E_{dgt} \\ E_{qgt} \\ E_{ogt} \\ E_{di} \\ E_{qi} \\ E_{oi} \end{bmatrix} \quad (3.134.)$$

Where:

$$\frac{d}{dt} T_1^{-1} = \begin{bmatrix} -\omega \sin(\delta) & \omega \cos(\delta) & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\omega \sin(\delta - \frac{2\pi}{3}) & \omega \cos(\delta - \frac{2\pi}{3}) & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\omega \sin(\delta - \frac{4\pi}{3}) & \omega \cos(\delta - \frac{4\pi}{3}) & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\omega \sin(\delta) & \omega \cos(\delta) & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\omega \sin(\delta - \frac{2\pi}{3}) & \omega \cos(\delta - \frac{2\pi}{3}) & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\omega \sin(\delta - \frac{4\pi}{3}) & \omega \cos(\delta - \frac{4\pi}{3}) & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\omega \sin(\delta) & \omega \cos(\delta) & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\omega \sin(\delta - \frac{2\pi}{3}) & \omega \cos(\delta - \frac{2\pi}{3}) & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\omega \sin(\delta - \frac{4\pi}{3}) & \omega \cos(\delta - \frac{4\pi}{3}) & 0 \end{bmatrix}$$

By rearranging and multiplying with T1 from the left side, the final equation state space model in rotational dqo frame becomes:

$$\frac{d}{dt} \begin{bmatrix} i_{1d} \\ i_{1q} \\ i_{1o} \\ i_{2d} \\ i_{2q} \\ i_{2o} \\ V_{cd} \\ V_{cq} \\ V_{co} \end{bmatrix} = A_1 \begin{bmatrix} i_{1d} \\ i_{1q} \\ i_{1o} \\ i_{2d} \\ i_{2q} \\ i_{2o} \\ V_{cd} \\ V_{cq} \\ V_{co} \end{bmatrix} + B \begin{bmatrix} E_{dgt} \\ E_{qgt} \\ E_{ogt} \\ E_{di} \\ E_{qi} \\ E_{oi} \end{bmatrix} \quad (3.135.)$$

Where in the most complex case of a fully coupled filter inductor and delta connected capacitors, matrices A and B become:

$$A_1 = \begin{bmatrix} -a & -\omega & 0 & e & 0 & 0 & -f & 0 & f \\ \omega & -a & 0 & 0 & e & 0 & f & -f & 0 \\ 0 & 0 & -a & 0 & 0 & e & 0 & f & -f \\ b & 0 & 0 & -d & -\omega & 0 & g & 0 & -f \\ 0 & b & 0 & \omega & -d & 0 & -g & g & 0 \\ 0 & 0 & b & 0 & 0 & -d & 0 & -g & g \\ c & -c & 0 & -c & c & 0 & 0 & -\omega & 0 \\ 0 & c & -c & 0 & -c & c & \omega & 0 & 0 \\ -c & 0 & c & c & 0 & -c & 0 & 0 & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} h & 0 & 0 & j & 0 & 0 \\ 0 & h & 0 & 0 & j & 0 \\ 0 & 0 & h & 0 & 0 & j \\ -i & 0 & 0 & -h & 0 & 0 \\ 0 & -i & 0 & 0 & -h & 0 \\ 0 & 0 & -i & 0 & 0 & -h \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

By observing the state space models in stationary and rotational reference frame, except for the large dose of similarity, one major difference can be notified. Rotational reference frame produces cross coupling terms between d and q axis's, which did not exist between phases in

stationary frame. Cross coupling is present for all 3 states, and thus becomes a major challenge for control design.

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4. MTI Control Technique

4.1. PWM Modulator Model

Digital control provides possibilities of implementing complex control algorithms with consideration of tolerances, system non linearities and parameter variation thru tuning strategies and self-analysis, which would be impossible to implement in analog control design [1]. Digital controllers are very flexible, allowing easy modification of control strategy, without need for hardware modifications. As compared to analog controllers, digital ones are highly noise tolerant and do not experience thermal drifts and ageing effects. Also, digital controllers provide a more convenient interface used for monitoring and control. The microgrid tie inverter controller is structured hierarchically. The average output voltage of each phase is based on the state of each of the two switches in that lag. Switch state is determined by modulator in the lowest control level according to the modulation law. Modulator input is the set point for the load average voltage which is provided by a current controller. Current controller is found in the control level above the modulator and is responsible for providing the set point to the modulator. Based on previous, Microgrid tie inverter is said to operate in current control mode, thus basically turning a voltage source topology into a controlled current source. Similarly, the current controller set-point can be provided in the higher level of control by another control loop.

Rising Edge Sawtooth, Falling Edge Sawtooth and Double Edge Symmetric Triangular are three types of carrier signals commonly used in constant-frequency PWM modulation. Double-edge symmetric triangular modulation was shown to eliminate certain harmonics when sine wave signals are used as set points [2]. Therefore, symmetric triangular modulation has a performance advantage and is a preferred method in AC–DC converters. Further work will only focus on and

assume double edge symmetric triangular modulation method as part of the modulator analysis.

The triangular modulator principle of operation is shown in figure 4.1.

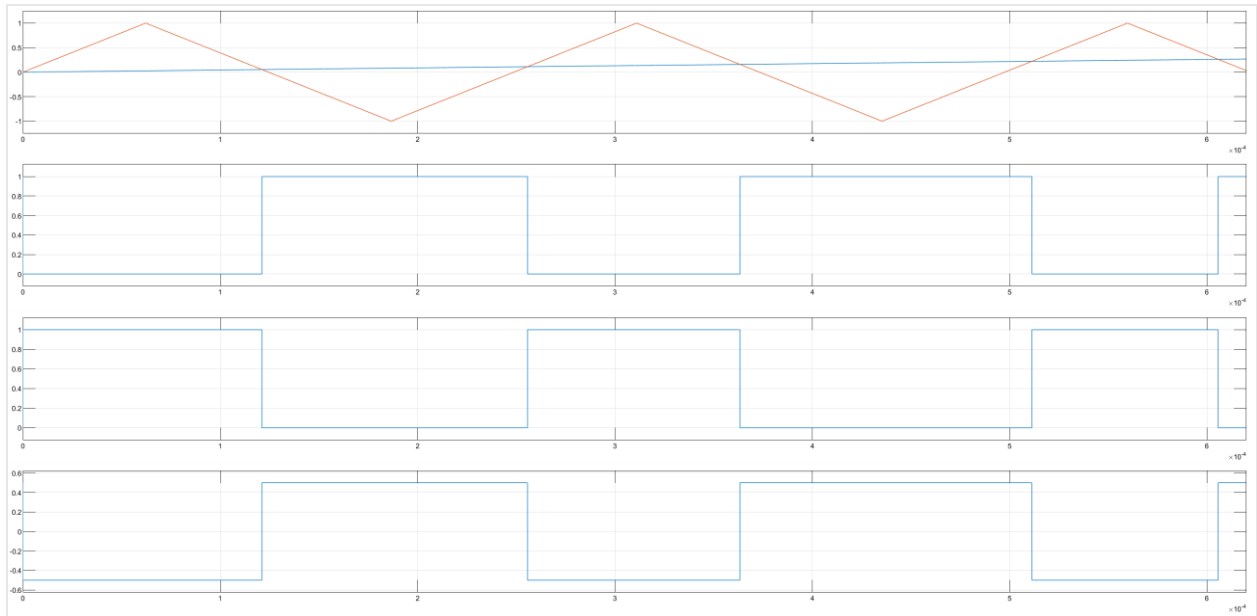


Figure 4. 1. Triangular PWM Modulator

As upper and lower switches are consecutively turning on, square wave voltage V_o is applied to the output with constant switching frequency $f_s = \frac{1}{T_s}$. T_s is the period of the carrier signal $c(t)$, as well as variable duty cycle d . Indirectly, duty cycle d is defined as the ratio between the time duration of $\frac{V_{dc}}{2}$ voltage on the output side and T_s . If we assume that modulating signal V_m is constant during each modulation period, the following equation holds:

$$\frac{V_m}{(2d - 1)T_s} = \frac{c_{pk}}{T_s} \Leftrightarrow d = 0.5 \left(1 + \frac{V_m}{c_{pk}} \right) \quad (4.1)$$

Also, relationship between the average output voltage and the duty cycle is calculated as:

$$\overline{V_o(d)} = \frac{1}{T_s} \int_t^{t+T_s} V_o(\tau) d\tau = \frac{1}{T_s} \left(T_s \frac{V_{dc}}{2} d - \frac{V_{dc}}{2} (1 - d) T_s \right) = \frac{V_{dc}}{2} (2d - 1) \quad (4.2.)$$

During each period T_s , modulation signal is never constant. However, if modulating signal changes slowly along time, with respect to the carrier signal, previous equation still holds, which has been mathematically shown in [3][4]. Since spectrum of modulating signal $V_m(t)$ is shifted and replicated along carrier frequency multiples by PWM process [2], a full reconstruction of a signal is possible as long as the bandwidth of the signal is limited. This means that the upper limit of $V_m(t)$ bandwidth is well below $\frac{1}{T_s}$ and that the information carried by the modulating signal is directly transferred to the duty-cycle by PWM process. This can be represented as:

$$\frac{\partial d}{\partial V_m} = \frac{1}{2c_{pk}} \quad (4.3.)$$

Following, the duty-cycle is transferred to the output voltage waveform by inverter. That implies that the average value of the output voltage will copy that of modulating signal $V_m(t)$ providing a formula for the modulator gain G_{pwm} as:

$$G_{pwm} = \frac{\partial V_o}{\partial d} \frac{\partial d}{\partial V_m} = \frac{V_{dc}}{2c_{pk}} \quad (4.4.)$$

Modulator gain G_{pwm} multiplied with previously derived inverter transfer function between input voltage and output current G_i represents dynamic relationship between small perturbation of modulation signal V_m and variation of output grid current I_2 .

It has been shown [2] that the frequency spectrum of the modulating signal $V_m(t)$ is shifted along frequency by the PWM process around all integer multiples of the carrier frequency.

This way the demodulation of signal $V_m(t)$ spectrum from the signal $V_o(t)$ can be easily achieved by low pass filtering $V_o(t)$, in the case modulating signal $V_m(t)$ is assumed to be limited in bandwidth.

In [5] it is demonstrated that analog (naturally sampled) implementation of PWM produces no phase lag between modulating signal and duty-cycle, concluding that the analog PWM modulator delay can always be considered negligible.

On the other hand, various digital implementations of the PWM modulator, due to sample-and-hold effects, introduce significant response delays that cannot be neglected [6].

Since modulating signal update in digital implementation is performed only at the beginning of each modulation period as per Figure 4.2, the simplest way to model it is by using a sample and hold equivalent as shown in Figure 4.3.

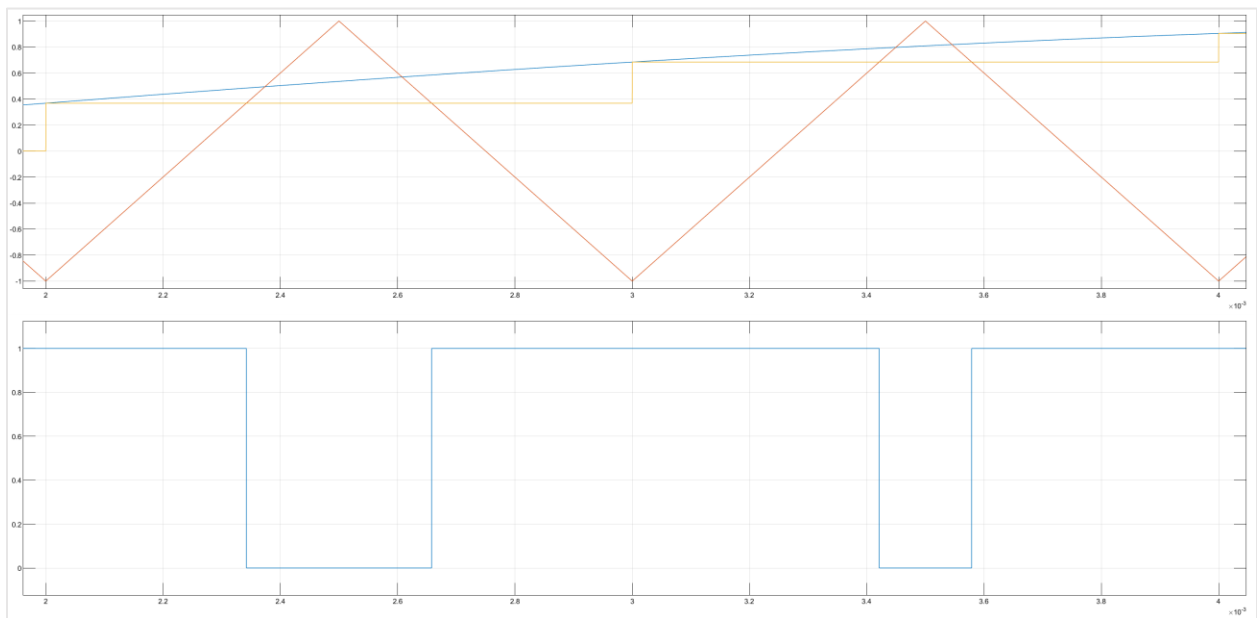


Figure 4. 2. Single sampled Symmetric Triangle PWM modulator

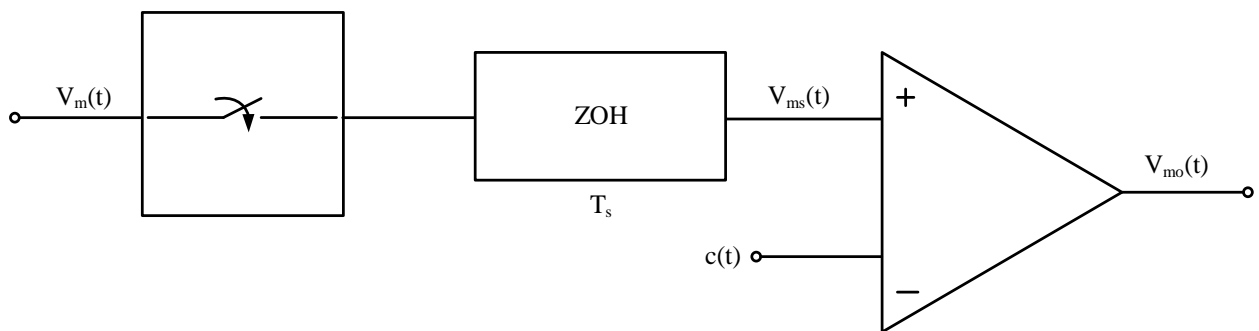


Figure 4. 3. Basic digital PWM modulator model

Due to the sample and hold effect, it is obvious that the modulator response to disturbance can only take place during the following modulation period. That introduces a delay that results in a dramatic difference in dynamic response of the digital modulator as compared to the analog modulator implementation.

If it is assumed that the bandwidth of the input signal is limited and below the Nyquist frequency, and if the output signal frequency content above the same frequency is neglected, based on [6], the transfer function between the modulator input and output signals is represented as:

$$G_{pwm}(s) = \frac{V_O(s)}{V_m(s)} = \frac{V_{dc}}{2c_{pk}} \left(e^{-s(1-d)\frac{T_s}{2}} + e^{-s(1+d)\frac{T_s}{2}} \right) \quad (4.5.)$$

By computing

$$\arg(|G_{pwm}(j\omega)|) = \arg\left(V_{dc} \frac{e^{-j\omega(1-d)\frac{T_s}{2}} + e^{-j\omega(1+d)\frac{T_s}{2}}}{2c_{pk}} \right) = -\omega \frac{T_s}{2} \quad (4.6.)$$

It is found that for the symmetric triangular modulation there is always a constant phase shift between the input and output signal that does not depend on the particular steady-state value of the duty-cycle, d , and is equal to half of the sampling period [7].

In order to somewhat compensate for the additional delay introduced by the uniformly sampled PWM [8], the double update mode of operation is most often used, and represents state of the art for modulators used in AC/DC converters. This way, duty cycle is updated at the beginning and at the half of each modulation period, as per Figure 4.4, which in absence of perturbations results in a stream of pulses that are symmetrically allocated within the modulation period.

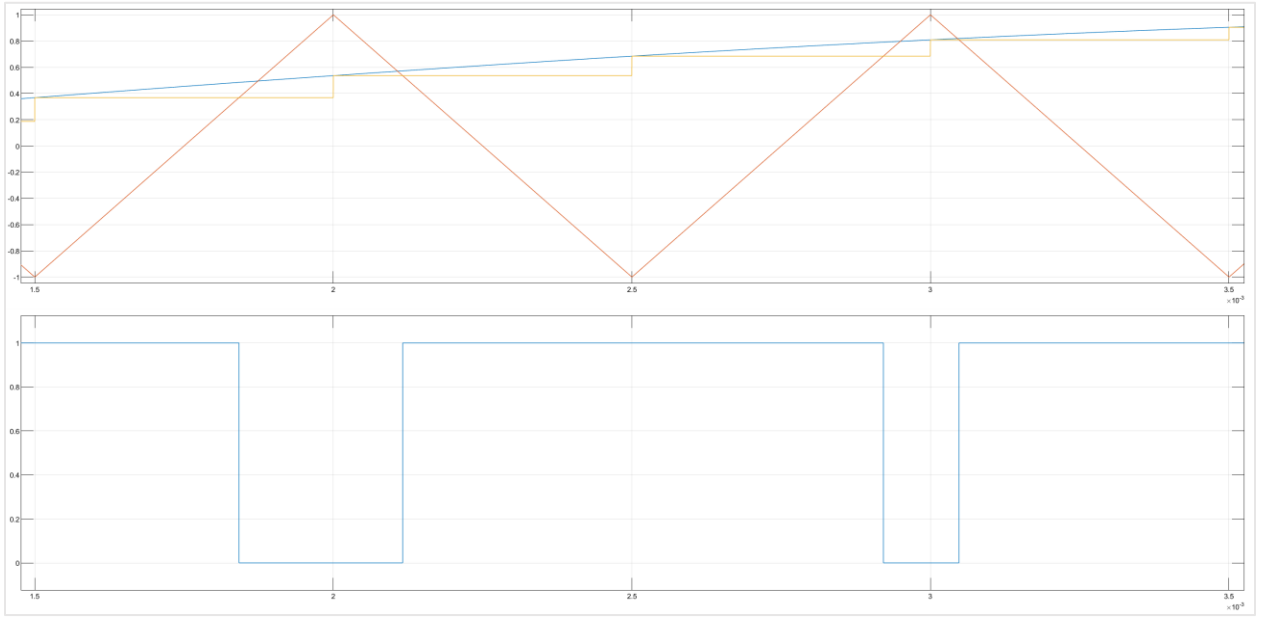


Figure 4. 4. Double sampled Symmetric Triangle PWM modulator

Assuming the same sampling period T_s , the transfer function $G_{pwm}(s)$ between the modulator input and output signal becomes:

$$G_{pwm}(s) = \frac{V_o(s)}{V_m(s)} = \frac{V_{dc}}{2c_{pk}} \left(e^{-sd\frac{T_s}{2}} + e^{-s(1-d)\frac{T_s}{2}} \right) \quad (4.7.)$$

Resulting in

$$\arg(|G_{pwm}(j\omega)|) = \arg\left(V_{dc} \frac{e^{-j\omega d\frac{T_s}{2}} + e^{-j\omega(1-d)\frac{T_s}{2}}}{2c_{pk}} \right) = -\omega \frac{T_s}{4} \quad (4.8.)$$

Which produces a half of the phase lag calculated for a single update mode [6].

In either case, regardless of whether the sampling frequency is set to one or two times the switching frequency, the Shannon's theorem conditions will be violated [9]. Shannon's theorem shows that there is an upper bound for the sampled signal bandwidth equal to a half of the sampling frequency, beyond which perfect signal reconstruction becomes impossible and aliasing

phenomena appear. Aliasing is an effect that causes different signals to become indistinguishable (or aliases of one another) when sampled.

However, despite using single or double sampling, aliasing phenomena is not present in these two cases due to proper synchronization between sampling and switching processes. By synchronization, aliasing phenomena results in reconstruction of the average value of the sampled signal [6] as shown in figure 4.5. for single phase PWM case. Basically, any time the sampling takes place in the middle of the switch on/off period or at both, it results in reconstruction of the average signal value, which is exactly what is needed for fundamental current feedback control.

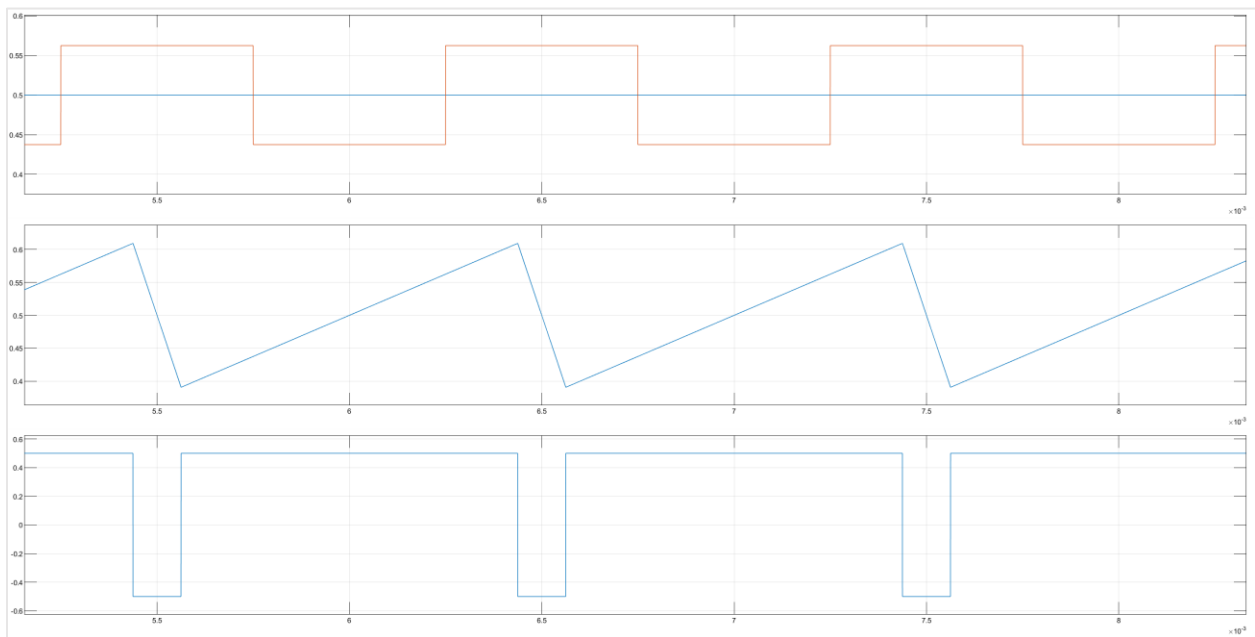


Figure 4. 5. Synchronization of PWM and sampling processes for single phase PWM.

In case of three phase PWM scheme, ripple current behaves differently, since current slope changes more than once during each PWM period, as per example in Figure 4.7. The reason for such kind of behavior is that current in one particular phase is dictated by switched line to line voltage waveforms occurring between that phase and other two phases across filter inductors, thus doubling the number of current transitions during one carrier period.

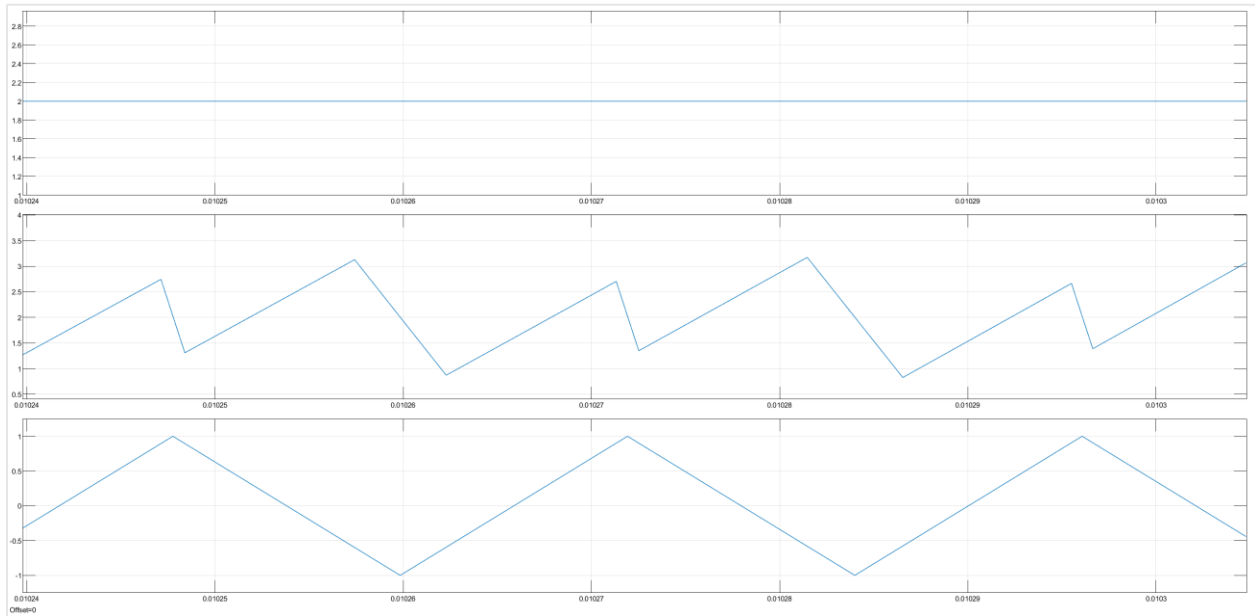


Figure 4. 6. Synchronization of PWM and sampling processes for three phase PWM.

However, Figure 4.6. clearly demonstrates that synchronization between sampling and switching processes still results in reconstruction of the average signal value in three phase PWM, same as for single phase PWM.

In case of microgrid tie inverter, where higher bandwidth and performance requirements exist, it is necessary to use multi sampling PWM implementation in order to reduce the phase lag effect produced by the sampling. In multi sampling, as number of samples per PWM period increases, the equivalent phase lag tends to zero, which matches a no delay case corresponding to naturally sampled implementation of the modulator. However, multi sampling introduces certain limitations like generation of deadbands and need for proper filtering of the switching noise. Multiple solutions have been proposed [10]-[14] on how to overcome the limitations and fully exploit the advantages of multi-sampling. Proposed solutions include processing input signals with low pass filters, moving average filters and selective filters as well as synchronization of the sampling process and the modulator to eliminate horizontal intersections.

Sampling of the modulating signal generates dead bands in the modulator trans characteristics [10] which have a negative effect on the system closed-loop operation, and will be further explained. As long as modulating signal and carrier intersection occurs under no transition of the modulating signal, the modulator gain is maximized for that operating point as in figure 4.7.(a). However, when modulating signal and carrier intersection occurs under vertical transition of modulating signal on one side as in Figure 5b, the local modulator gain is halved. The worst case scenario is when the intersection occurs under vertical transition on both sides as in Figure 5c, thus leading to local modulator gain becoming zero. This way any local variation in the modulating signal will not produce any change in the duty cycle.

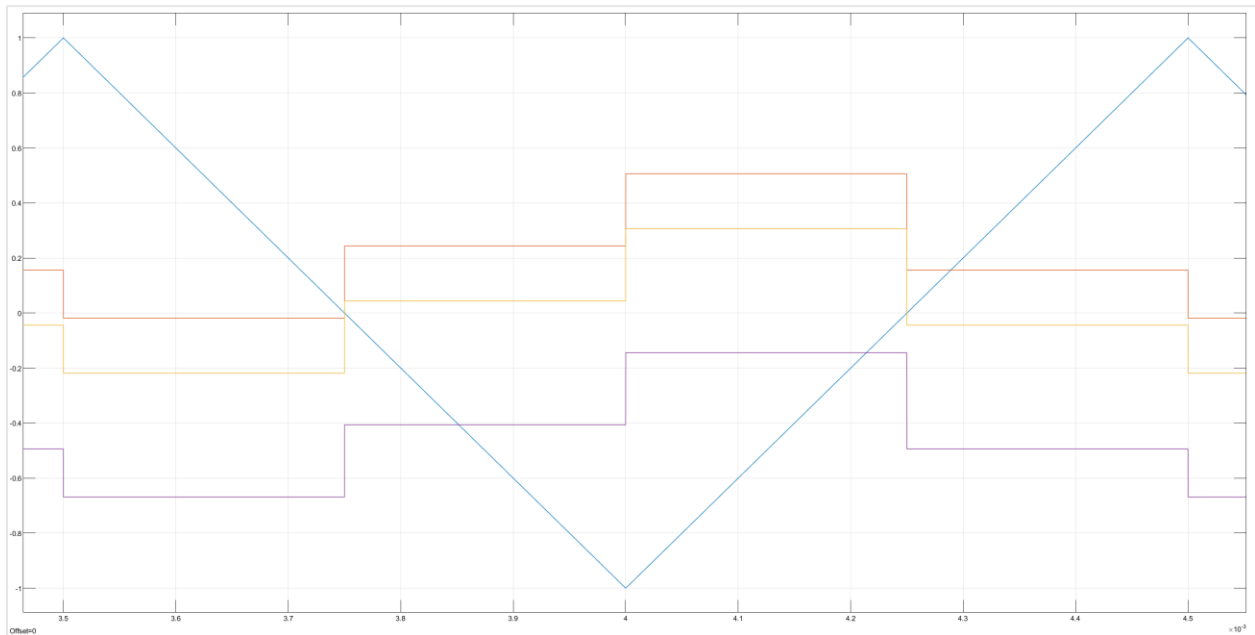


Figure 4. 7. Multisampled Modulator (a) No transition (b) Single vertical transition (c) Double vertical transition

Modulator trans characteristic, which represents duty cycle as an average value of the modulating signal, becomes distorted in presence of deadbands. Such created deadbands will produce harmonics in the output waveform, degrade the closed loop regulation performance and stability, and lead to oscillatory behavior. Modulator trans characteristic strongly depends on the

shape and amplitude of the modulating signal which is directly dependent on the ripple content of the measured feedback signal, the bandwidth of the controller, and the signal level. However, general rule is that higher sampling rates and lower modulation signal bandwidths result in lower distortion of the trans characteristic as compared to the ideal case.

4.2. Digital Control System Model

Digital control systems for inverter circuits are typically developed using microcontrollers (μ Cs), digital signal processors (DSPs), or field programmable gate arrays (FPGAs) with suitable peripheral circuits like analog to digital converter (ADCs) and PWM units, which are required by the system. Basic digital control system structure for microgrid tie inverter is represented in figure 4.8.

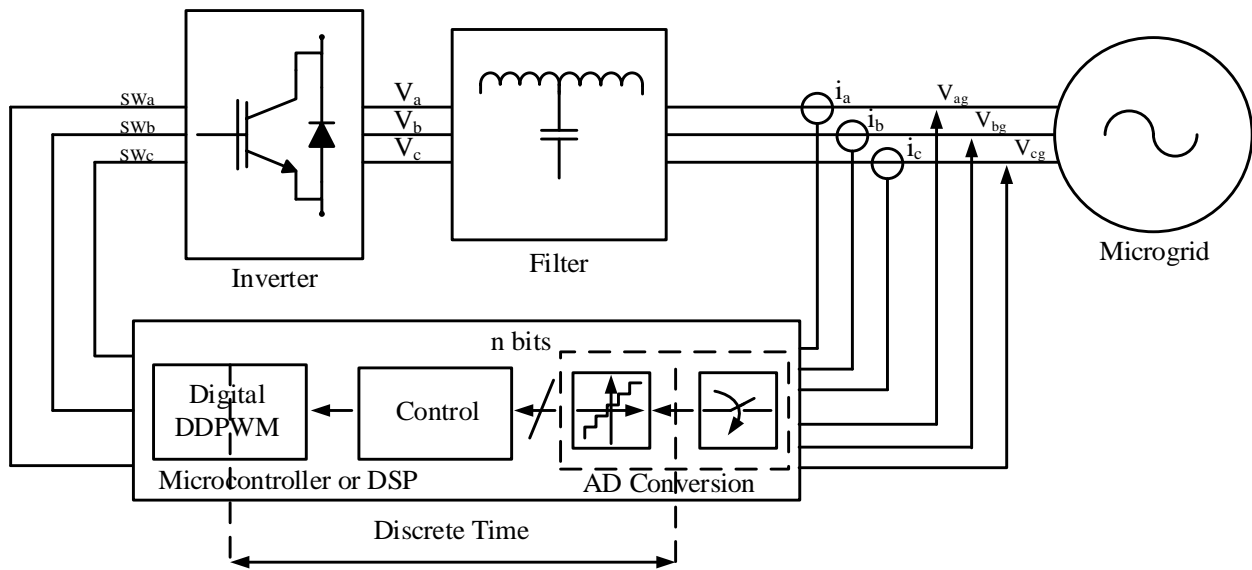


Figure 4. 8. Digital control system structure for Microgrid Tie Inverter

The data acquisition path for current feedback circuit is represented by a series connection of current sensor, current sensing feedback circuit and ADC for each phase. Also, similar data acquisition path exists for voltage feedback circuit that also consists of voltage sensing circuit and ADC. Multiple current and voltage feedback paths exist in parallel as part of the feedback circuit in a system. Sensing circuit has a role to properly scale and filter the current and voltage feedback signals. Analog to digital conversion process can be mathematically modelled as a series connection of an ideal sampler and a bit uniform quantizer. Ideal sampler has a function to model

the sampling process and its output as a stream of Dirac pulses at sampling instants, with amplitude matching that of the input signal. Quantizer has a function to model a transformation of the continuous amplitude signal into a discrete amplitude signal of a finite number of values. Discrete signal is represented as a multiplier of a quantization step Q , which represents a fundamental unit:

$$Q = \frac{FSR}{2^n} = LSB \quad (4.9.)$$

Where n is the ADC bit number, FSR represents the full scale range, in V and LSB is the least significant bit. Q represents the minimum variation of input signal that guarantees variation of at least one bit in the digital signal. Typical transcharacteristic of a uniform quantizer is shown in figure 4.9.

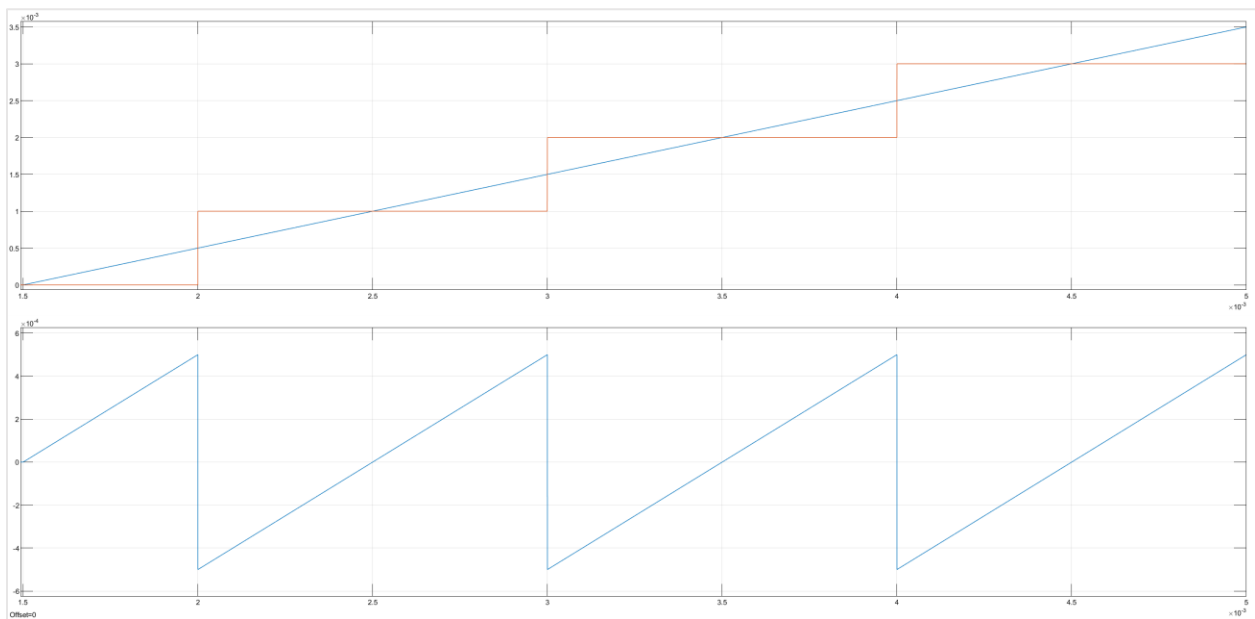


Figure 4. 9. Transcharacteristic of a uniform quantizer

Loss of information of the input signal due to analog to digital conversion is always present during quantization. Common approach in literature is to model it as an additive noise on top of the signal in order to analyze optimal resolution and signal to noise ratio. Since both sampler and quantizer are instantaneous functions, there is no impact on the dynamic behavior of the system.

Also in a typical power electronics application, quantization step is selected to be low enough, such that quantization error effect can be neglected. In order to ensure a reduction in negative effects related to quantization, full voltage range on the ADC input needs to be exploited. This way it is ensured that the maximum number of bits is utilized to internally represent a sampled signal, thus leading to better resolution. The number N_e of effective bits used for representation of the input signal samples is:

$$N_e = n - \text{floor} \left(\frac{\log_{10} \frac{FSR}{S_{pp}}}{\log_{10} 2} \right) \quad (4.10)$$

Where S_{pp} represents a voltage peak to peak amplitude of the feedback signal, FSR a full scale voltage range of ADC and n the total number of ADC bits. Voltage peak to peak amplitude of the feedback signal is typically set based on the maximum expected signal values for overcurrent and overvoltage conditions.

In order to properly define loop gains it is necessary to know a normalization factors, since normalization factors dictate different gains for ADC and PWM modulator. This work will assume a fractional internal representation of variables, meaning that the full scale ranges of the ADC and modulator are internally represented as unity. Fractional normalization has many implementation advantages, mostly related to the simplification of the controller design and prevention of multiplication induced overflow. In this case the ADC gain is indirectly set to $\frac{1}{FSR}$, since maximum input signal gets interpreted as unity. Also, PWM modulator gain becomes unity, since highest internally representable fraction is transformed into a unity duty-cycle. In case different normalization factor K is used, the equivalent gains for the ADC and the DDPWM have to be adjusted.

As can be seen in figure 4.8., both the controller and modulator blocks are inside the digital domain marked with the shaded area, that represents a Digital control system block. On the other hand, inverter power structure, current sensor and conditioning circuit models are continuous time models. The link between digital and continuous time domains is represented by the ideal sampler on the controller inputs and by the digital pulse width modulator as a controller output that implements holder function, which basically serves as an interpolator. In order to simplify controller design, digital controller can be designed based on the continuous time control by using controller discretization technique. Controller discretization is a technique that is widely used in power electronics applications by exploiting broad experience in continuous time control and requiring minimal knowledge of the digital control theory for successful implementation. The procedure calls for a satisfactory continuous time controller design that gets transformed later into a digital controller by using one of the several possible discretization methods. By using the appropriate continuous time models for modeling of the discretization process and equivalent loop delays, controller discretization technique implies very minor loss of precision as compared to direct digital design. The controller synthesis in continuous time requires to model the discrete time system in between the input ideal sampler and the output holder in continuous time domain. The most common way to do this is to pull a continuous controller model out and make a cascade connection of the ideal sampler, unit delay and the holder. After that the controller can be synthesized in the continuous time domain and converted back to discrete time in the original sampled data system and it will maintain the closed loop properties of the continuous time design. As derived in (4.6.) and (4.8.), by assuming a limited bandwidth of the modulation signal and unity gain for the modulator $c_{pk} = 1$, the dynamic model of the discrete PWM represents a delay behavior with half DC bus gain per (4.4). This discrete PWM block model assumes a zero order hold function to dynamically model the inherited interpolator function.

Also besides time delay introduced by discrete PWM model, the digital control loop has another independent source of delay represented as the control algorithm computation delay [1], [15]. Since digital controller cannot compute the input to the modulator in the same sampling period when it has to be applied, control algorithm computational delay represents time required by the processor to compute new output signal values based on the input variable samples. It basically means that the modulator input within a given sampling period had to be computed during the previous control algorithm period. This leads to an additional one modulation period delay introduced by the control algorithm.

In order to simplify the controller design equations, both delays due to discrete PWM and control algorithm can be grouped together [8], [16], and approximated as a first order transfer functions by implementing Pade approximation:

$$e^{-sT_d} \cong \frac{1 - s\frac{T_d}{2}}{1 + s\frac{T_d}{2}} \quad (4.11.)$$

With these two delays taken into account, the purely continuous model of the sampled data closed loop system of the microgrid tie inverter is completed and represented in Figure 4.10.

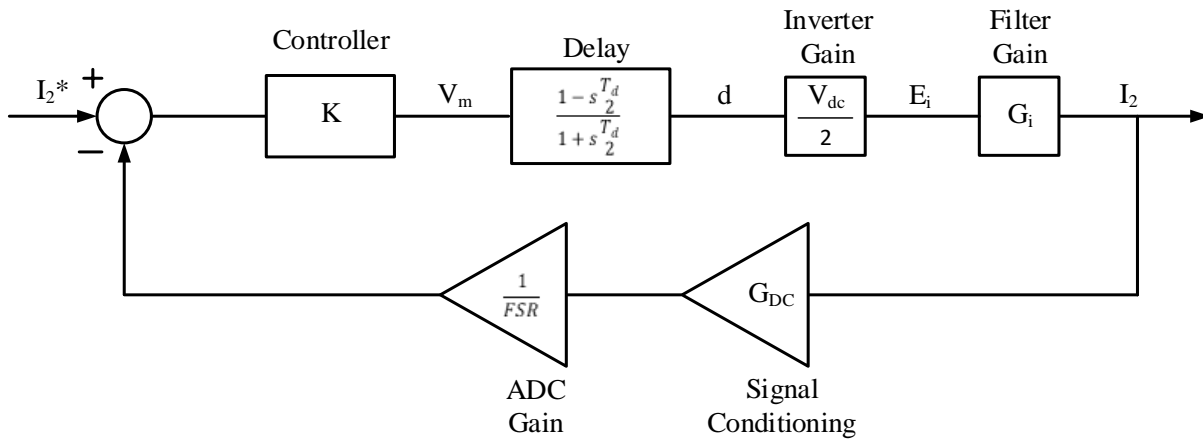


Figure 4. 10. Continuous model of the microgrid tie inverter closed loop system

With the continuous model of the closed loop system being established, the design of the continuous time controller for the current control loop can be initiated.

4.3. Control in DQ0 rotational reference frame

As discussed previously in Chapter 3.3.3, synchronous reference frame transformation achieves current control to be realized in a system that involves DC signals that rotate with the grid voltage frequency, rather than using AC signals instead. Every time there is a demand for the power delivery to the microgrid, current control loop exhibits a step change in the reference current signal, which introduces a transient response of the whole MTI system. Transient response of a grid tie inverter system is very restrictive [17], [18], [19], [20] and requires various system characteristic values such as rise time, overshoot and oscillation damping to be satisfied [21], [22], [23]. In order to achieve satisfactory dynamic performance of the system, proportional-integral (PI) controllers have been dominantly used in grid tie inverter applications in the past [22], [19]. Since usage of PI based current controllers does not always allow for all the dynamic performance requirements to be met [24], multiple other control techniques have been proposed as an improvement [18], [25-32]. These different linear and nonlinear control techniques are more complicated in implementation and tuning than conventional PI controllers, and may only provide a comparative benefit in limited number of specific applications, which MTI is not considered as.

A single-loop digitally controlled MTI system with d and/or q axis representation as shown in Figure 4.11. will be considered for controller design and analysis.

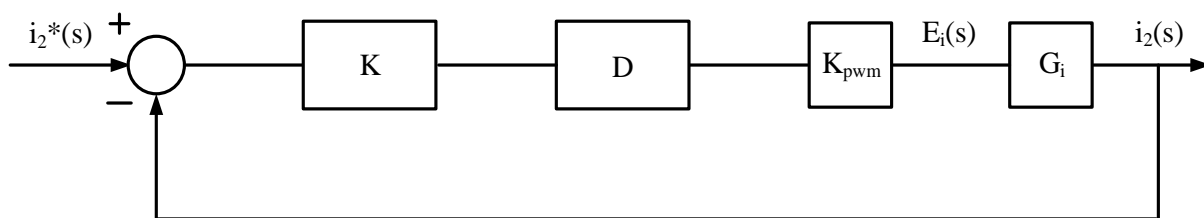


Figure 4. 11. Single loop controlled MTI system

As shown in (4.11), the total processing delay time for sampling, analog to digital conversion, computation, and duty cycle update is summarized and represented as single transfer function D_d :

$$D_d(s) = e^{-sT_d} \cong \frac{1 - s\frac{T_d}{2}}{1 + s\frac{T_d}{2}} \quad (4.12.)$$

Also, k_{pwm} represents a total loop gain, consisting of a product of inverter, ADC and current sensing circuit gains. i_2^* is a current reference setpoint adjusted to output current levels in circuit. K is the classical PI controller represented as $K = K_p + \frac{K_i}{s}$, and G_i represents a LCL filter transfer function from input filter voltage to output filter current. Therefore, the loop gain of the system is:

$$\begin{aligned} G_{lg}(s) &= K(s)D_d(s)G_i(s)k_{pwm} \\ &= \frac{(k_{pwm}(Fs^3 + Gs^2 + Hs + K_I))}{\frac{T_d}{2}As^5 + \left(\frac{T_d}{2}B + A\right)s^4 + \left(\frac{T_d}{2}C + B\right)s^3 + \left(\frac{T_d}{2}D + C\right)s^2 + Ds} \quad (4.13) \end{aligned}$$

And the closed-loop transfer function of the system from current reference to output current is yielded as:

$$\begin{aligned} G_{cl}(s) &= \frac{i_2(s)}{i_2^*(s)} = \frac{K(s)D_d(s)G_i(s)k_{pwm}}{1 + K(s)D_d(s)G_i(s)k_{pwm}} \\ &= \frac{(k_{pwm}(Fs^3 + Gs^2 + Hs + K_I))}{\frac{T_d}{2}As^5 + \left(\frac{T_d}{2}B + A\right)s^4 + \left(\frac{T_d}{2}C + B + F\right)s^3 + \left(\frac{T_d}{2}D + C + G\right)s^2 + (D + H)s + K_I k_{pwm}} \quad (4.14.) \end{aligned}$$

Where:

$$A = C_f L_1 (L_2 + L_g)$$

$$B = C_f [L_1 (R_2 + R_g + R_c) + (L_2 + L_g)(R_1 + R_c)]$$

$$C = [C_f (R_1 R_c + (R_2 + R_g)(R_1 + R_c)) + L_1 + L_2 + L_g]$$

$$D = R_1 + R_2 + R_g$$

$$E = C_f R_c$$

$$F = -K_p \frac{T_d}{2} E k_{pwm}$$

$$G = (E(K_p - \frac{T_d}{2} K_I) - \frac{K_p T_d}{2}) k_{pwm}$$

$$H = (K_p - \frac{T_d}{2} K_I + E K_I) k_{pwm}$$

For the controller design based on the open-loop Bode plot, frequency ranges in which the magnitudes are above 0 dB are the only ones that will be considered. Integral portion K_i of PI controller has been shown to have negligible influence on system stability if it's value is selected such that it has negligible effect on the phase margin of the loop gain of system [1][33][34]. Therefore, for the purpose of PI controller design, controller can be treated as a proportional controller [24]. In that case the magnitude and phase of the loop gain of the system is given as:

$$20 \log |G_{lg}(j\omega)| = \{20 \log(K_p k_{pwm} |G_i|) \quad (4.15)$$

$$\angle(G_{lg}(j\omega)) = \begin{cases} -\frac{\pi}{2} - \omega T_d, (\omega < \omega_{res}) \\ -\frac{3\pi}{2} - \omega T_d, (\omega < \omega_{res}) \end{cases} \quad (4.16)$$

The Bodeplot of the exemplary loop gain is shown in Figure 4.12., in which a total of three crossover frequencies can be noticed.

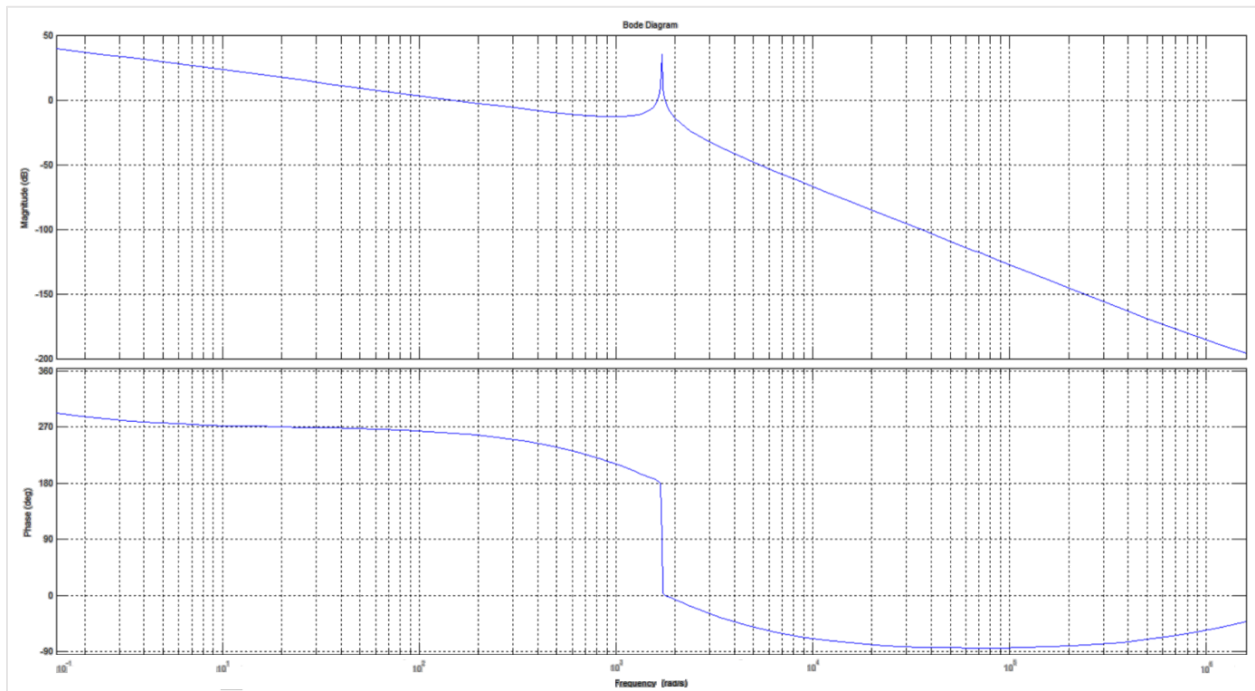


Figure 4. 12. Bode plot of the loop gain of the undamped MTI system

Two crossover frequencies are located on both sides of resonant peak, and are a direct consequence of the undamped nature of the LCL filter. However, as shown previously in Figure 77, MTI cannot meet harmonic standards unless appropriate resonance damping technique is implemented. Therefore, passive resistor damping will be assumed at this point, and resonance damping will be discussed in more details later in the work. As shown with representation of both systems in Figure 4.13., a passively damped system can be approximated as a second order system with almost no error introduced in the low frequency range.

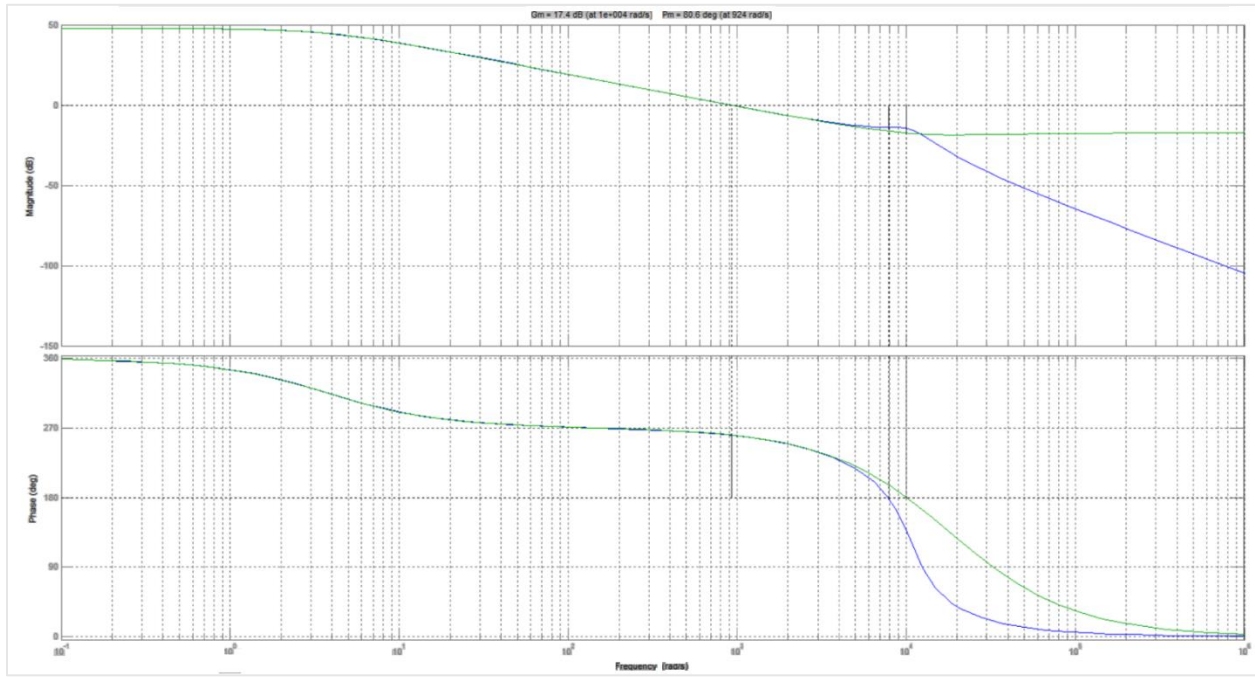


Figure 4. 13. Bode plot of the loop gain of the damped MTI system and second order system approximation

Therefore, by treating damped system as a second order system for controller design purposes, desired dynamic characteristics of the system can be achieved by setting a target value for the system phase margin, and using a well-known relation between those characteristics and phase margin of a second order system [21]. In order to achieve targeted phase margin ρ , the crossover frequency ω_{co} is calculated firstly as:

$$\omega_{co} = \frac{\pi - \rho}{2T_d} \quad (4.17.)$$

which at $0dB$ gain results in proportional gain K_p :

$$K_p = \frac{1}{k_{pwm} |G|(at \omega_{co})} \quad (4.18.)$$

It is important to point out that in order to maintain a target phase margin of a system, a product of the proportional gain and total time delay in the loop needs to be kept constant $K_p T_d =$

const. For cases where T_d is very small, the increase in k_p value is limited until the point where crossover frequency becomes close to resonance frequency. On the other hand, for a given delay in the loop, increase in proportional gain K_p leads to reduction in phase margin. Figure 4.14. shows a relation between phase margin ρ and proportional gain K_p as a function of k_{pwm} , $K_p = X_p * k_{pwm}$.

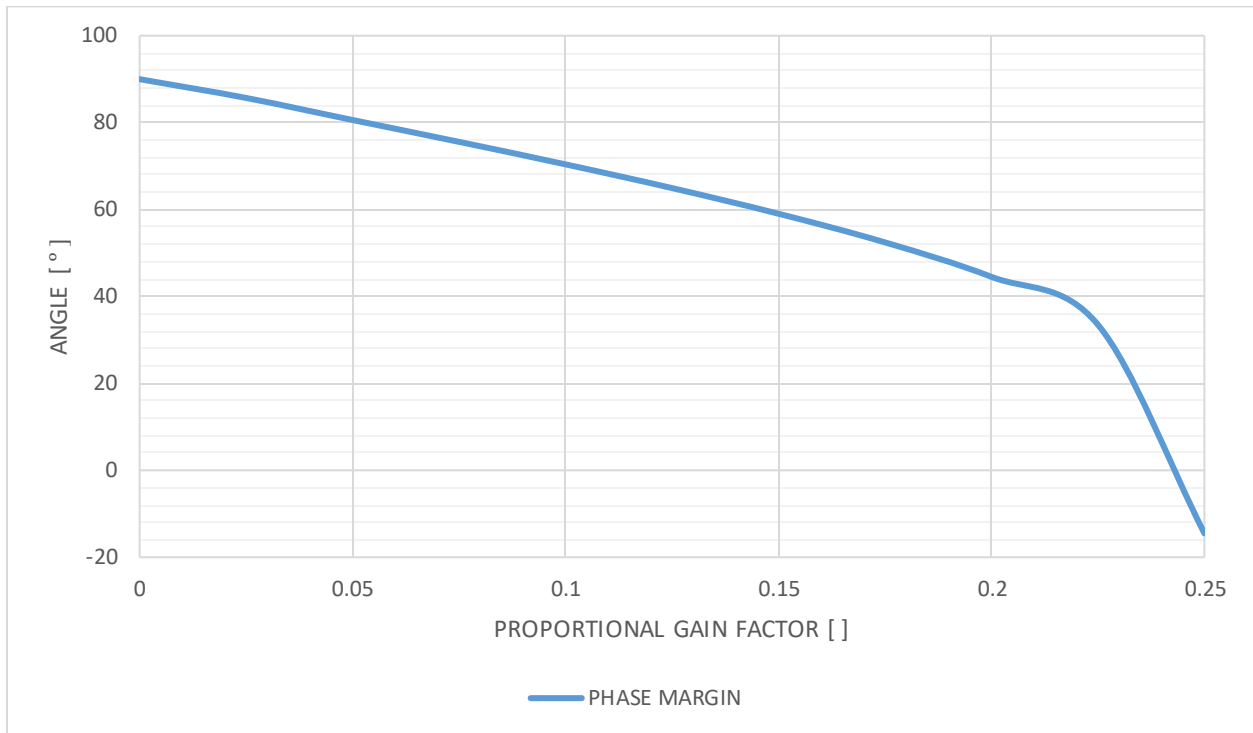


Figure 4. 14. Phase margin dependency on proportional gain factor X_p

Finally, after the proportional gain of the controller is determined, integral gain K_i is designed such that it has minor contribution on the phase margin value, therefore

$$K_i = \frac{\omega_{co}}{20} = \frac{\frac{\pi}{2} - \rho}{20T_d} \quad (4.19.)$$

4.4. Grid Synchronization

In order to consistently deliver power to the microgrid, currents have to be synchronized with grid voltages [35]. On top of that, phase angle of the grid voltage needs to be a clean signal in order to be used as part of the inverter current reference generation. Therefore, grid voltage synchronization techniques have an essential role in detection of the phase angle of the grid voltage [36]. Comparative analysis of all the major grid synchronization algorithms under various grid conditions is presented in [37]. The algorithm that has become most popular, due to simple implementation and good performance under balanced voltage condition, is the phase locked loop [38] implemented in rotating reference frame and shown in Figure 4.15.

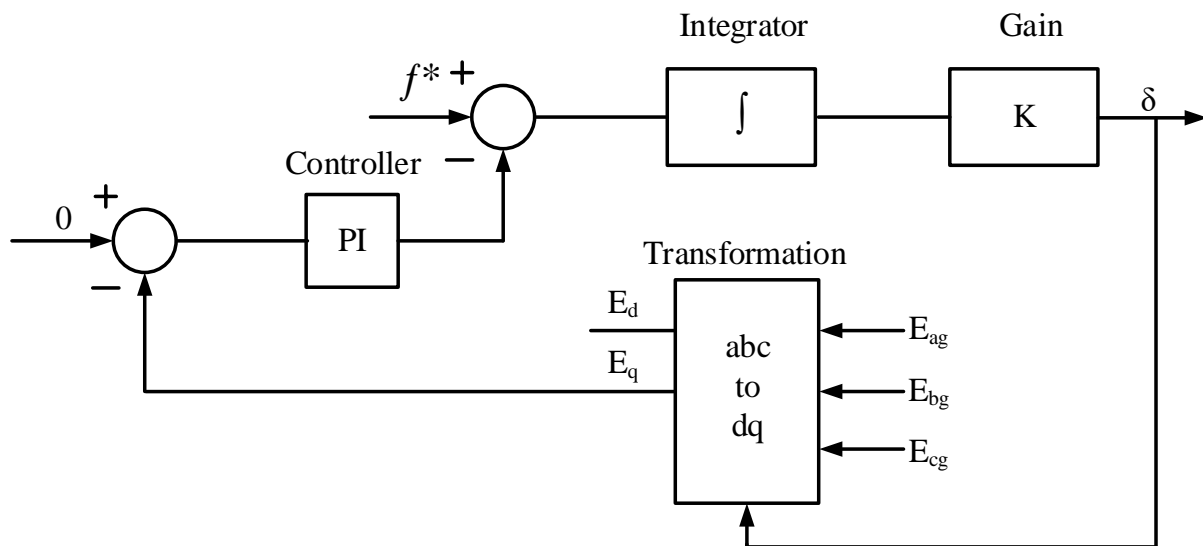


Figure 4. 15. Phase Locked Loop Structure

For a balanced three-phase grid voltage represented as (4.20.), with amplitude E_m and $\theta_g = \omega_g t$, where ω_g is the fundamental grid frequency.

$$\begin{bmatrix} E_{gA} \\ E_{gB} \\ E_{gC} \end{bmatrix} = E_m \begin{bmatrix} \cos \theta_g \\ \cos \left(\theta_g - \frac{2}{3}\pi \right) \\ \cos \left(\theta_g + \frac{2}{3}\pi \right) \end{bmatrix} \quad (4.20.)$$

The dq signals become (4.21.) and turn into dc values with $E_q = 0$ when detected phase $\angle \delta$ becomes same as θ_g [39].

$$\begin{bmatrix} E_{gd} \\ E_{gq} \\ E_{go} \end{bmatrix} = T_{dq} \begin{bmatrix} E_{gA} \\ E_{gB} \\ E_{gC} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\delta) & \cos\left(\delta - \frac{2\pi}{3}\right) & \cos\left(\delta - \frac{4\pi}{3}\right) \\ \sin(\delta) & \sin\left(\delta - \frac{2\pi}{3}\right) & \sin\left(\delta - \frac{4\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} E_{gA} \\ E_{gB} \\ E_{gC} \end{bmatrix} = E_m \begin{bmatrix} \cos(\theta_g - \delta) \\ \sin(\theta_g - \delta) \\ 0 \end{bmatrix} \quad (4.21.)$$

[38] and [40] provide linearized models of phase locked loop showing that it is a type 2 system which is able to track the ramp phase angle signal with zero steady-state error, therefore leading to δ equaling θ_g and full grid synchronization.

In cases where grid voltage has unbalanced conditions, or is polluted by harmonics, the phase angle signal detected by the phase locked loop becomes distorted. Therefore, some improvements of the phase locked loop algorithm have been proposed to address performance under distorted grid conditions [40-42]. Also, [43] and [44] point out that the proper design of the phased locked loop is essential since it may have impact on inverters output impedance and closed loop stability.

Considering that when detected phase angle δ becomes same as θ_g , E_q becomes 0, the instantaneous active (P) and reactive (Q) power injected into the grid calculated in dqo reference frame become [45], [46]:

$$P = \frac{3}{2}(E_{gd}i_{gd} + E_{gq}i_{gq}) = \frac{3}{2}E_{gd}i_{gd} \quad (4.22.)$$

$$Q = \frac{3}{2}(E_{gq}i_{gd} - E_{gd}i_{gq}) = -\frac{3}{2}E_{gd}i_{gq} \quad (4.23.)$$

Basically, active and reactive power injected into the grid are controlled by controlling the d and q component of the current injected into the grid respectively.

4.5. System Stability

Stability is considered one of the most important properties of a control system, and adequate stability margin requirement needs to be satisfied firstly. For linear, time invariant, continuous systems, stability requirement is reflected thru the placement of poles of a closed loop transfer function of a system, which have to be placed in the left half plane in order for the system to be stable [21]. One of the classical methods for stability analysis is the root locus analysis [21], which will be used as a main approach for stability analysis in this work. The major constraint in digital control based grid tie inverter system is the introduced time delay which significantly affects stability [1]. There had been numerous studies related to the stability analysis of the grid tie inverter system based on the single loop control without any damping measures applied [1], [15], [22], [24], [33], [47-54]. However, results are quite conflicting, and no conclusion can be derived, especially when control loop delays are considered.

In order to illustrate the relation between the loop delay T_d and proportional gain of the controller K_p for an undamped system using a single loop control, root locus of the closed loop function G_{cl} as a function of K_p is presented in Figure 4.16., considering asynchronous regular sampling $T_s = \frac{1}{2f_{sw}}$, which is typical for most standard inverter applications. K_p varies in a range

$$\frac{1e^{-5}}{k_{pwm}} < K_p < \frac{1}{k_{pwm}}.$$

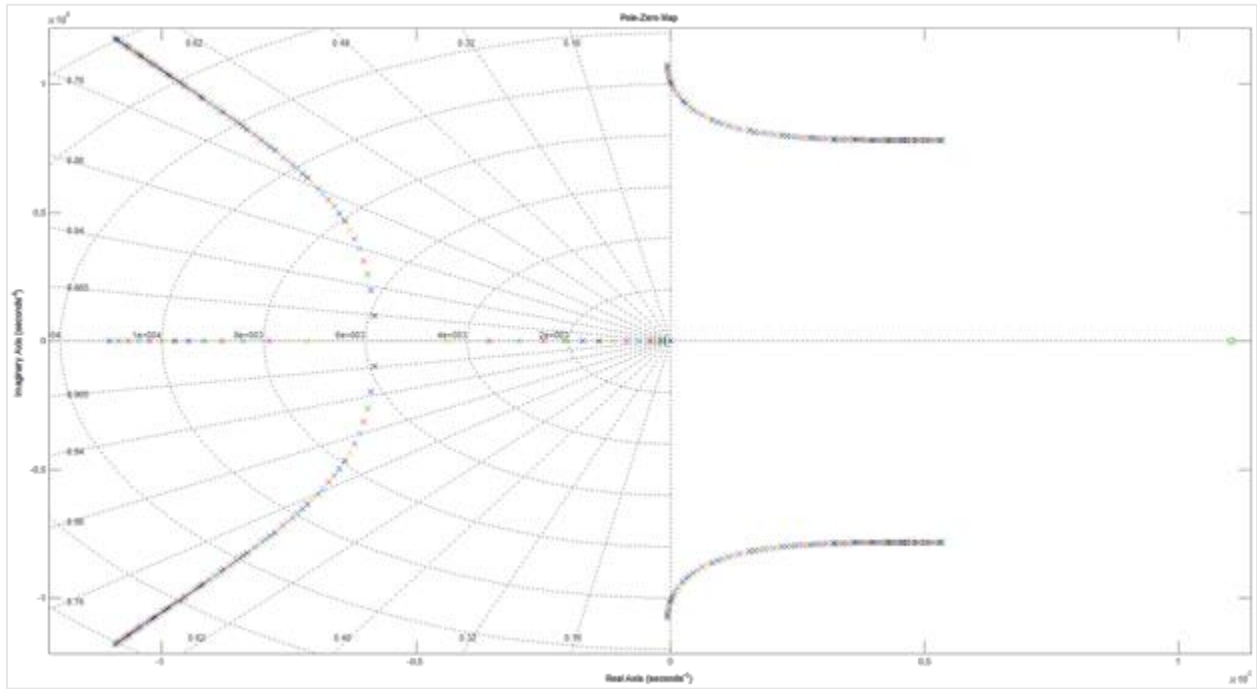


Figure 4. 16. Root Locus of G_{cl} as a function of K_p

With the exception of very low values of K_p , resonant poles are located in right half plane, thus making a closed loop system unstable. Also, it is important to note that in case of low K_p , where system is obviously stable, damping factor is really low, thus making a system unacceptable from harmonics standpoint. Another opportunity to analyze stability of a single loop controlled undamped system is by analyzing a root locus of G_{cl} as a function of loop delay T_d under constant $K_p = 0.05/k_{pwm}$, as shown in Figure 4.17. T_d varies in range $0.1 \left(\frac{1.5}{4140} \right) < T_d < 5 \left(\frac{1.5}{4140} \right)$

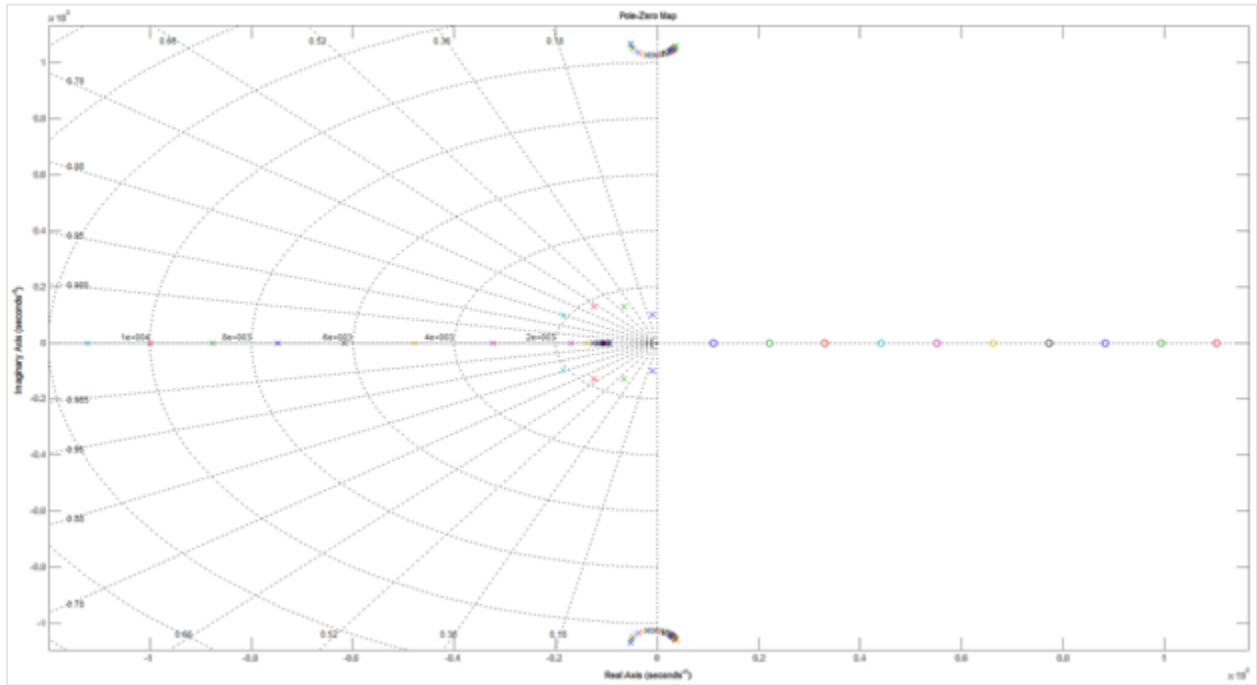


Figure 4. 17. Root Locus of G_{cl} as a function of T_d

In cases of no delay or small loop delay high frequency resonant poles are located in the right half plane, causing system to be unstable. As loop delay increases, resonant poles start moving towards left half plane, thus making system stable. After further increase in the delay, low frequency poles start becoming imaginary and moving towards right half plane, therefore making system unstable again. Therefore, it important to notice that a range of loop delay values exist, under which undamped single loop controlled system is stable. Out of all the previous studies mentioned, this result is closest to the conclusions derived in [15][51], where the grid current controlled, undamped system is stable only if the sampling frequency falls within the stable range defined based on the resonance frequency of the LCL. However, results obtained in these two studies do not match results obtained in this work, most probably due to exclusion of parasitic resistances in the circuit, which are crucial for stability analysis of undamped systems. Despite the fact that undamped single loop controlled systems can be designed to maintain stable over the wide range of parameter variation, these undamped poles in the system will constantly get excited by

the switching action of the inverter, thus creating oscillations that would deteriorate the harmonic performance of the system.

4.6. Resonance Damping

4.6.1. Passive Damping

A simplest way to provide desired resonance damping for a single loop controlled MTI system is by including a damping resistor into the LCL filter design [55][56]. There are multiple different locations where resistor can be placed in a filter circuit, and this whole set of damping solutions is called passive damping. As already demonstrated in chapter 3.1.4., addition of resistor in series with either of the filter inductors has minor effect on resonance damping, but it introduces large power losses and voltage drop across filter. Therefore, additional damping resistors in series with filter inductors are considered an impractical solution for filter damping and will not be further investigated in this work. Another set of solutions is related to the resistors added to the capacitor branch, which can all be simplified by an equivalent series or parallel resistor with the filter capacitor, as shown in Figure 4.18.

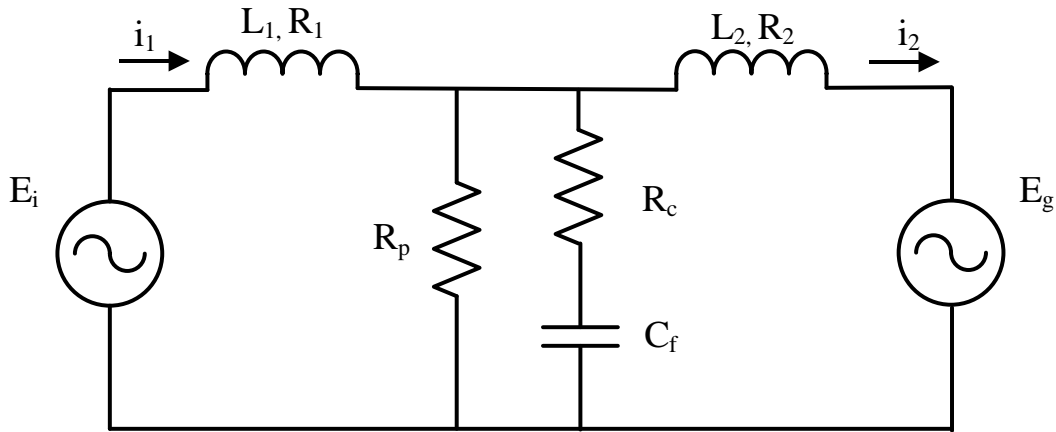


Figure 4. 18. Filter equivalent circuit with series or parallel damping resistor

Frequency characteristic of a series resistor solution is shown in Figure 4.19., where damping resistor R_s varies between $1\% < R_s < 20\%$.

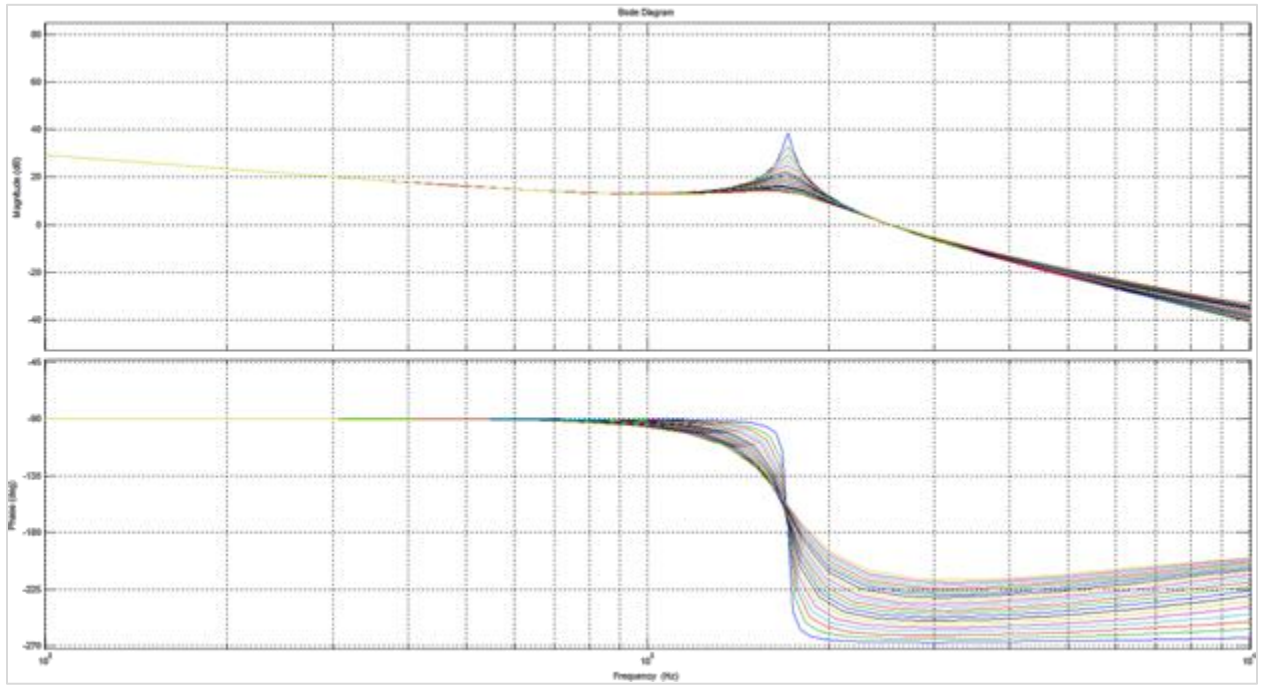


Figure 4. 19. Bode plot of transfer function $G_i(s)$ for filter series damping resistor R_s variation

Series damping resistor is quite effective in damping of the resonance, but there is also a drawback related to the decreased filtering performance in a high frequency range, where the switching ripple is present. This is an expected behavior since at high frequencies resistor starts becoming a dominant impedance in capacitor branch, therefore increasing its impedance. Also, series resistor introduces additional power losses that are a large concern in terms of heat dissipation and efficiency of the overall system. With some minor approximation, power loss per resistor can be calculated as:

$$P_{loss} = R_s \left[(I_{ripple}^2) + \frac{U_{ln}^2 (1 + \frac{Q}{S} L_2 [\%])^2}{X_c^2} \right] \quad (4.24.)$$

Where I_{ripple} is ripple current of inductor L_1 , U_{ln} is line to neutral voltage at PCC, Q is the reactive power injected into the grid, S is the rated apparent power of the MTI, L_2 is the inductance in per unit percentile, and X_c is the capacitor reactance at line frequency.

Losses in the resistor have two components, one related to the fundamental line frequency, and second one related to the ripple current produced by switching. As demonstrated previously in chapter 2.5.4, DDPWM methods produce high ripple rms current at low modulation index values, while the fundamental frequency losses in resistor are peaking at high modulation index values in cases where reactive power support is needed. Therefore, these two loss components are individually reaching maximum values at different conditions, so this needs to be carefully considered when designed.

Another available damping technique is a damping resistor connected in parallel with filter capacitor. The LCL filter state-space model is derived from the single phase model as:

$$\frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \\ V_f \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L_1} & 0 & -\frac{1}{L_1} \\ 0 & -\frac{R_2}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_f} & -\frac{1}{C_f} & -\frac{1}{C_f R_p} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ V_f \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{L_1} \\ -\frac{1}{L_2} & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} E_g \\ E_i \end{bmatrix} \quad (4.25.)$$

Frequency characteristic of a parallel resistor solution is shown in Figure 4.20., where damping resistor R_p varies between $1pu < R_p < 20pu$.

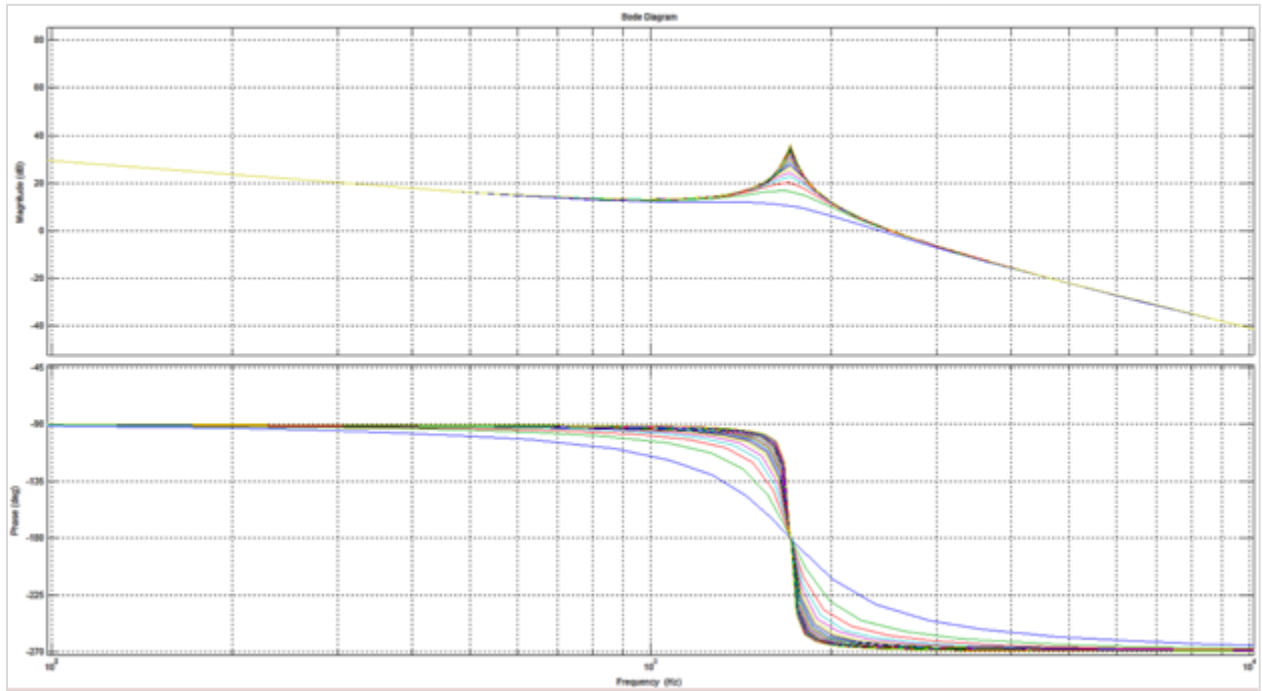


Figure 4. 20. Bode plot of transfer function $G_i(s)$ for filter parallel damping resistor R_p variation

Frequency characteristic of a filter with parallel damping resistor looks even more beneficial than series resistor, simply due to non-affected filtering performance in a high frequency range, where the switching ripple is present. The reason for that is that the parallel resistor is not in the direct flow of the ripple current, which closes thru the filter capacitors undisturbed.

With some minor approximation, power loss per parallel resistor can be calculated as:

$$P_{loss} = \frac{U_{in}^2 (1 + \frac{Q}{S} L_2[\%])^2}{R_p^2} \quad (4.26.)$$

Parallel resistor is not a viable solution for passive resonance damping due to significantly smaller damping to power loss coefficient, which brings higher losses and decreased efficiency of the system with this solution. However, parallel resistor still remains a valuable concept to investigate, since it will be used later on when active damping techniques are introduced.

For damping solution that involves series damping resistor, Figure 4.21. shows how the resistor R_s value affects the closed loop system by showing the root locus of the closed loop function G_{cl} when considering $T_s = \frac{1}{2f_{sw}}$ and $K_p = \frac{0.05}{k_{pwm}}$. R_s varies in a range $1\% < R_s < 100\%$.

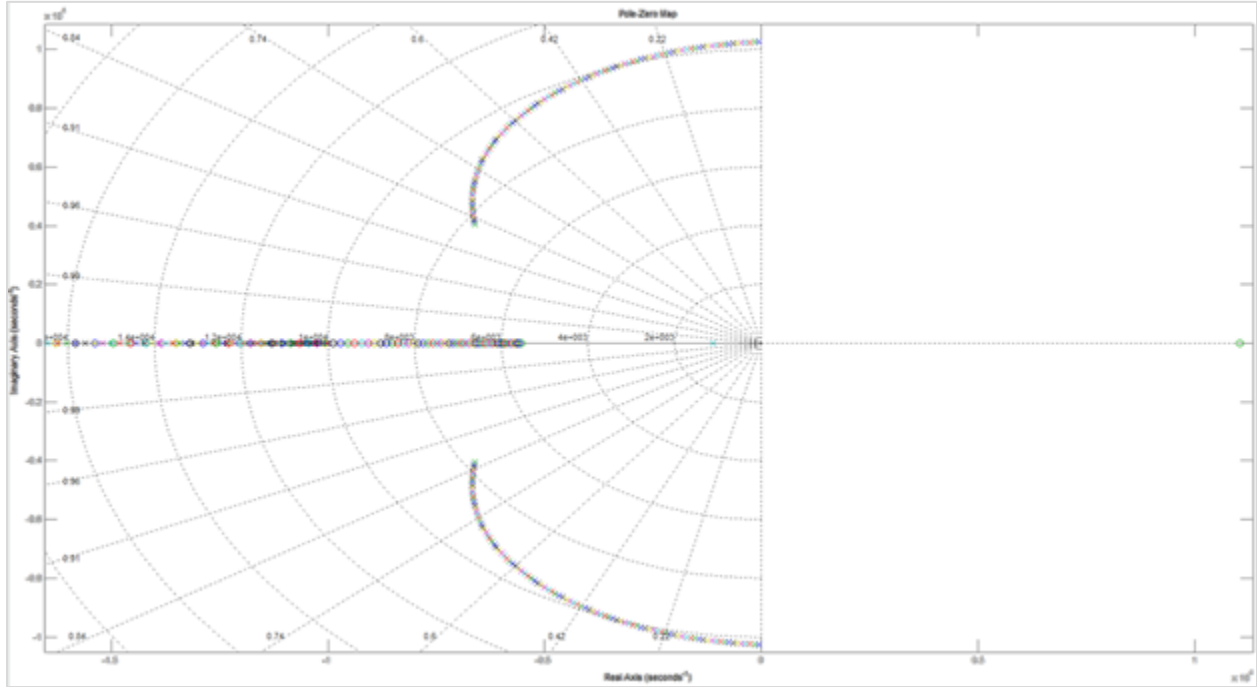


Figure 4. 21. Root Locus of G_{cl} as a function of R_s

As damping resistor value increases, damping factor of resonant poles increases and system gains more stability. Also, another useful figure is root locus of the closed loop function G_{cl} as a function of K_p as presented in Figure 4.22., with $T_s = \frac{1}{2f_{sw}}$. K_p varies in a range $\frac{1e^{-5}}{k_{pwm}} < K_p <$

$$\frac{1}{k_{pwm}}$$

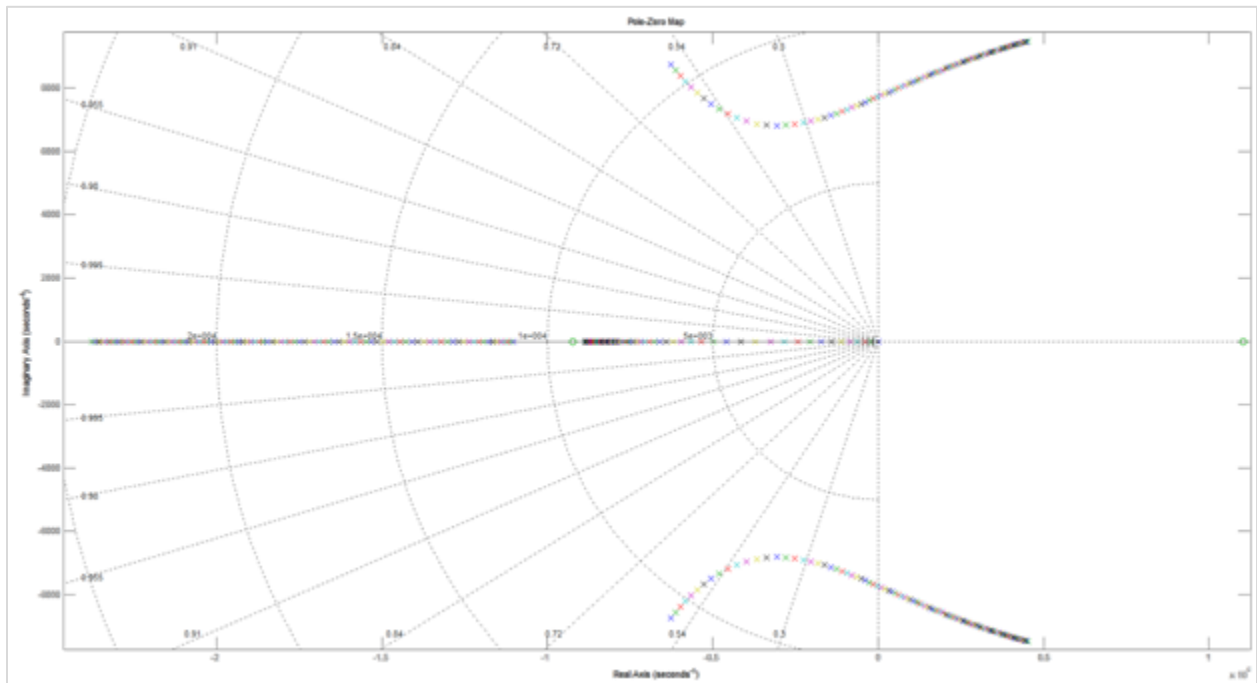


Figure 4. 22. Root Locus of G_{cl} as a function of K_p

As opposed to the same analysis performed for undamped single loop controlled system, where only low values of K_p provided stability, damped system shows a wider range of values under which system remains stable. Also, trend of damping factor drop with increase in proportional gain K_p is present, meaning that K_p affects system damping.

Finally, the stability of a single loop controlled passively damped system is by analyzing a root locus of G_{cl} as a function of loop delay T_d under constant K_p , as shown in Figure 4.23. T_d

$$\text{varies in range } 0.1 \frac{1.5}{4140} < T_d < 5 \frac{1.5}{4140}$$

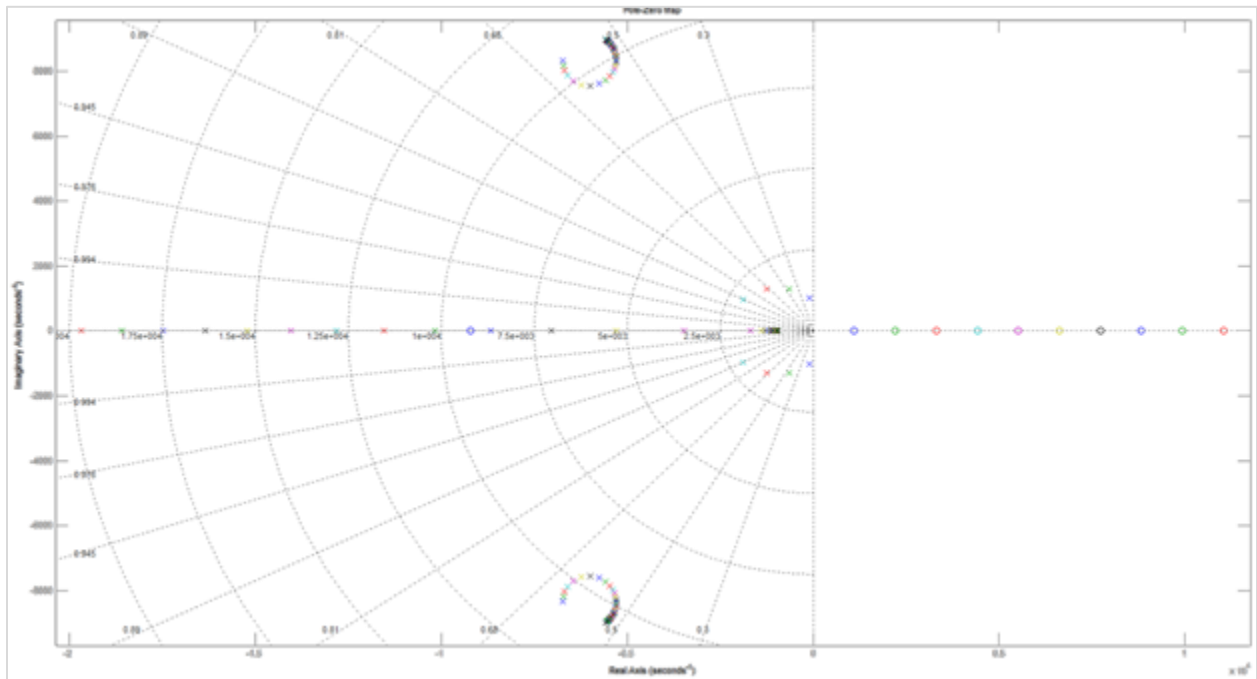


Figure 4. 23. Root Locus of G_{cl} as a function of T_d

Contrary to the undamped system, where a system was stable only for a certain range of loop delay values, damped system is stable until the delay values become high enough that low frequency poles start becoming affected by becoming imaginary first, and moving towards the right half plane. Also, throughout this wide range of loop delay values, high frequency resonant poles barely get affected in terms of damping. Therefore, it is conclusive that loop delay has almost no impact on damping performance of the passive damping solution.

On top of stability issue, which is obviously addressed thru passive damping technique, it is also important to characterize the harmonic performance of the single loop controlled system., The major two sources of harmonics present in the grid side current are sourced from the inverter input voltage and grid voltage. Harmonics caused by the grid voltage will be discussed in chapter 4.7 and will not be further investigated here. Nevertheless, as already explained in chapter 2.5, grid current harmonics generated by inverter input voltage are caused by switching of the inverter, and are mostly influenced based on the selection of the modulation technique, dead time value, pulse width limitations and semiconductor switch parameters. Based on the single loop controlled

diagram shown in Figure 4.24., all the harmonics generated by switching can be modeled as an input disturbance acting on a filter (plant) after the controller.

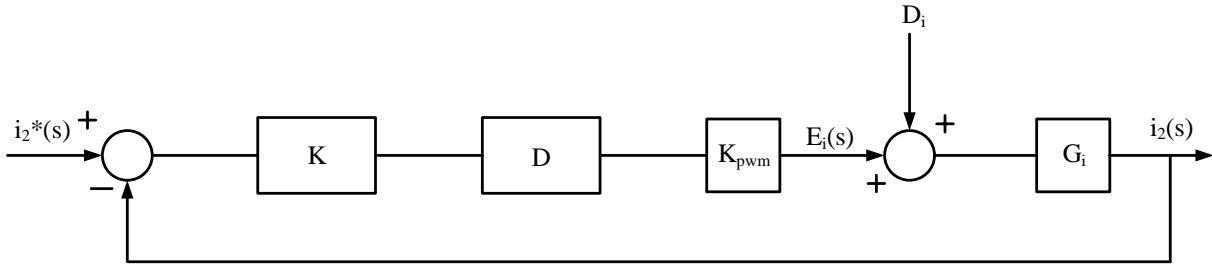


Figure 4. 24. Single loop controlled MTI system with input disturbance D_i representation

Since disturbance rejection is the most important performance measure of MTI system, it is important to define the influence that input voltage harmonics, represented as disturbance, have on the output grid current. Therefore, disturbance transfer function needs be defined as:

$$G_d = \frac{I_2}{D_i} = \frac{G_i(s)}{1 + K(s)D_d(s)k_{pwm}G_i(s)}$$

$$= \frac{s^3 E \frac{T_d}{2} + s^2 \left(E + \frac{T_d}{2} \right) + s}{\frac{T_d}{2} A s^5 + \left(\frac{T_d}{2} B + A \right) s^4 + \left(\frac{T_d}{2} C + B + F \right) s^3 + \left(\frac{T_d}{2} D + C + G \right) s^2 + (D + H)s + K_I k_{pwm}} \quad (4.27.)$$

Figure 4.25. shows a frequency characteristic of a disturbance transfer function G_d as a function of K_p with $T_s = \frac{1}{2f_{sw}}$ and $R_s=100\text{m}\Omega$, which represents 60% of base impedance. K_p varies in a range $0 < K_p < \frac{0.2}{k_{pwm}}$, and system is stable in a full range of K_p values.

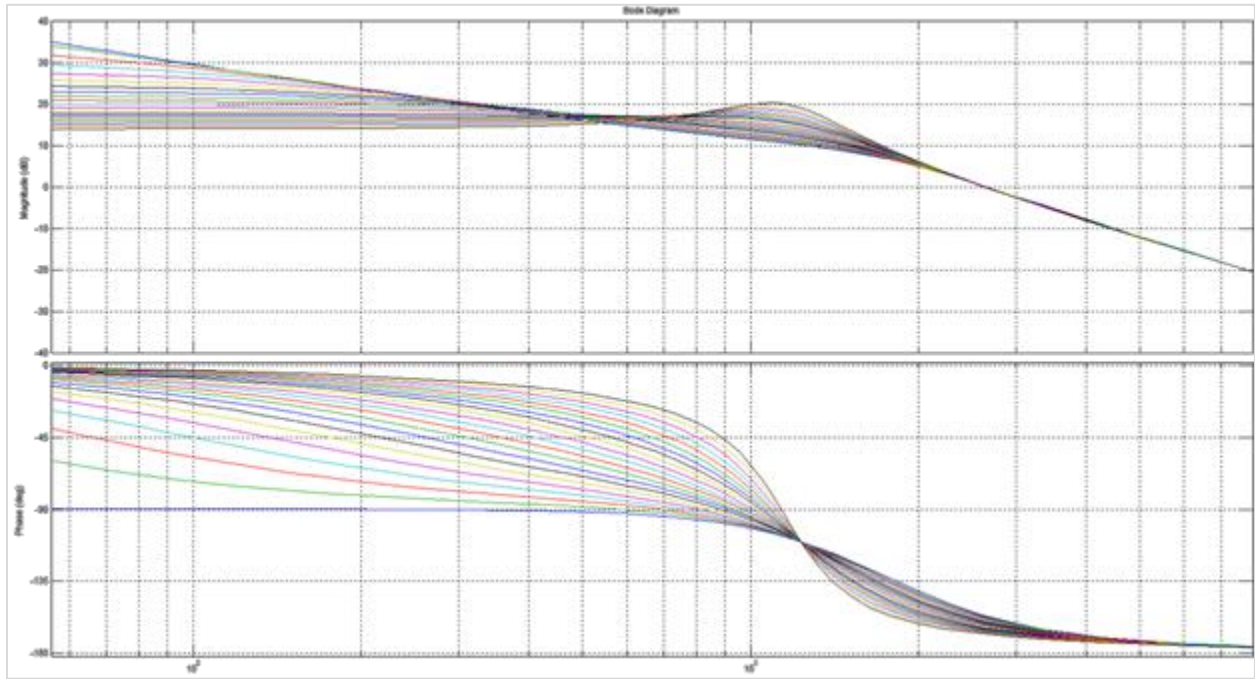


Figure 4. 25. Frequency characteristic of G_d as a function of K_p

Per Figure 4.25., for the purpose of analysis, Bode plot of disturbance transfer function can be divided into three sections, which are in low frequency, medium frequency and high frequency ranges. In low frequency range, where 5th and 7th harmonics as the most dominant low order harmonics are, disturbance rejection increases with rise of K_p . In medium frequency range, where rest of the low order frequency harmonics are, including resonant frequency, increase in K_p value decreases disturbance rejection, therefore reducing harmonic performance of a system. High frequency range, where switching frequency is, is not affected by the changes in K_p . Since low order voltage harmonics created by DDPWM are increasing in value with the rise in harmonic order, from overall harmonic performance of MTI it is desirable to keep K_p value low.

It is of interest to also look into the affect that loop delay T_d has on the disturbance transfer function G_d , which is shown in Figure 4.26. for constant K_p , where T_d varies in range $\frac{1.5}{(2*4140)} <$

$$T_d < \frac{1}{20} \frac{1.5}{(2*4140)}.$$

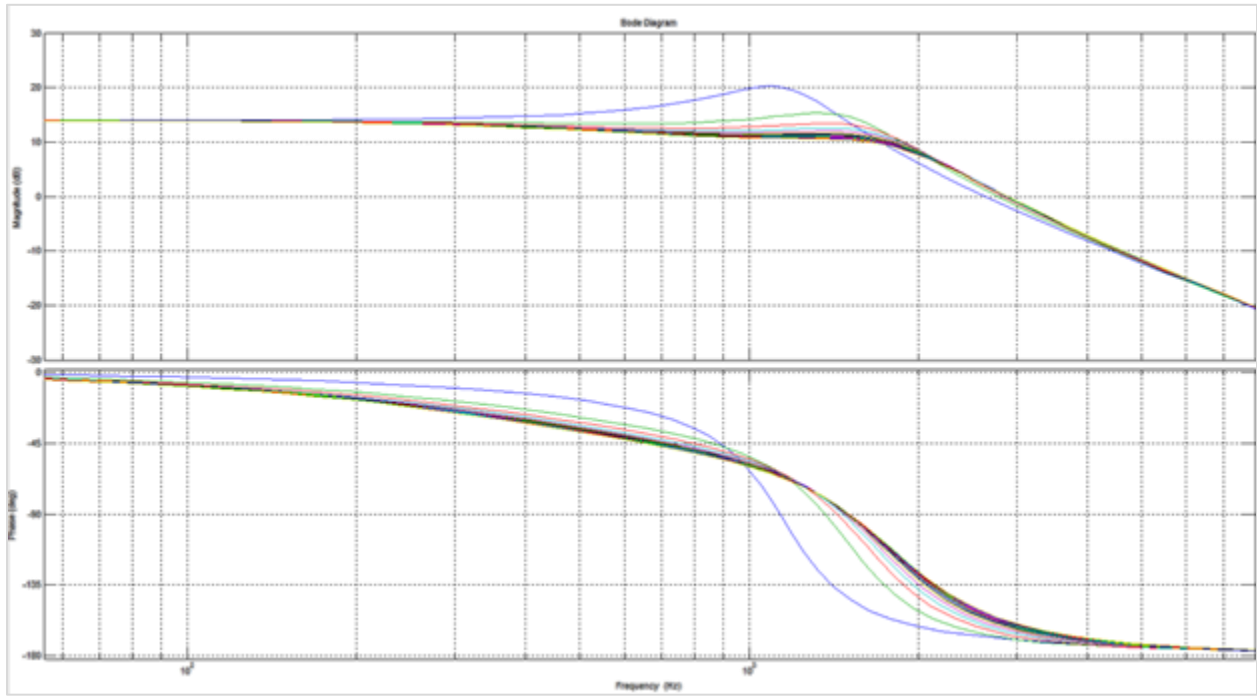


Figure 4. 26. Frequency characteristic of G_d as a function of T_d

In the medium frequency range, where disturbance rejection was the lowest for high K_p values, lower loop delay values cause higher disturbance rejection without any impact on low or high frequency values. Therefore, it is worthy of concluding that in order to provide an optimal harmonic performance using a single loop controlled, passively damped MTI system, it is desired to use higher K_p values and lower loop delay T_d values in order to ensure high disturbance rejection in low frequency and medium frequency ranges respectively.

In order to test for harmonic performance of passively damped MTI system, system was tested with DDPWM a $c_f = 69$ and full reactive power support to the grid, which was determined to represent the worst case scenario from harmonic performance perspective. All the design parameters selected previously along with all the nonlinearities have been considered in the simulation model. Figure 4.27. compares $K_p = 0$, $K_p = \frac{0.2}{k_{pwm}}$ with $T_d = \frac{1.5}{(2*4140)}$, and $K_p = \frac{0.2}{k_{pwm}}$

with no time delay, in terms of TRD and STHD for first 10 and ranges of harmonics from 10 – 20, 20 – 30, 30 – 40, and 40 – 50 harmonics.

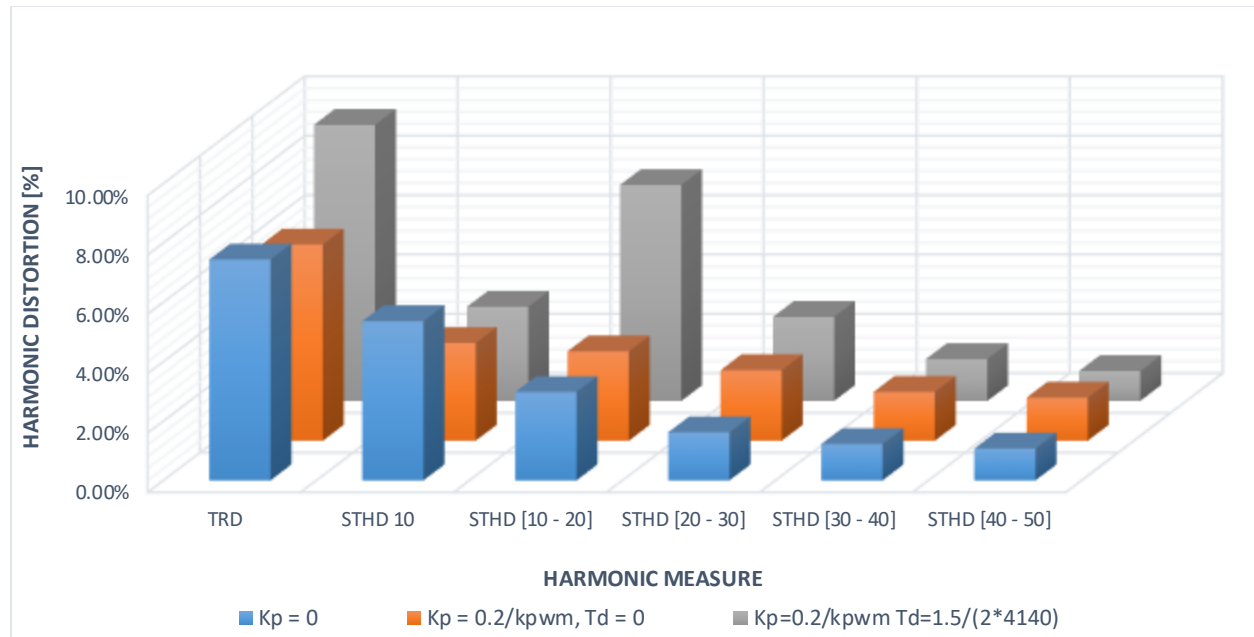


Figure 4. 27. TRD and STHD10/10-20/20-30/30-40/40-50 Comparison between

$$a) K_p = 0; b) K_p = \frac{0.2}{k_{pwm}}, T_d = 0; c) K_p = \frac{0.2}{k_{pwm}}, T_d = \frac{1.5}{(2 \cdot 4140)}$$

The best overall TRD performance is achieved with high K_p gains and no time delay in the loop, as well as for first 10 harmonics. On the other hand, as expected, $K_p=0$ performs worse in low frequency gain, but the best in high frequency range. Time delay introduced into the control loop causes resonant frequency to decrease and resonant harmonics to increase. Therefore, in cases where high proportional gains K_p in the controller are used, resonant frequency is not a function of filter parameters only, but also a function of a loop delay T_d . Also, if high values of K_p are used, despite the usage of a damping resistor, resonance damping decreases with increase in loop delay T_d value. Therefore, we can conclude that highest K_p value possibly achieved for a given system is inversely proportional to the value of the total time delay in the control loop T_d .

So far, the analysis of passive damping solution has assumed no added line impedance on the microgrid side, after the point of common coupling. Criteria necessary for proper resonance damping solution is to retain satisfactory performance under high microgrid impedance values. Effect of high line impedance on the open loop filtering performance has already been covered in chapter 3.3.1.2. However, closed loop stability and high disturbance rejection needs to be maintained. Figure 4.28. shows a root locus of the closed loop function G_{cl} for line impedance variation $0\% < L_g < 20\%$ with $K_p = \frac{0.2}{k_{pwm}}$ and $T_d = 0$. Obviously, line impedance value does not affect stability of the closed loop system.

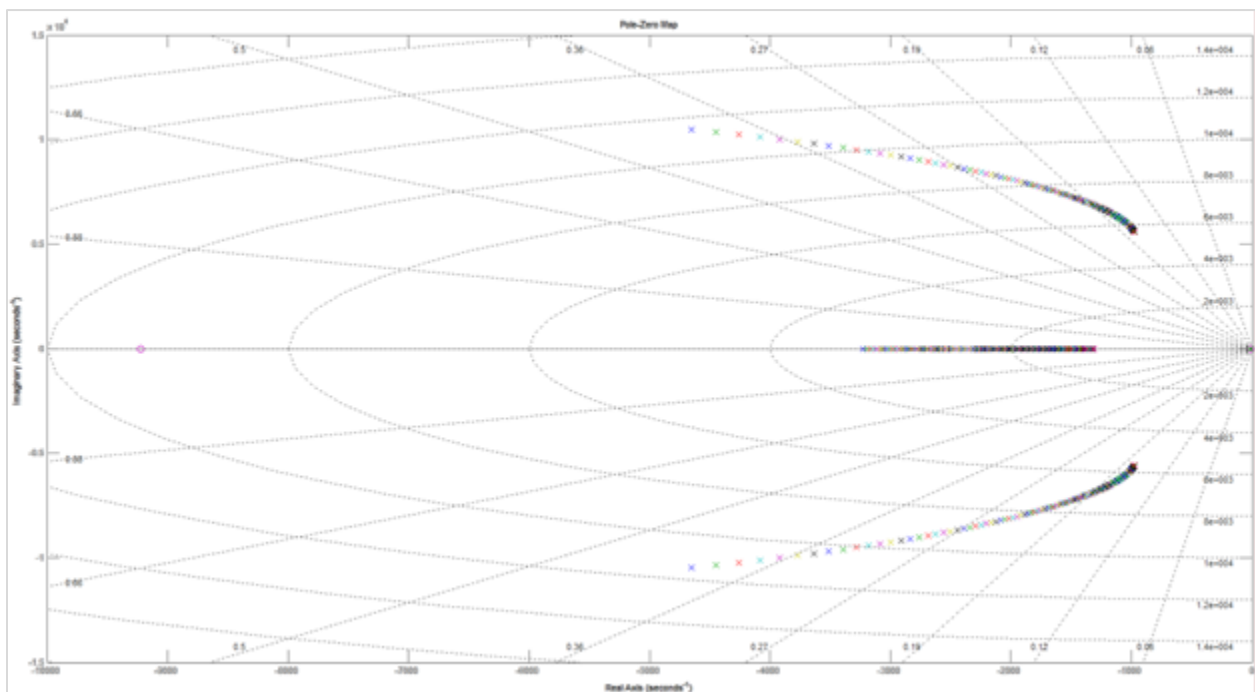


Figure 4. 28. Root Locus of G_{cl} as a function of L_g

Figure 4.29. shows a frequency characteristic of a disturbance transfer function G_d as a function of L_g for the same range and values as in Figure 4.28.

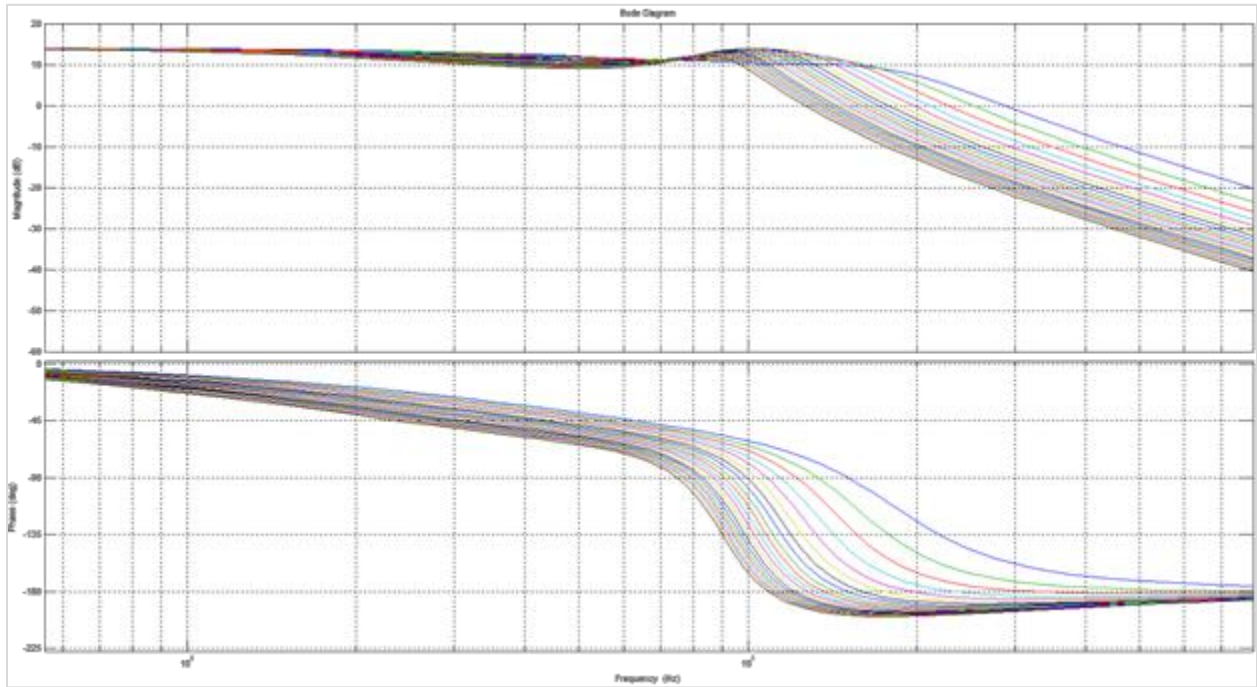


Figure 4. 29. Frequency characteristic of G_d as a function of L_g

Higher line impedance values offer higher disturbance rejection in low and high frequency ranges, thus better harmonic performance. In the medium frequency range around resonant frequency, rise in line impedance values to a certain point decreases and then further increases disturbance rejection back again. This line impedance boundary value is defined by $L_{gb} = L_1 - L_2$. However, DDPWM produces higher voltage sideband harmonics as frequencies get closer to the switching frequency, so decreased disturbance rejection around resonant frequency is expected to be somewhat compensated by lower voltage harmonics. Therefore, it can be stated that line impedance L_g improves overall harmonic performance of a MTI system, and it also impacts resonance by affecting frequency at which resonance occurs, with certain increase in resonant harmonic values for line impedance values $L_g < L_{gb}$.

4.6.2. Active Damping

Inherent resonance of the LCL filter will severely impact stability and performance of the MTI system if no damping techniques are implemented [54, 57, 58]. Therefore resonance damping is crucial part of the MTI system and different passive and active techniques are proposed [55], [58], [59]. As discussed previously, passive damping is the most intuitive way to implement resonance damping, but it also creates undesired and unnecessary power loss. Therefore, active damping methods based on different control algorithms have been proposed [58], [60-62]. Active damping techniques can be divided into two groups, which are either multiloop or filter based. Filter based damping techniques are based on higher order controllers that are basically used to implement a zero pole cancellation technique [24], [63], [64]. However, filter based algorithms have very poor resonance damping performance in cases of variation of system parameters. Specifically, grid side inductance variation is a common issue that moves the resonant frequency, therefore causing filter not to be effective in canceling resonance. Also another drawback of using filter based active damping technique is the complex design algorithm. Therefore, filter based active damping is considered impractical for MTI application, and will not be further investigated in this work. On the other hand, multiloop active damping algorithms are the most popular active damping methods that are based on the inner system state feedback loop, surrounded by the outer current control loop. Inner state feedback loop serves as a damping loop that uses filter capacitor current and/or voltage, and inverter current to stabilize the system and provide damping [1], [61], [65], 66].

Out of all the dual loop control strategies, ones that use inner filter capacitor current with proportional feedback are most commonly applied [58], [60], [65], [67], [68].

A dual-loop digitally controlled MTI system for dq axis representation is shown in Figure

4.30.

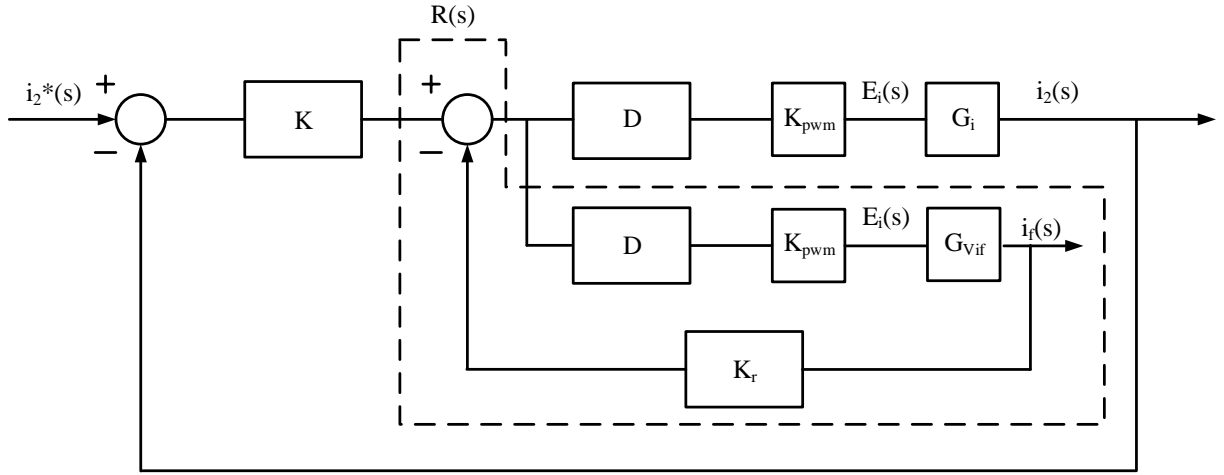


Figure 4. 30. Dual loop controlled MTI system

K_r represents proportional feedback of the filter capacitor current, used as an active resonance damper. The loop gain of the system is obtained as:

$$G_{lg}(s) = K(s)R(s)D_d(s)G_i(s)k_{pwm}$$

$$= \frac{k_{pwm}(Fs^3 + Gs^2 + Hs + K_I)}{\frac{T_d}{2}A_1 s^6 + \left(\frac{T_d}{2}B_1 + A_1\right)s^5 + \left(\frac{T_d}{2}C_1 + B_1\right)s^4 + \left(\frac{T_d}{2}D_1 + C_1\right)s^3 + s^2D_1} \quad (4.28.)$$

Where:

$$R(s) = \frac{1}{(1 + D_d(s)k_{pwm}K_r(s) G_{vif}(s))} \quad (4.29.)$$

And $G_{vif} = \frac{i_f(s)}{E_i(s)}$, as defined in (3.34).

The closed-loop transfer function of the system becomes:

$$\begin{aligned}
G_{cl}(z) &= \frac{i_2(s)}{i_2^*(s)} = \frac{K(s)R(s)D_d(s)G_i(s)k_{pwm}}{1 + K(s)R(s)D_d(s)G_i(s)k_{pwm}} \\
&= \frac{k_{pwm}(Fs^3 + Gs^2 + Hs + K_I)}{\frac{T_d}{2}A_1 s^6 + \left(\frac{T_d}{2}B_1 + A_1\right)s^5 + \left(\frac{T_d}{2}C_1 + B_1\right)s^4 + \left(\frac{T_d}{2}D_1 + C_1 + F\right)s^3 + s^2(D_1 + G)} \quad (4.30.)
\end{aligned}$$

Where:

$$A_1 = A \frac{T_d}{2}$$

$$B_1 = A + B \frac{T_d}{2} - \frac{T_d}{2}C_f L_2 k_{pwm} K_r$$

$$C_1 = B + C \frac{T_d}{2} + C_f L_2 k_{pwm} K_r - \frac{T_d}{2} + C_f R_2 k_{pwm} K_r$$

$$D_1 = C + D \frac{T_d}{2} + C_f R_2 k_{pwm} K_r$$

The effect that proportional feedback gain K_r has on the the closed loop system. Figure 4.31. shows the root locus of the closed loop function G_{cl} when considering $T_s = 0$ and $K_p = \frac{0.05}{k_{pwm}}$.

K_r varies in a range $0 < K_r < \frac{1}{k_{pwm}}$.

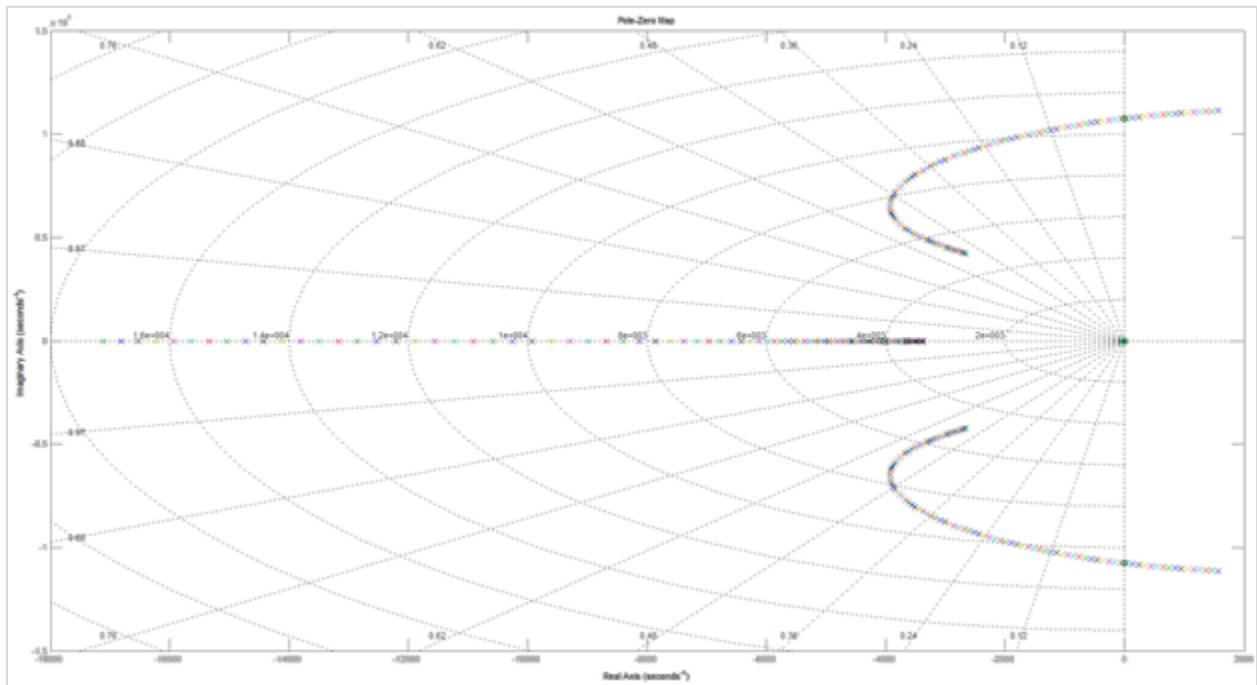


Figure 4. 31. Root Locus of G_{cl} as a function of K_r

With small values of K_r , system is unstable. As gain value increases, system becomes stable, and systems becomes better damped. Next step is to evaluate the effect of the time delay in the control loop. Figure 4.32. represents root locus of the closed loop function G_{cl} as a function of loop delay T_d under constant $K_p = \frac{0.2}{k_{pwm}}$ and $K_r = \frac{0.7}{k_{pwm}}$. T_d varies in range $\frac{1}{10} \frac{1.5}{(2*4140)} < T_d <$

$$\frac{1.5}{(2*4140)}$$

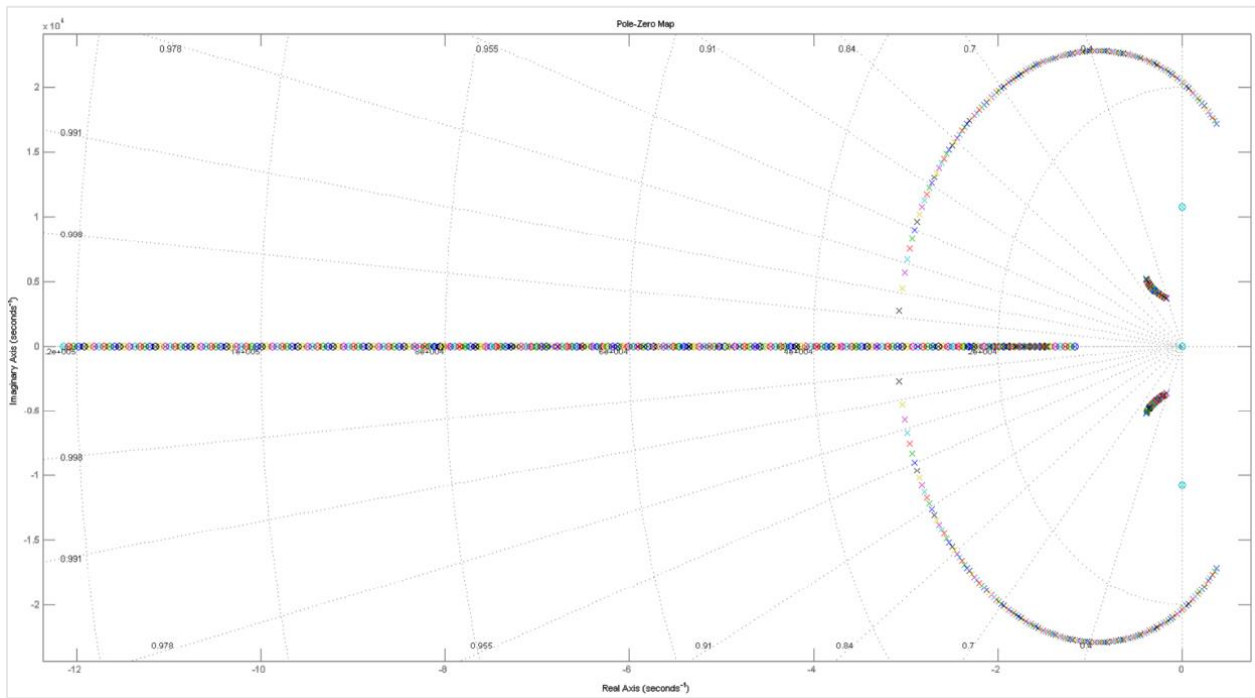


Figure 4. 32. Root Locus of G_{cl} as a function of T_d

Based on the closed loop pole placement, system is unstable for high time delay values. Resonant poles are stable and well damped throughout the whole set of time delay values, but the high frequency poles are unstable first and become stable and better damped with the decrease in loop delay.

Finally, it is useful to investigate whether proportional gain K_p value can improve the stability of the actively damped closed loop system with a loop delay $T_d = \frac{1.5}{(2 \cdot 4140)}$. Figure 4.33.

represents a root locus of the closed loop function G_{cl} as a function of K_p , with $K_r = \frac{0.7}{k_{pwm}}$.

K_p varies in a range $\frac{0.001}{k_{pwm}} < K_p < \frac{0.2}{k_{pwm}}$.

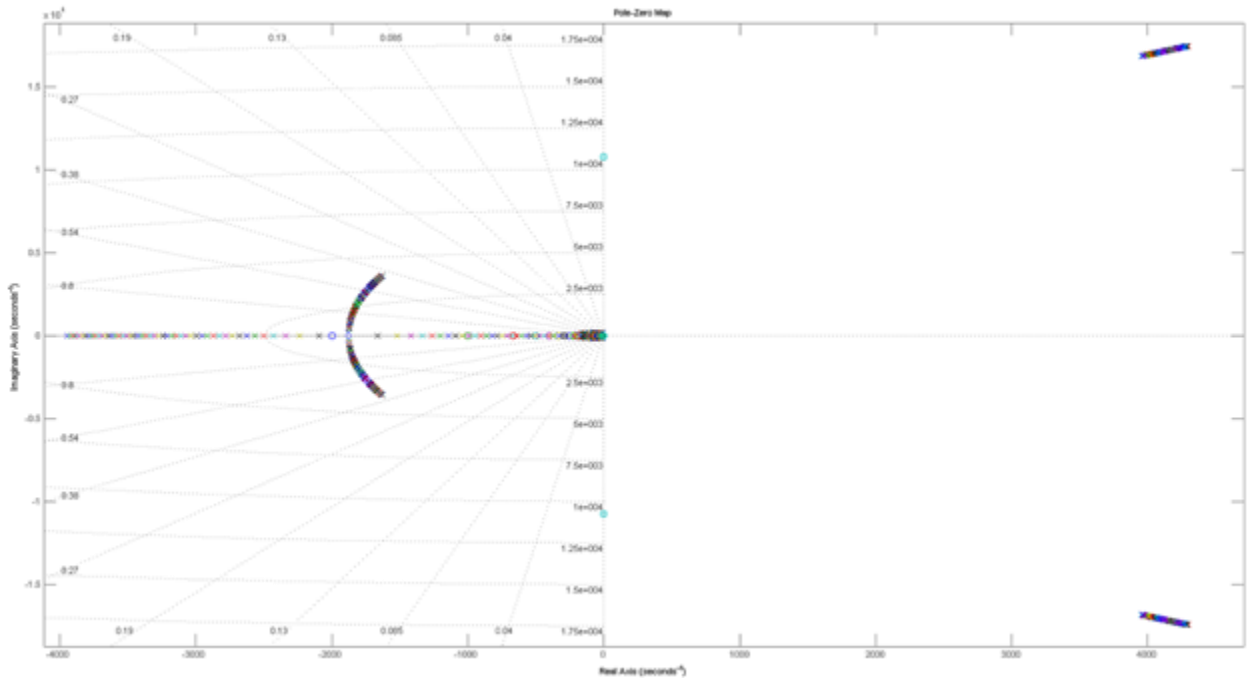


Figure 4. 33. Root Locus of G_{cl} as a function of K_p

K_p has large impact on damping of resonant poles, and lower K_p values provide higher damping. On the other hand, K_p has very little impact on system stability since high frequency poles remain in the right half plane, and hardly get affected.

In addition to evaluation of system stability, which is achieved thru root locus of closed loop system, harmonic performance is another important aspect that needs to be evaluated. Since harmonics generated by switching can be modeled as an input disturbance acting on a plant, disturbance rejection will be the major performance measure of dual loop controlled MTI system. Therefore, disturbance transfer function for dual loop controlled system is defined as:

$$G_d = \frac{I_2}{D_i} = \frac{R(s)G_i(s)}{1 + K(s)D_d(s)k_{pwm}R(s)G_i(s)}$$

$$= \frac{s^3 E \frac{T_d}{2} + s^2 \left(E + \frac{T_d}{2} \right) + s}{\frac{T_d}{2} A_1 s^6 + \left(\frac{T_d}{2} B_1 + A_1 \right) s^5 + \left(\frac{T_d}{2} C_1 + B_1 \right) s^4 + \left(\frac{T_d}{2} D_1 + C_1 + F \right) s^3 + s^2 (D_1 + G) + sH + K_I k_{pwm}}$$

(4.31.)

Frequency characteristic of a disturbance transfer function G_d as a function of K_r with $K_p = \frac{0.2}{k_{pwm}}$ and $T_s = 0$ is shown in Figure 4.36. K_r varies in a range $\frac{0.2}{k_{pwm}} < K_r < \frac{1}{k_{pwm}}$, and system is stable in a full range of K_r values.

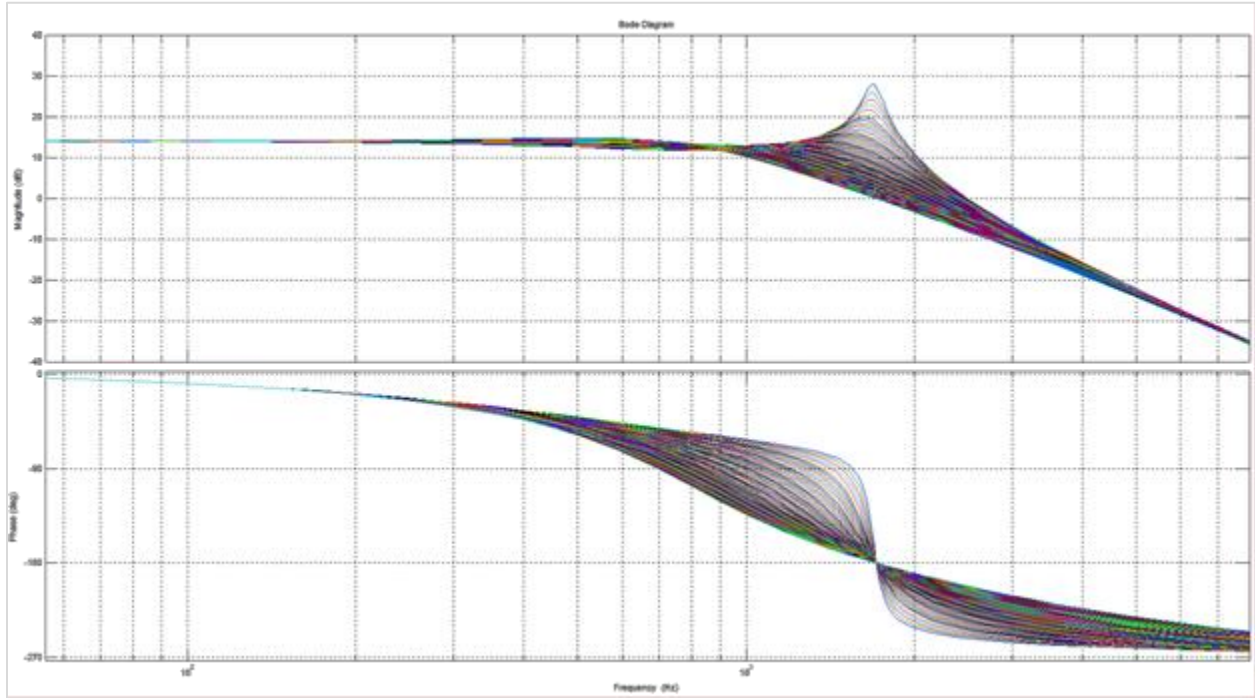


Figure 4. 34. Frequency characteristic of G_d as a function of K_r

Per Figure 4.34., low frequency and high frequency range disturbance rejection gets very little affected by increase in gain K_r . In medium frequency range, where resonance and some low order frequency harmonics are placed, increase in K_r value increases disturbance rejection, therefore drastically improving harmonic performance of a system.

Another analysis of the affect that proportional gain K_p has on the disturbance transfer function G_d , is based on the Figure 4.35. for $K_r=0.7$ and $T_d=0s$, where K_p varies in a range $\frac{0.001}{k_{pwm}} <$

$K_p < \frac{0.2}{k_{pwm}}$, in which system is stable.

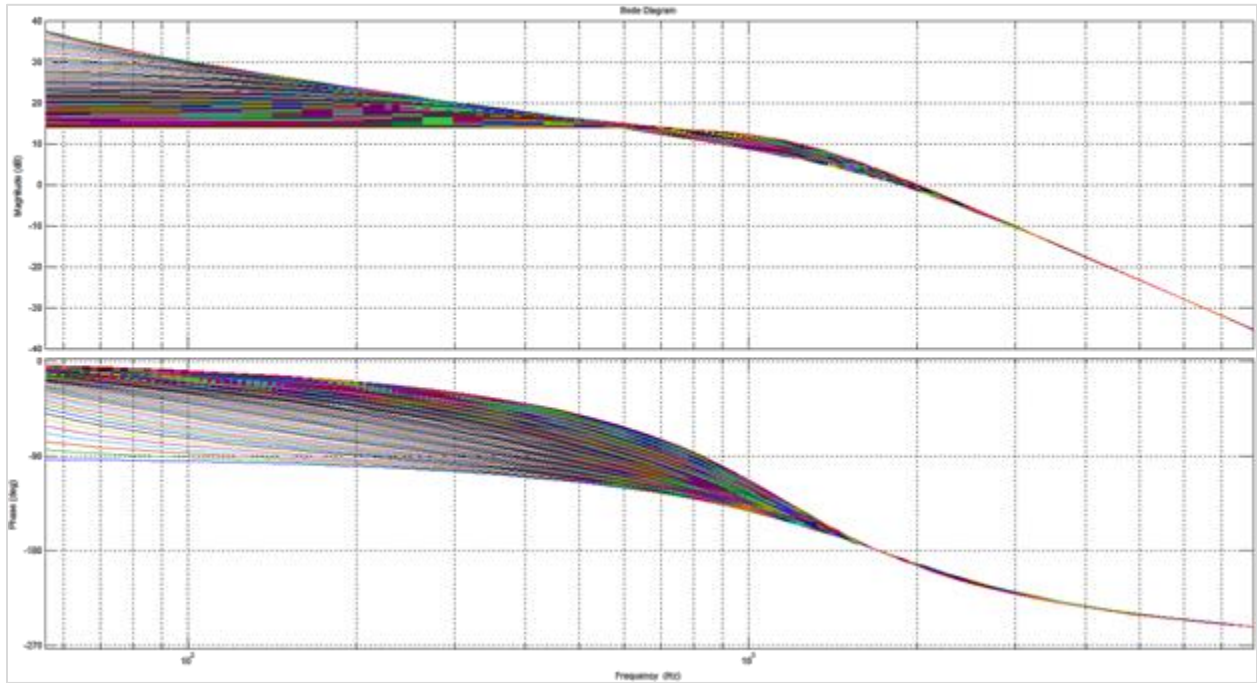


Figure 4. 35. Frequency characteristic of G_d as a function of K_p

Similar to passive damping case, increase in K_p has shown to increase disturbance rejection in low frequency range, and decrease it in medium frequency range. High frequency range does not get affected by the changes in proportional gain K_p .

For the evaluation of harmonic performance of actively damped MTI system, switching model of the system with all nonlinearities was simulated. DDPWM was used as a modulation technique at $c_f=69$ and full reactive power support to the grid, which was determined to represent the worst case scenario from harmonic performance perspective. Figure 4.36. shows TRD and STHD for first 10 and ranges of harmonics from 10 – 20, 20 – 30, 30 – 40, and 40 – 50 harmonics for $K_r = \frac{0.7}{k_{pwm}}$, $K_p = \frac{0.2}{k_{pwm}}$ and $T_d = 0$.

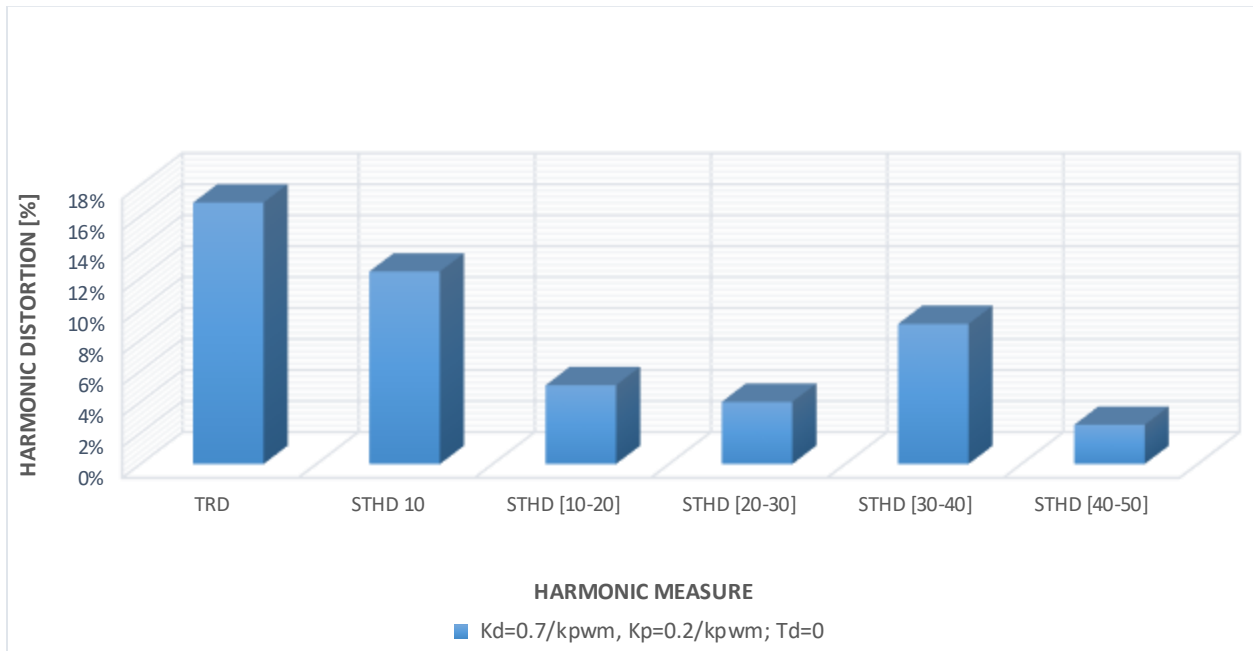


Figure 4. 36. TRD and STHD10/10-20/20-30/30-40/40-50 for actively damped system

Despite the careful selection of the control parameters, active damping technique shows poor harmonic performance that does not meet IEEE 1547 limits and is not in line with root locus and frequency characteristics analyzed previously. Mismatch between predicted and actual harmonic performance is better understood by looking at the individual harmonic value in the low order harmonic spectrum shown in Figure 4.37.

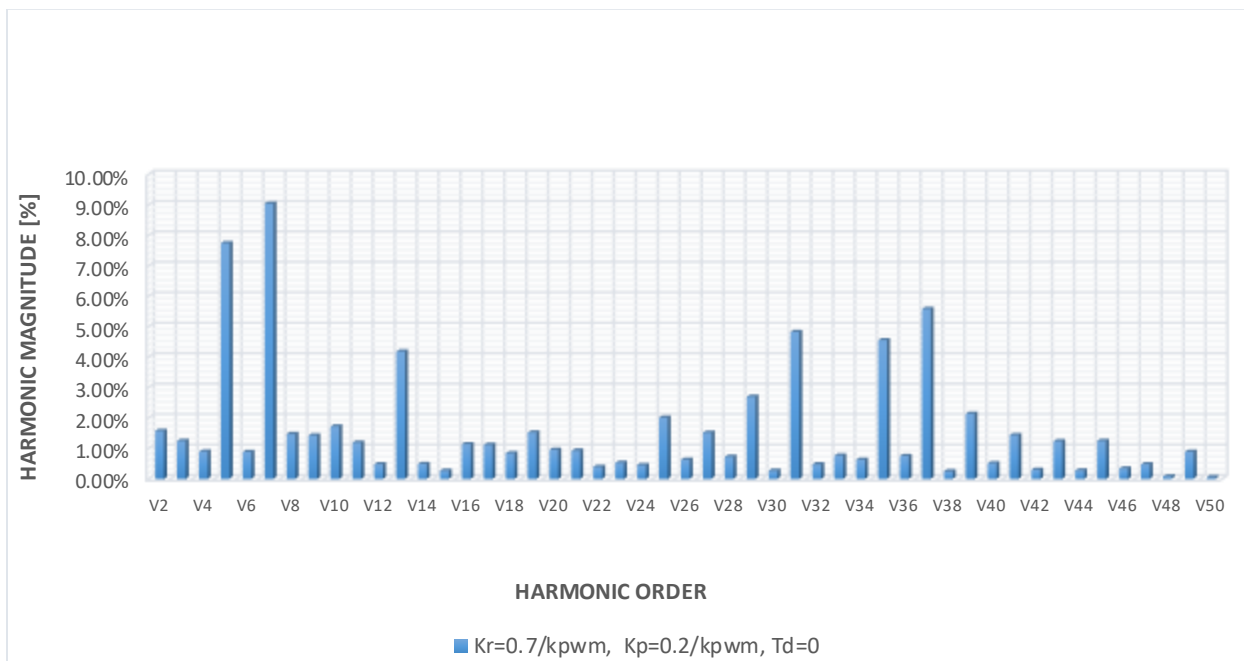


Figure 4. 37. Low order Harmonic spectrum for actively damped system

In addition to high harmonic content around resonance frequency, which is a sign of unsuccessful active resonance damping, 5th and 7th harmonics are unexpectedly high. Therefore, it is useful to look at the voltage modulation signal for one of the phases, coming out of the controller and entering DDPWM modulator, shown in Figure 4.38.

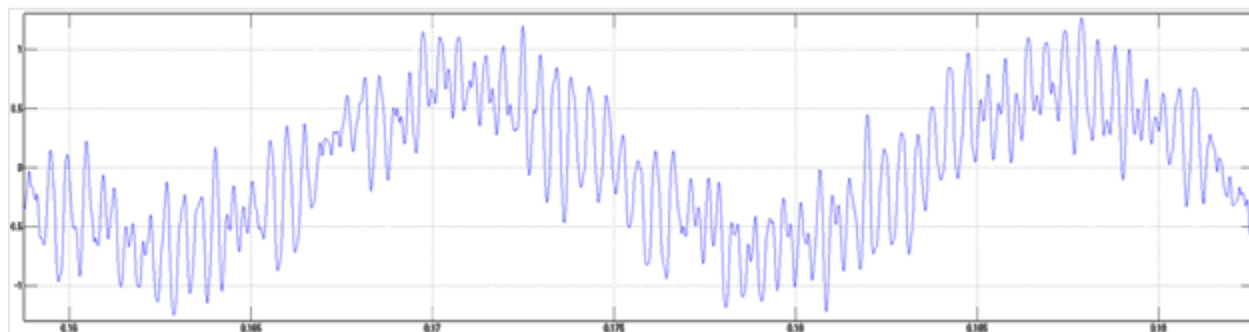


Figure 4. 38. Voltage modulation signal for one of the inverter phases

Modulation signal has a dominant fundamental harmonic component, but with very high harmonic content. High input harmonic content is a consequence of a filter capacitor current feedback multiplied by gain K_r , and added back to the control loop. These higher order input

harmonics are fed thru a modulator that has carrier frequency selected for fundamental frequency with high cf value, and that is not the case with high order input harmonics anymore. Therefore, additional sideband harmonics are created as a product of modulation as a consequence of lower equivalent cf for higher input harmonics. Also, even greater negative harmonic impact is made by additional input harmonic components creating periodic over modulation, which is known to cause very high weighted THD of the output voltage waveform, mostly due to very high 5th, 7th, 11th and 13th harmonic [69]. Therefore, it is fair to say that successful implementation of active damping represents a tradeoff between resonance damping and additional harmonics generated by modulator.

In order to successfully implement active damping, a following method is proposed:

- 1) Selection of control loop delay. It has been shown thru previous analysis that loop time delay has a major impact on stability and effectiveness of the active damping. Therefore, in order to successfully implement active damping, it is of great interest to minimize loop delay to the lowest possible value. That can be achieved by investing in faster digital control hardware such that the sampling rate is increased and control processing time is minimized. For the example used, sampling rate is selected as 10 times the switching frequency $f_s = 10f_{sw}$, and processing is considered to take one full time sample. In that case, total control loop time delay becomes $T_d = \frac{1.5}{20} \frac{1}{4140}$. With the current state of the art in digital control hardware, this is achievable with relatively inexpensive hardware.
- 2) Selection of controller parameters. PI controller parameters should be selected per instructions described in previous section. Basically, by assuming proper resonance damping, system is treated as a second order system for controller design purposes. Proportional gain K_p is selected based on the desired system phase margin, and integral

gain K_I is designed such that it has minor contribution on the phase margin value. For the exemplary case, for phase margin of $\rho = 77^\circ$ at $\omega_{co} = 646\text{Hz}$, $K_p = \frac{0.2}{k_{pwm}}$ and $K_I = \frac{2}{k_{pwm}}$

- 3) Selection of filter capacitor series resistor R_s . As previously discussed, series resistor R_s is used for passive resonance damping, but in this case its value is selected differently. It is selected such that its value is just enough to make closed loop system stable, for given K_p, K_I and T_d and in case where no active damping is applied. For selected example, the value is selected as $31.6\text{ m}\Omega$, which represents 19% of base impedance Z_b .
- 4) Selection of capacitor current feedback gain K_r . It has been demonstrated previously that K_r has a major effect on the performance of active damping algorithm by affecting resonance damping and introducing additional harmonics by “overexciting” the DDPWM modulator. Therefore, its value should be selected such that it represents the highest K_r value that does not affect harmonic performance of the system. $K_r = \frac{0.15}{k_{pwm}}$ was selected as the appropriate capacitor feedback gain for this example.

One very important observation to make is that a certain characteristic ratio of K_p/R_s value exists for a given T_d value, such that closed loop system without active damping is stable and resonance poles stay unchanged. For our example, this ratio is $\frac{K_p}{R_s} = \frac{6.3}{k_{pwm}} \frac{1}{\text{m}\Omega}$, and root locus for

$\frac{0.002}{k_{pwm}} < K_p < \frac{0.2}{k_{pwm}}$ and $0.19\% < R_s < 19\%$ is shown in Figure 4.39.

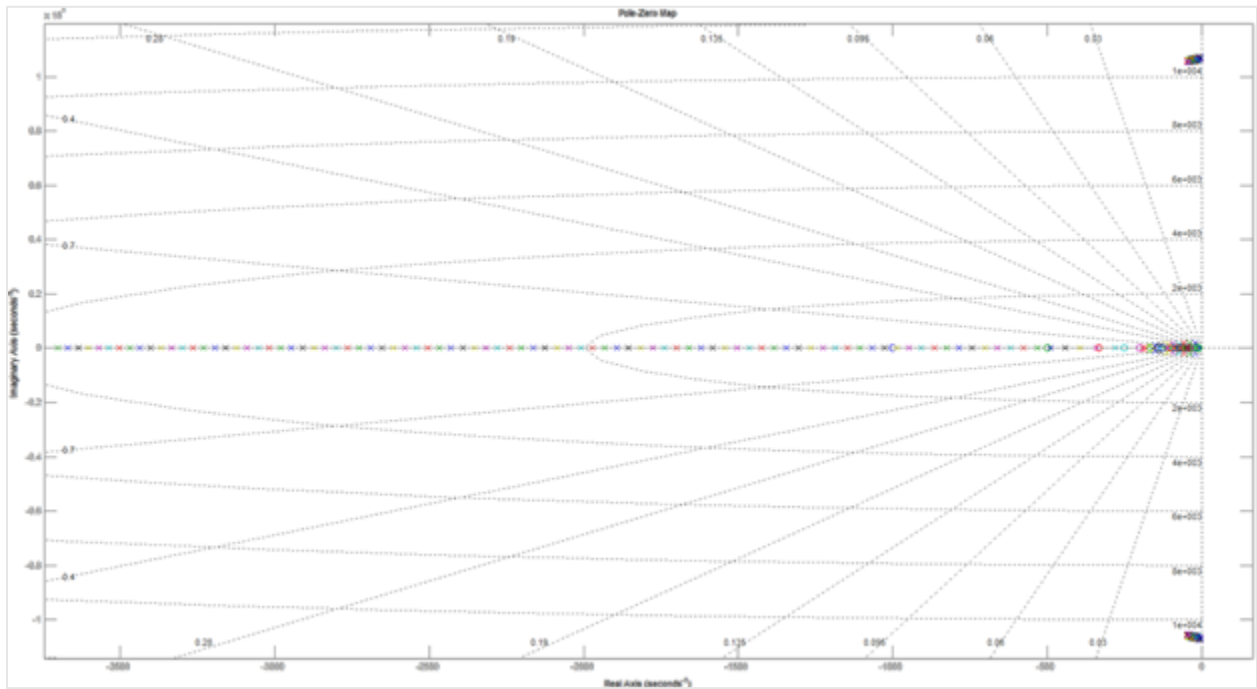


Figure 4. 39. Root Locus of G_{cl} as a function of K_p and R_s for $K_p/R_s = \text{const}$

Since power losses in resistor R_s is proportional to its value, in order to minimize losses and increase efficiency of the system, K_p needs to be reduced. Since lower K_p values lead to lower bandwidth of the closed loop system, a balance between efficiency and bandwidth needs to be made based on the system requirements.

Another criteria that active resonance damping solution needs to satisfy, is to maintain closed loop stability and disturbance rejection under high microgrid impedance values. Figure 4.40. shows a root locus of the closed loop function G_{cl} for line impedance variation $0\% < L_g < 20\%$ with $K_p = \frac{0.2}{K_{pwm}}$, $K_r = \frac{0.125}{K_{pwm}}$ and $T_d = \frac{1.5}{10 \cdot 4140}$ s. Increase in line impedance value increases damping of resonant poles, and improves stability of the closed loop system.

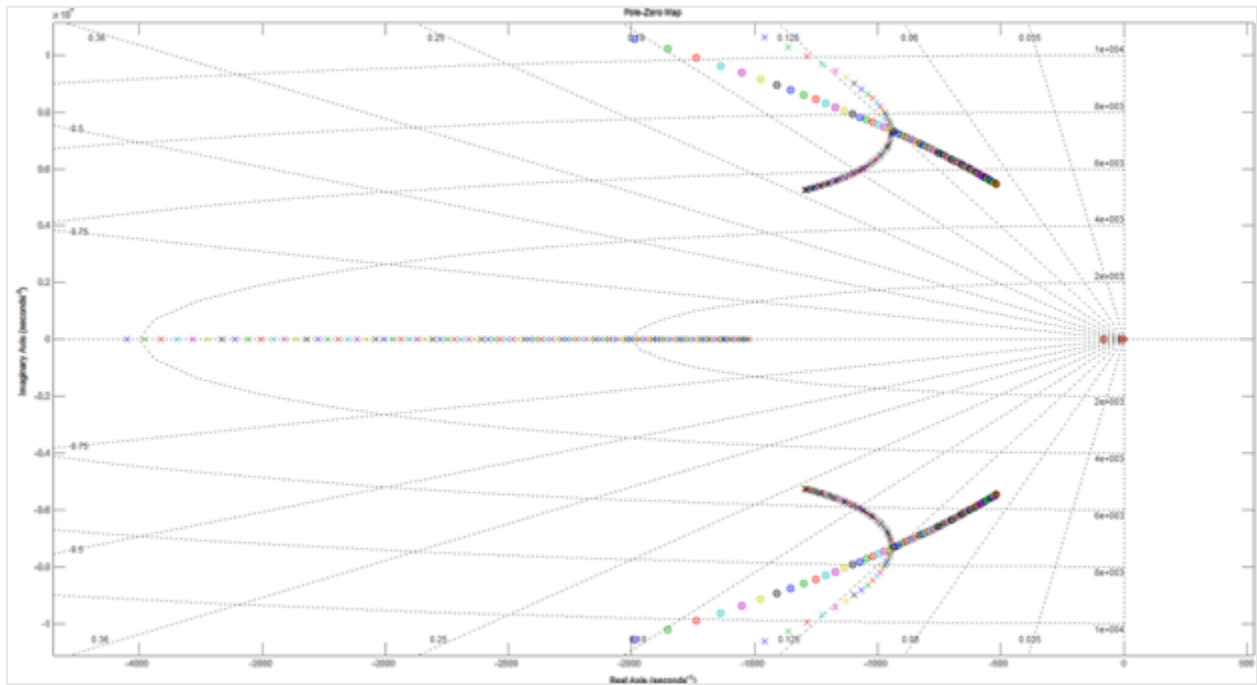


Figure 4. 40. Root Locus of G_{cl} as a function of L_g

Also, disturbance transfer function G_d as a function of L_g for the same range and values is shown in Figure 4.41.

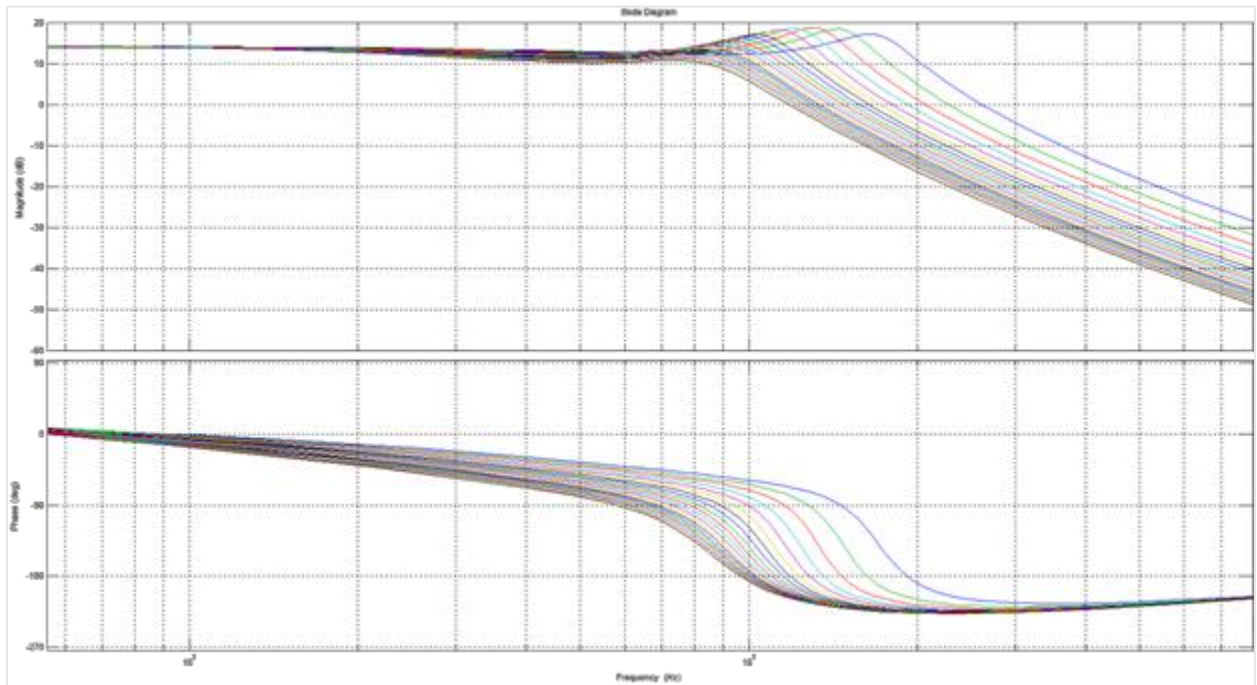


Figure 4. 41. Frequency characteristic of G_d as a function of L_g

Similar to passive damping case, higher line impedance values offer higher disturbance rejection in low and high frequency ranges, thus providing better harmonic performance. However, in the medium frequency range around resonant frequency, rise in line impedance values to a certain point decreases and then further increases disturbance rejection back again. Since resonant frequency decreases as well, decreased disturbance rejection is expected to be somewhat compensated by lower voltage harmonics produced.

For evaluation of harmonic performance of actively damped MTI system, it was tested with DDPWM at $c_f = 69$ and full reactive power support to the grid with previously selected parameters along with all the nonlinearities included in the simulation model. Figure 4.42.

compares first 50 harmonic values for two cases where $R_s = 30\%$ and $K_d = \frac{0.15}{k_{pwm}}$ and $R_s = 35\%$

and $K_d = \frac{0.14}{k_{pwm}}$ was used with $K_p = \frac{0.2}{k_{pwm}}$ with $T_d = \frac{1.5}{20*4140}$.

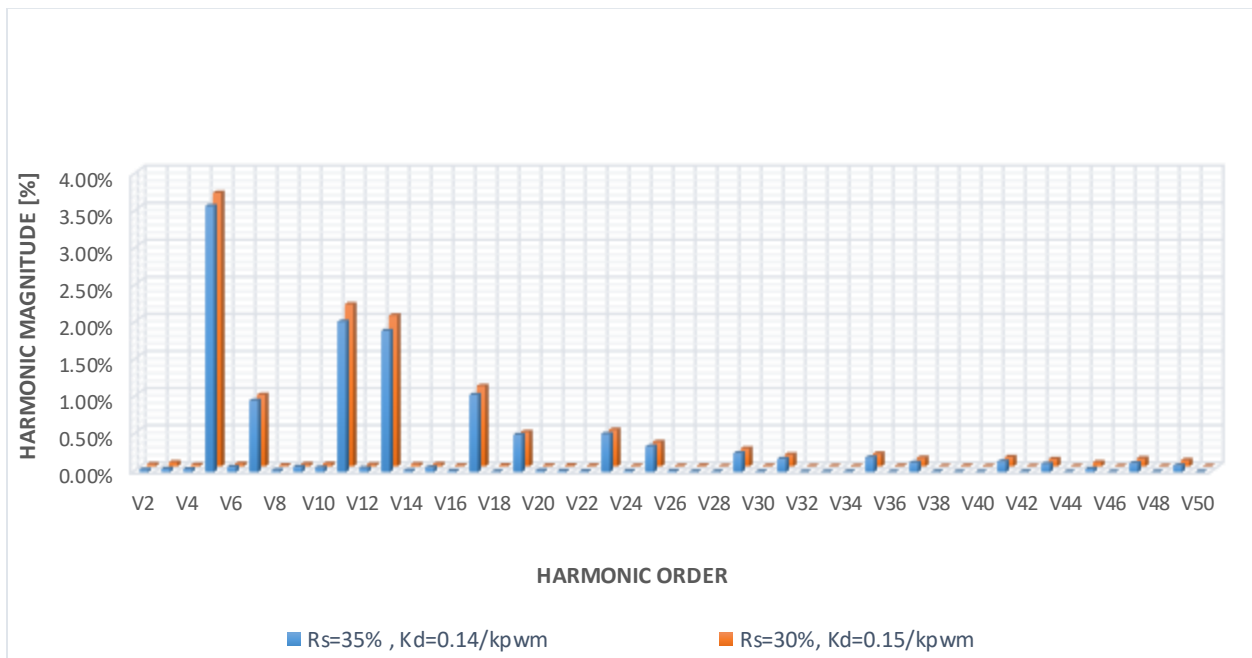


Figure 4. 42. Low order harmonic spectrum comparison between two actively damped cases

From Figure 4.42., it can be observed that with $R_s = 30\%$ and $K_d = 0.15$ system does not meet IEEE 1547 for individual harmonic values due to 11th and 13th harmonic being above 2% value. Therefore, damping resistor value had to be increased to $R_s = 35\%$ and capacitor current feedback gain reduced to $K_d = 0.14$.

Also, two cases were compared if Figure 16 in terms of TRD and STHD for first 10 and ranges of harmonics from 10 – 20, 20 – 30, 30 – 40, and 40 – 50 harmonics.

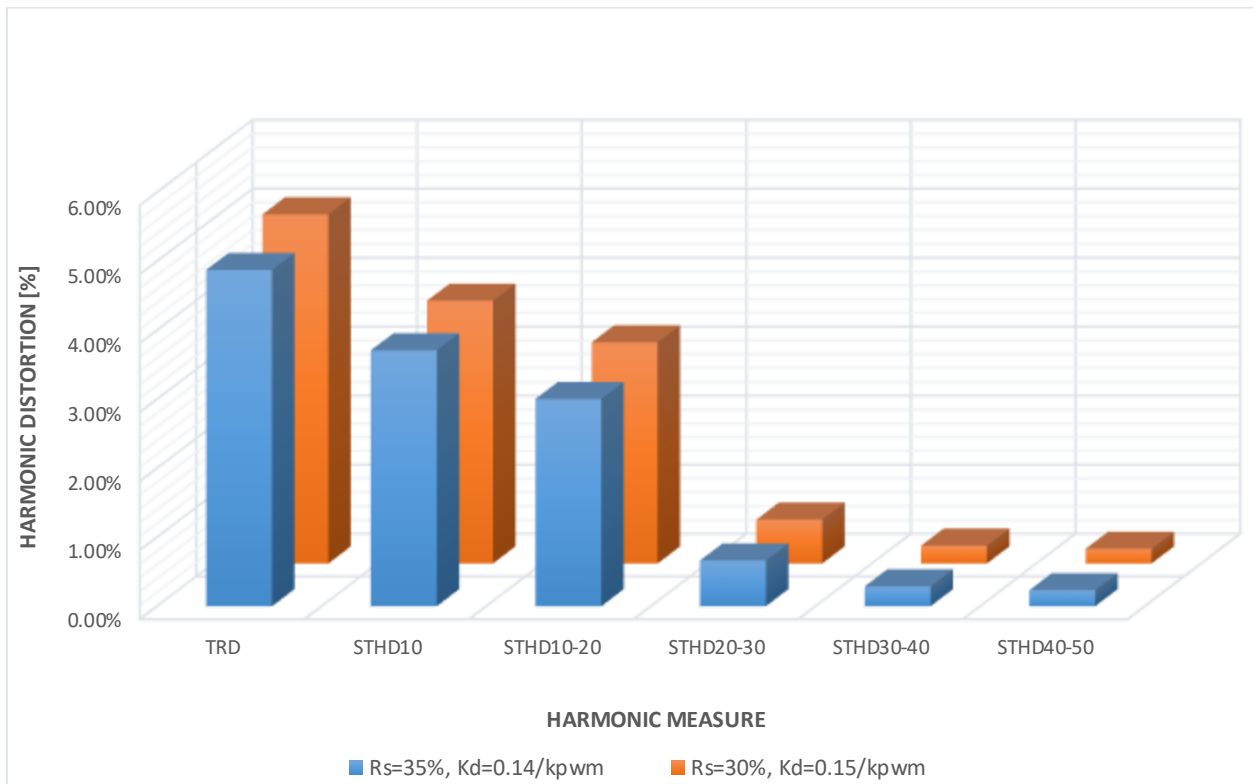


Figure 4. 43. TRD and STHD10/10-20/20-30/30-40/40-50 Comparison between a two actively damped cases

Figure 4.43. also shows that case where $R_s = 30\%$ and $K_d = \frac{0.15}{k_{pwm}}$ also does not meet IEEE 1547 requirement for $TRD < 5\%$, thus R_s had to be increased to 35% and new value of $K_d = \frac{0.14}{k_{pwm}}$ had to be used in order to meet TRD requirement.

4.7. Input Impedance of Closed Loop System

An important parameter of MTI system is the input impedance which defines a simple measure of sensitivity of closed loop system to various types of grid harmonic distortions. Early work has shown that small grid harmonic distortions can cause significant current distortions [70]. Also another early study reported in [65] has identified that the distortion is a consequence of a control scheme that is designed under the assumption of sinusoidal fundamental voltage supply. In order to be able to quantify the distortion impact, Input impedance is defined as a relationship between a grid voltage harmonic disturbance and resulting grid current harmonic. In ideal case it is desired for input impedance to be infinite for low order harmonics, such that inverter produces no current harmonics in the presence of distorted supply. A general block diagram of a closed loop MTI system with grid voltage E_g acting as an output disturbance on the plant G_i is shown in Figure 4.44.

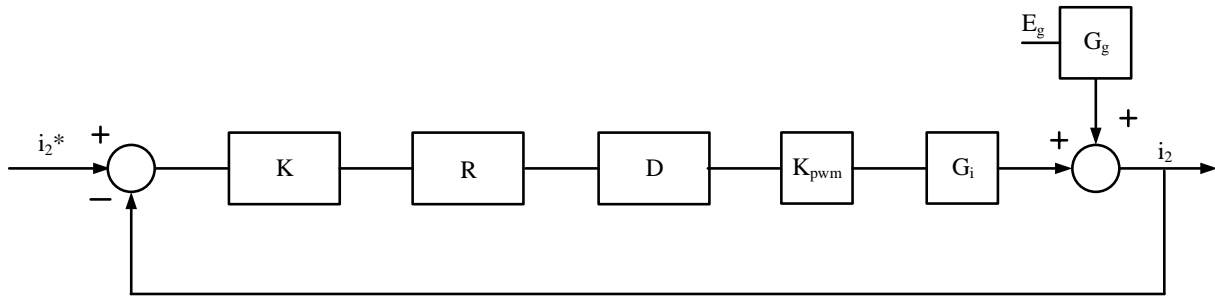


Figure 4. 44. Block Diagram of MTI system with grid voltage E_g acting as an output disturbance

As discussed previously in LCL filter design section, input impedance of a filter is indirectly considered during the filter parameter selection process. For an LCL filter, input impedance for each phase is defined as:

$$Z_{inLCL}(s) = -\frac{E_g(s)}{i_2(s)}$$

$$= \frac{s^3 C_f L_1 L_2 + s^2 C_f [L_1 (R_2 + R_c) + L_2 (R_1 + R_c)] + s [C_f (R_1 R_c + (R_2)(R_1 + R_c)) + L_1 + L_2] + R_1 + R_2}{s^2 C_f L_1 + s C_f (R_1 + R_c) + 1}$$

(4.32.)

Figure 4.45. shows the input harmonic impedance magnitude and phase versus frequency for filter parameter value calculated previously, for both undamped and passively damped filter with $R_c = 60\%$.

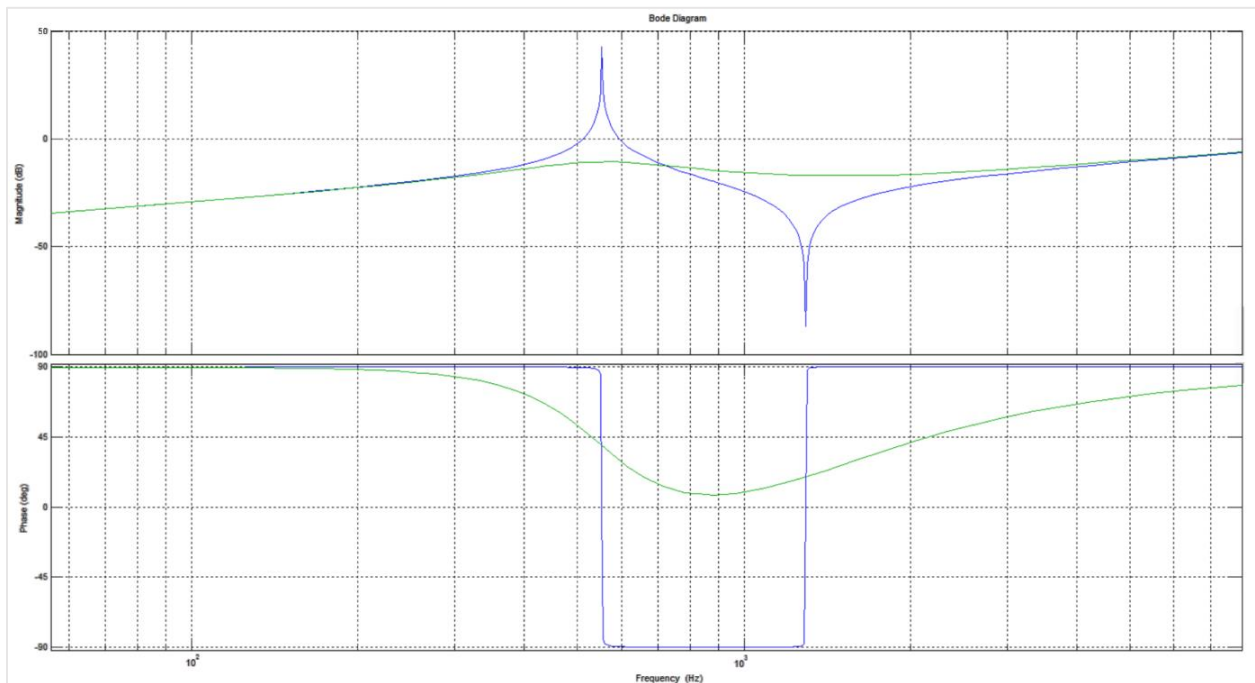


Figure 4. 45. Frequency characteristic of LCL Filter Input impedance for a)undamped b) passively damped filter

It can be seen from Figure 4.45. that undamped system impedance becomes minimal around resonant frequency, while the maximum is observed around antiresonant frequency. Also, absolute magnitude of impedance generally increases with frequency rise in both damped and undamped system cases. However, input impedance of an LCL filter basically represents an open loop harmonic response of system, which does not represent the actual input impedance of the

closed loop system. When closed loop system is considered, input impedance per each of the dq axis becomes:

$$Z_{indq}(s) = -\frac{E_g(s)}{i_2(s)} = -\frac{1 + K(s)D_d(s)k_{pwm} R(s)G_i(s)}{G_g(s)} \quad (4.33.)$$

For single loop controlled, passively damped system final input impedance transfer function turns out as:

$$Z_{indq}(s) = \frac{\frac{T_d}{2} A s^5 + \left(\frac{T_d}{2} B + A\right) s^4 + \left(\frac{T_d}{2} C + B + F\right) s^3 + \left(\frac{T_d}{2} D + C + G\right) s^2 + (D + H)s + K_I k_{pwm}}{E_2 \frac{T_d}{2} s^4 + \left(E_2 \frac{T_d}{2} + F_2 \frac{T_d}{2}\right) s^3 + \left(F_2 + \frac{T_d}{2}\right) s^2 + s} \quad (4.34.)$$

Where:

$$E_2 = C_f L_1$$

$$F_2 = C_f (R_1 + R_c)$$

A comparison of the frequency characteristic of input impedance for LCL filter and for closed loop system is shown in Figure 4.46. Parameters used are $K_p = \frac{0.2}{k_{pwm}}$, $K_I = \frac{12}{k_{pwm}}$, $R_s =$

$$60\%, T_d = \frac{1.5}{(20 \cdot 4140)}$$

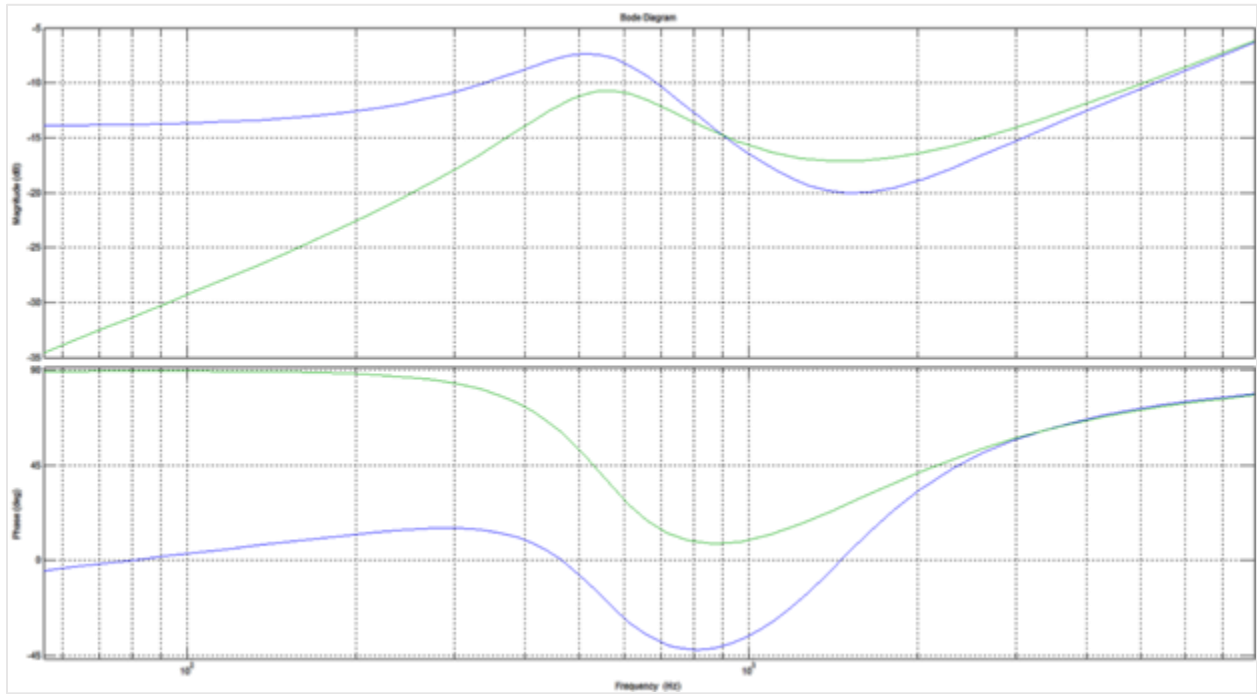


Figure 4. 46. Frequency characteristic of Input impedance for a) LCL Filter b) Closed loop system

Input impedance of a closed loop system shows higher magnitude values in low frequency range, thus leading to lower current harmonics. However, impedance magnitude drops around resonant frequency, therefore leading to worse harmonic performance in frequency range around resonant frequency.

Since closed loop system shows a significant difference in terms of input impedance magnitude, it is of interest to investigate the impact of controller parameters on input impedance.

Figure 4 shows a set of frequency characteristics of input impedance of a closed loop system for a

range of proportional gain values $\frac{0.002}{k_{pwm}} < K_p < \frac{0.2}{k_{pwm}}$.

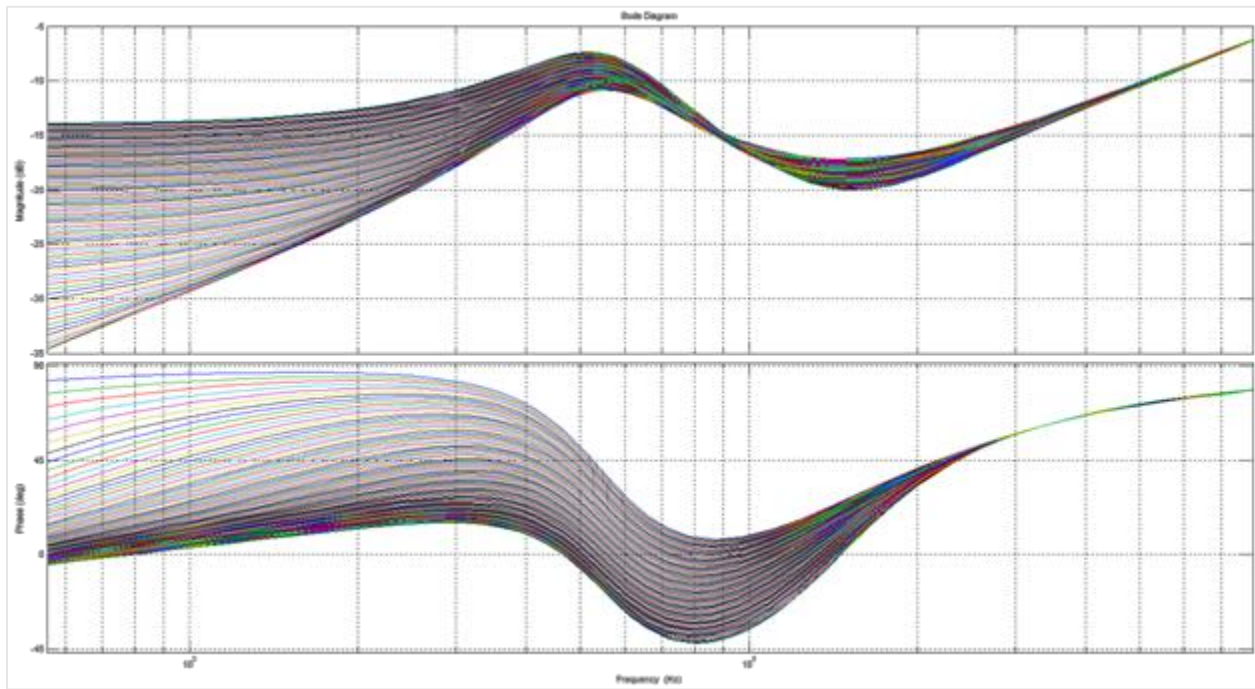


Figure 4. 47. Set of Frequency characteristics of Input impedance for K_p variation

Figure 4.47. shows that for higher levels of proportional gain K_p , grid current harmonics induced by grid distortions will decrease. On the other hand, it also shows that higher levels of proportional gain K_p lead to higher possibility of resonance excitation due to lower impedance values in that frequency range. This is in line with conclusions made previously, where higher levels of K_p also led to lower input disturbance rejection of the disturbance transfer function Gd in resonance frequency range, and higher disturbance rejection in low frequency range, under the assumption of same damping resistor value R_s , thus affecting harmonic performance of the system even on an undistorted grid supply. Therefore, it is fair to say that for a given damping resistor value R_s , selection of K_p represents a tradeoff between system bandwidth and low frequency harmonic performance on one side, and resonant frequency harmonic performance on other side.

Finally, impact of additional line impedance on input impedance of a closed loop MTI system is very important to evaluate. Figure 4.48. shows a set of frequency characteristics of input impedance of a closed loop system for a range of Line impedance values $0 < L_g < 20\%$.

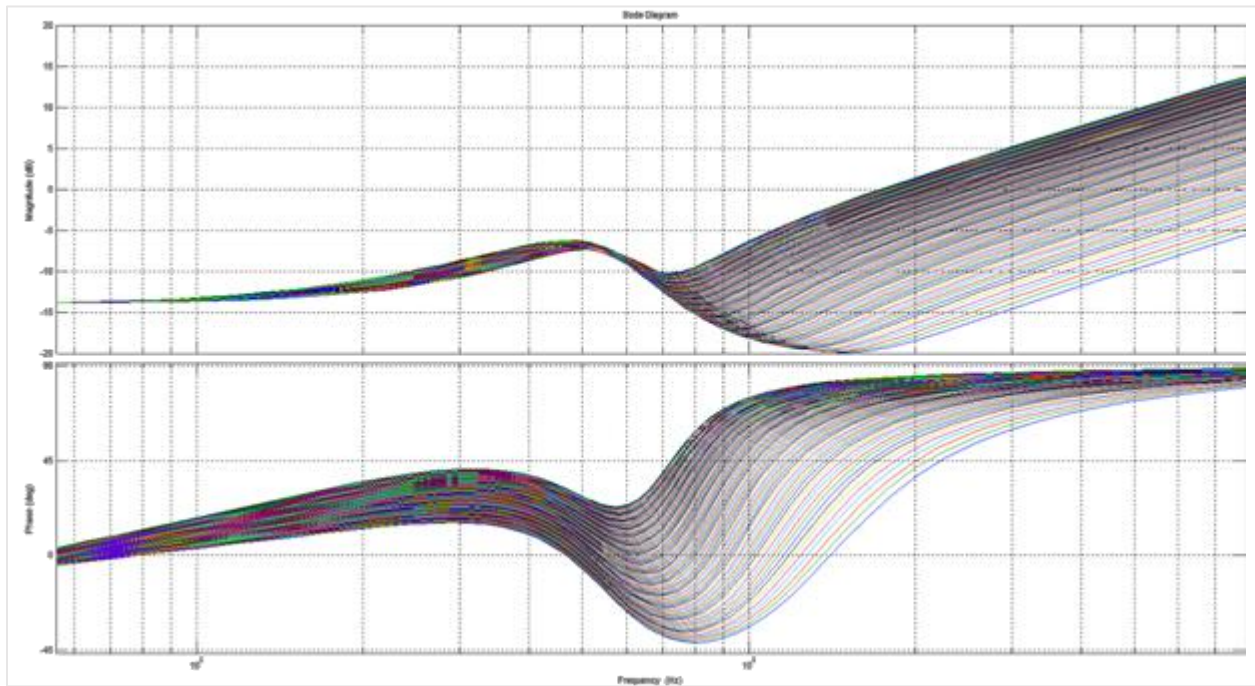


Figure 4. 48. Set of Frequency characteristics of Input impedance for L_g variation

The impact of added line impedance is that it increases the input impedance value throughout the whole frequency range, but the magnitude difference is very frequency dependent, such that the impact is more significant with the higher frequency values. Also another significant impact is that the additional line impedance decreases frequency value at which resonance occurs, which was also observed in previously in chapter 3.3.1.2.

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5. Decoupled Power and Grid Feedforward Control

As per derivations in chapter 3.3.3., after applying three to two phase and stationary to the synchronous reference frame transformations for a balanced three-phase system, the following set of equations describes the voltage and the current conditions on the LCL filter:

$$\frac{di_{d1}}{dt} = -\frac{R_1 + R_c}{L_1}i_{d1} - \omega i_{q1} + \frac{R_c}{L_1}i_{d2} - \frac{V_{fd}}{L_1} + \frac{E_{id}}{L_1} \quad (5.1.)$$

$$\frac{di_{d2}}{dt} = \frac{R_c}{L_2}i_{d1} + \frac{R_2 + R_c}{L_2}i_{d2} - \omega i_{q2} + \frac{V_{fd}}{L_2} - \frac{E_{gd}}{L_2} \quad (5.2.)$$

$$\frac{dV_{fd}}{dt} = \frac{1}{C}i_{d1} - \frac{1}{C}i_{d2} - \omega V_{fq} \quad (5.3.)$$

$$\frac{di_{q1}}{dt} = \omega i_{d1} - \frac{R_1 + R_c}{L_1}i_{q1} + \frac{R_c}{L_1}i_{q2} - \frac{V_{fq}}{L_1} + \frac{E_{iq}}{L_1} \quad (5.4.)$$

$$\frac{di_{q2}}{dt} = \frac{R_c}{L_2}i_{q1} + \omega i_{d2} + \frac{R_2 + R_c}{L_1}i_{q2} + \frac{V_{fq}}{L_2} - \frac{E_{gq}}{L_2} \quad (5.5.)$$

$$\frac{dV_{fq}}{dt} = \frac{1}{C}i_{q1} - \frac{1}{C}i_{q2} + \omega V_{fd} \quad (5.6.)$$

It should be noted that since there is no additional elements or connections in the neutral path, the o axis set of equations have been omitted. Fig. 5.1. shows the equivalent circuit model in the synchronous dq reference frame.

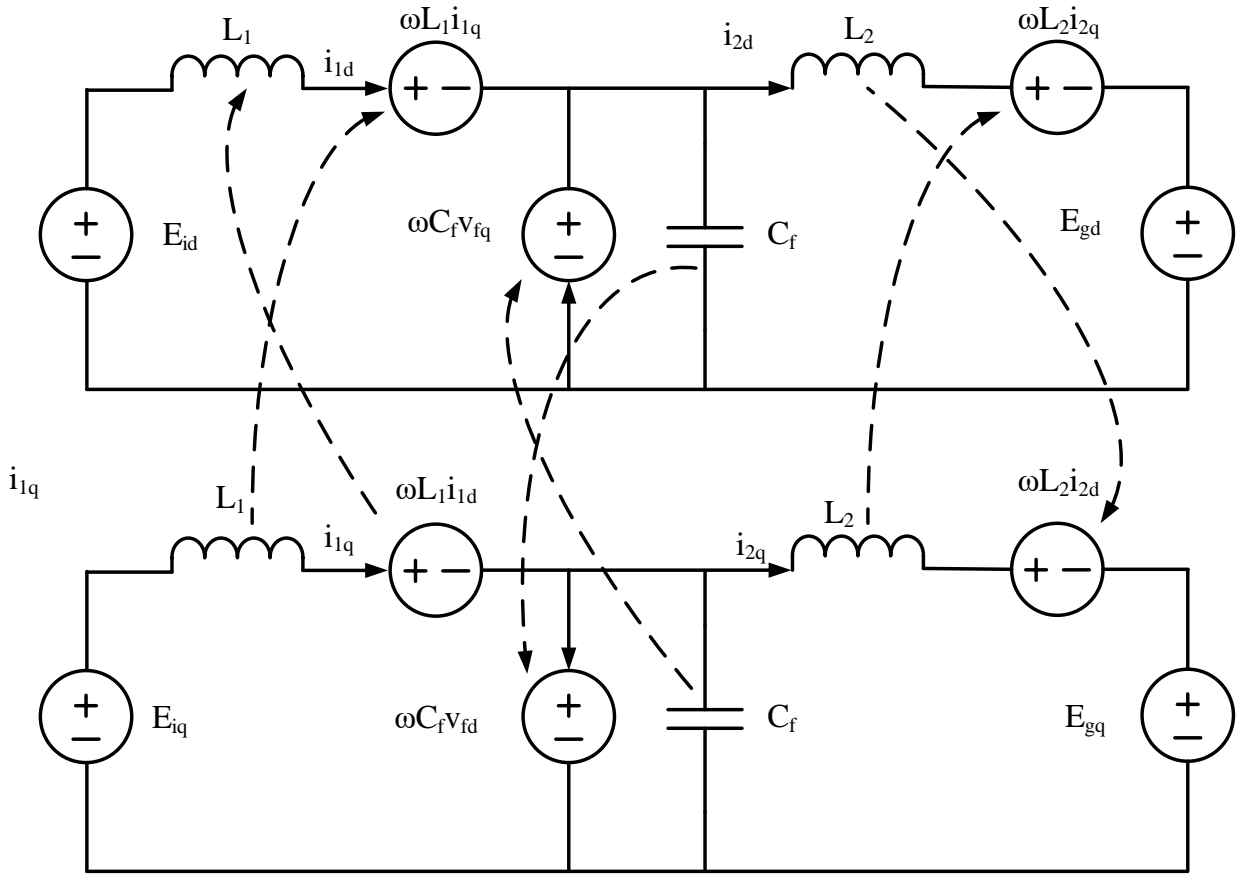


Figure 5. 1. Circuit Model of the LCL filter in the synchronous reference frame

In order to derive a transfer function based block diagram, equations are rearranged and represented in Laplace domain:

$$i_{d1}(sL_1 + R_1 + R_c) = -\omega L_1 i_{q1} + R_c i_{d2} - V_{fd} + E_{id} \quad (5.7.)$$

$$i_{d2}(sL_2 + R_2 + R_c) = R_c i_{d1} - \omega L_2 i_{q2} + V_{fd} - E_{gd} \quad (5.8.)$$

$$sC V_{fd} = i_{d1} - i_{d2} - \omega C V_{fq} \quad (5.9.)$$

$$i_{q1}(sL_1 + R_1 + R_c) = \omega L_1 i_{d1} + R_c i_{q2} - V_{fq} + E_{iq} \quad (5.10.)$$

$$i_{q2}(sL_2 + R_2 + R_c) = R_c i_{q1} + \omega L_2 i_{q2} + V_{fq} - E_{gq} \quad (5.11.)$$

$$sC V_{fq} = i_{q1} - i_{q2} + \omega C V_{fd} \quad (5.12.)$$

The block diagram of the LCL filter in the synchronous reference frame is presented in Fig. 5.2.

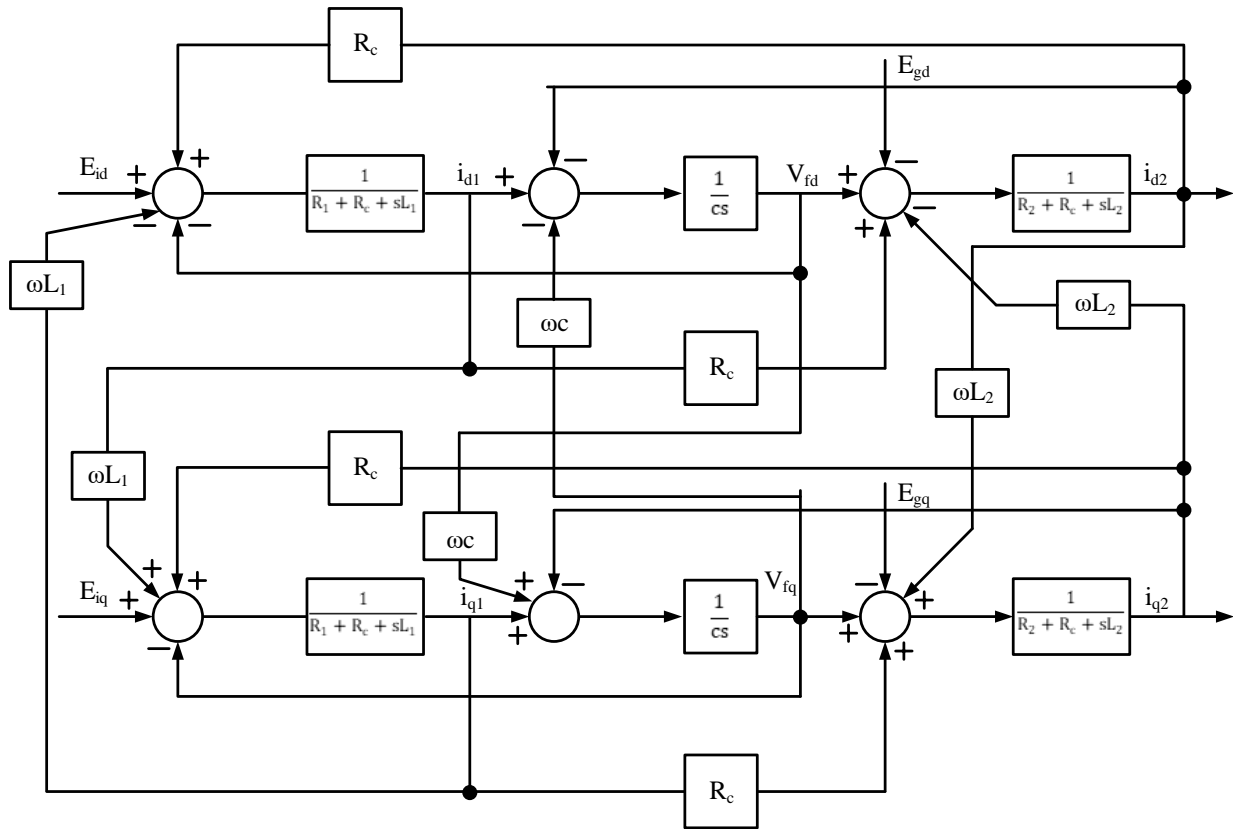


Figure 5. 2. Block diagram of the LCL filter in the synchronous reference frame

Looking at the block diagram, there is an obvious cross coupling between the d – axis and q – axis which includes all the existing states (V_f, I_1 and I_2) of the opposite axis. Dqo transformation creates cross-couplings between d – axis and q – axis variables [1, 2, 3]. This has impact on the individual control of active and reactive power and needs to be mitigated in order to maintain system performance. Also, in applications where low sampling frequency is used, coupling has shown to cause stability problems [1], [4-6]. LCL filter based inverter system has shown to have much more complicated couplings in comparison to L filter [7-9]. Despite the differences in complexity, [10], has addressed coupling problem by treating the LCL filter as a plain L filter by neglecting the filter capacitor value. Other more complex decoupling strategies have been proposed which are based either on state-feedback decoupling [11] or capacitor voltage feedforward decoupling [12].

In order to minimize undesirable coupling transients of coupled axis, provide better tracking capability, achieve zero steady state error and better robustness these cross coupling terms need to be compensated.

All three coupling states along with grid side voltage measurement E_{cc} can be treated as a disturbance signal, which leads to the following state space model for each axis:

$$\frac{d}{dt} \begin{bmatrix} i_{dq1} \\ i_{dq2} \\ V_{dqf} \end{bmatrix} = \begin{bmatrix} -\frac{R_1+R_c}{L_1} & \frac{R_c}{L_1} & -\frac{1}{L_1} \\ \frac{R_c}{L_2} & -\frac{R_2+R_c}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_{dq1} \\ i_{dq2} \\ V_{dqf} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \end{bmatrix} [E_{dqi}] + \begin{bmatrix} 0 & -/+ \omega & 0 & 0 \\ -\frac{1}{L_2} & 0 & -/+ \omega & 0 \\ 0 & 0 & 0 & -/+ \omega \end{bmatrix} \begin{bmatrix} E_{dqcc} \\ i_{qd1} \\ i_{qd2} \\ V_{qdf} \end{bmatrix} \quad (5.13.)$$

The best way of compensating the disturbance signal effect on the output is by adding feed forward signals to the outputs of the current regulators, which in this case would be plant model input, which are directly proportional to the inverter output voltages. Generally, adding feedforward control to the control algorithm can significantly improve performance of a feedback based system whenever there is a major disturbance that can be measured before it affects the system output. In the ideal case, feedforward control can completely eliminate the effect of the measured disturbance on the output. Feedforward control is especially useful in cases where the measurements for each of the disturbances are already available. In the grid tie inverter case, due to synchronization and protection reasons, all of the disturbances (V_f , I_1 , I_2 and V_g) acting on one axis can be either directly measured or calculated based on the existing measurements. Figure 5.3. gives the traditional block diagram of a feedforward control system.

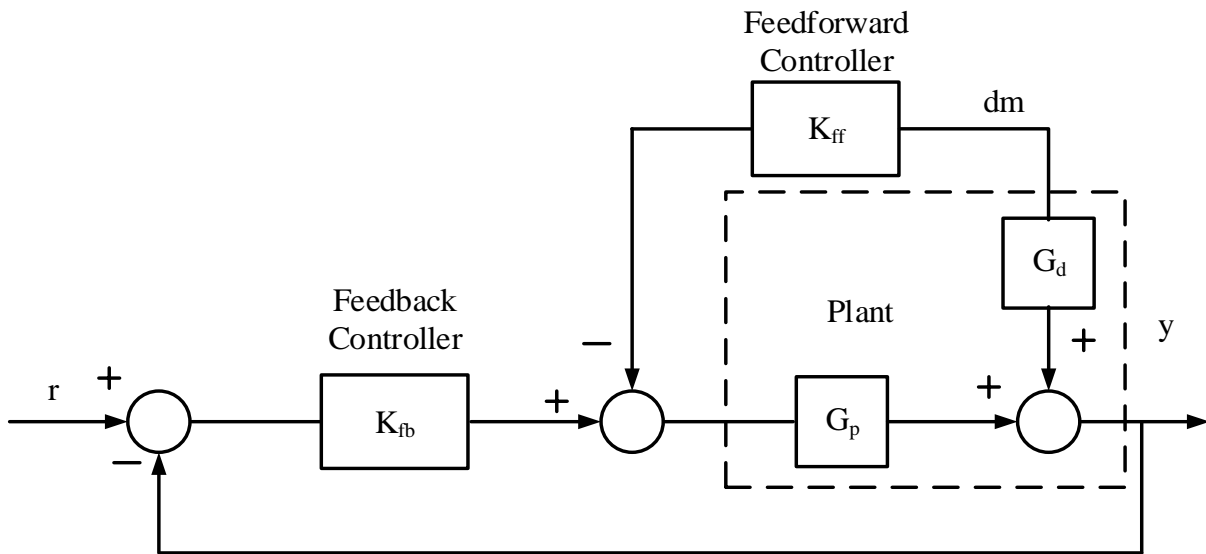


Figure 5. 3. Traditional feedforward control diagram

The transfer function between the process output y and the measured disturbance d_m from Figure 5.3. is:

$$\frac{y(s)}{d_m(s)} = \frac{(G_d - G_p K_{ff})}{1 + K_{fb} G_p} \quad (5.14.)$$

To eliminate the effect of the measured disturbance, we need to select K_{ff} so that

$$G_d - G_p K_{ff} = 0 \quad (5.15.)$$

From which:

$$K_{ff}(s) = G_p^{-1}(s) G_d(s) \quad (5.16.)$$

The conditions for making this possible are:

- $K_{ff}(s)$ must be stable since it acts in open loop.

- $K_{ff}(s)$ should be proper since future disturbances are unknown. In order to ensure that $K_{ff}(s)$ is proper, excess poles at high frequency can be introduced when needed:

$$K_{ff}(s) = \frac{G_p^{-1}(s)G_d(s)}{\left(\frac{s}{\omega_c} + 1\right)^\delta} \quad (5.17.)$$

Where δ is the relative degree of $G_p^{-1}(s)G_d(s)$, and ω_c is large, at least a few times maximum bandwidth of $d_m(s)$.

By applying the previous set of equations onto the LCL filter equations for $d - axis$ and $q - axis$, the following results are obtained:

$$G_p = \frac{sC_f R_c + 1}{s^3 C_f L_1 L_2 + s^2 C_f [L_1(R_2 + R_c) + L_2(R_1 + R_c)] + s[C_f(R_1 R_c + R_2(R_1 + R_c)) + L_1 + L_2] + R_1 + R_2} \quad (5.18.)$$

$$\begin{aligned} G_{dd1} &= -\omega L_1 \frac{sC_f R_c + 1}{s^3 C_f L_1 L_2 + s^2 C_f [L_1(R_2 + R_c) + L_2(R_1 + R_c)] + s[C_f(R_1 R_c + R_2(R_1 + R_c)) + L_1 + L_2] + R_1 + R_2} \\ &= -G_{dq1} \quad (5.19.) \end{aligned}$$

$$\begin{aligned} G_{dd2} &= -\omega C \frac{sL_1 + R_1}{s^3 C_f L_1 L_2 + s^2 C_f [L_1(R_2 + R_c) + L_2(R_1 + R_c)] + s[C_f(R_1 R_c + R_2(R_1 + R_c)) + L_1 + L_2] + R_1 + R_2} \\ &= -G_{dq2} \quad (5.20.) \end{aligned}$$

$$\begin{aligned} G_{dd3} &= -\omega L_2 \frac{(s^2 C_f L_1 + sC_f(R_1 + R_c) + 1)}{s^3 C_f L_1 L_2 + s^2 C_f [L_1(R_2 + R_c) + L_2(R_1 + R_c)] + s[C_f(R_1 R_c + R_2(R_1 + R_c)) + L_1 + L_2] + R_1 + R_2} \\ &= -G_{dq3} \quad (5.21.) \end{aligned}$$

$$\begin{aligned} G_{dd4} &= -\frac{(s^2 C_f L_1 + sC_f(R_1 + R_c) + 1)}{s^3 C_f L_1 L_2 + s^2 C_f [L_1(R_2 + R_c) + L_2(R_1 + R_c)] + s[C_f(R_1 R_c + R_2(R_1 + R_c)) + L_1 + L_2] + R_1 + R_2} \\ &= G_{dq4} \quad (5.22.) \end{aligned}$$

$$K_{ffd1} = -\omega L_1 = -K_{ffq1} \quad (5.23.)$$

$$K_{ffd2} = -\omega C \frac{sL_1 + R_1}{sC_f R_c + 1} = -K_{ffq2} \quad (5.24.)$$

$$K_{ffd3} = -\omega L_2 \frac{s^2 C_f L_1 + sC_f (R_1 + R_c) + 1}{(sC_f R_c + 1) \left(\frac{s}{\omega_c} + 1 \right)} = -K_{ffq3} \quad (5.25.)$$

$$K_{ffd4} = \frac{s^2 C_f L_1 + sC_f (R_1 + R_c) + 1}{(sC_f R_c + 1) \left(\frac{s}{\omega_c} + 1 \right)} = K_{ffq4} \quad (5.26.)$$

Depending on the final design of the grid tie inverter, number and placement of the voltage and current sensors may vary. Along with the variation varies the actual implementation of the decoupling strategy. In order to implement decoupling strategy per previous set of equations, the required measurement signals for the cross coupling and disturbance compensation are all three states (grid side current I_2 , inverter side current I_1 and filter capacitor voltage V_f) and voltage at the point of common coupling E_g . However in the actual setup, rarely will the measurements of all states along with the output voltage be available. Therefore, some additional equation rearrangements need to be performed in order to accommodate for the available measurement signals. The following calculation example is based on the grid side voltage measurements E_g and inverter branch I_1 and capacitor branch I_c current measurements in all three phases as per figure 5.4.

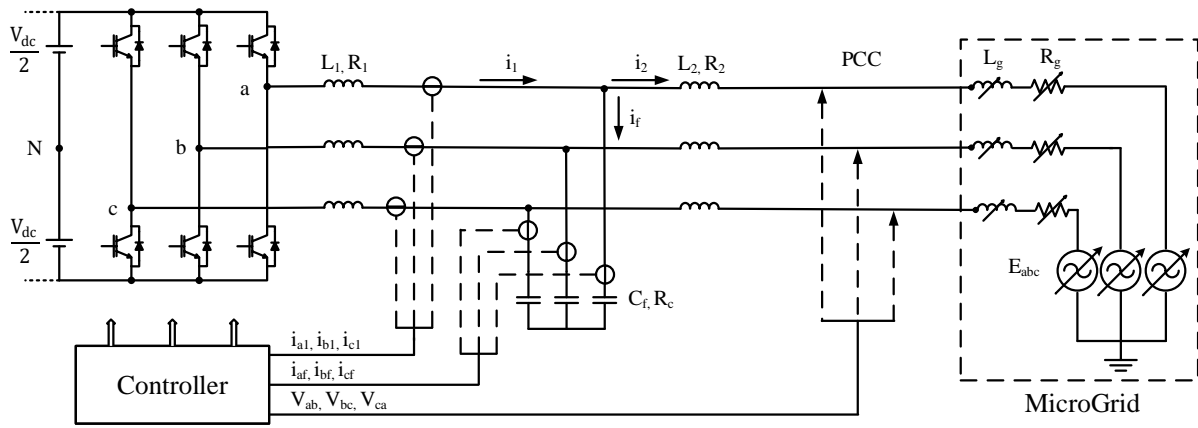


Figure 5. 4. Three phase equivalent circuit

Grid side voltage measurements E_{cc} should be always available because of the necessary grid voltage synchronization. Inverter branch I_1 and capacitor branch I_c current measurements were selected as the first choice because the sum of the two currents provides a grid side current value which is the ultimate goal for the higher-level control of the grid tie inverter. Also, each of the current sensors provide measurement signals that are essential for the protection and better performance of the inner loop controller. That leads to the following set of equations:

$$I_{dq2} = I_{dq1} - I_{dqf} \quad (5.27.)$$

$$V_{dqf} = \frac{I_{dqf}}{sC_f} \quad (5.28)$$

When directly inserted into the feedforward loop, they result in a final set of equations:

$$K_{ffd1} = -\omega L_1 - \omega L_2 \frac{s^2 C_f L_1 + s C_f (R_1 + R_c) + 1}{(s C_f R_c + 1) \left(\frac{s}{\omega_c} + 1 \right)} = -K_{ffq1} \quad (5.29.)$$

$$K_{ffd2} = -\frac{\omega s L_1 + R_1}{s s C_f R_c + 1} + \omega L_2 \frac{s^2 C_f L_1 + s C_f (R_1 + R_c) + 1}{(s C_f R_c + 1) \left(\frac{s}{\omega_c} + 1 \right)} = -K_{ffq2} \quad (5.30.)$$

$$K_{ffd4} = \frac{s^2 C_f L_1 + s C_f (R_1 + R_c) + 1}{(s C_f R_c + 1) \left(\frac{s}{\omega_c} + 1 \right)} = K_{ffq4} \quad (5.31.)$$

The block diagram of the LCL filter in the synchronous reference frame with a feedforward compensation for axis decoupling and disturbance compensation is presented in Fig. 5.5.

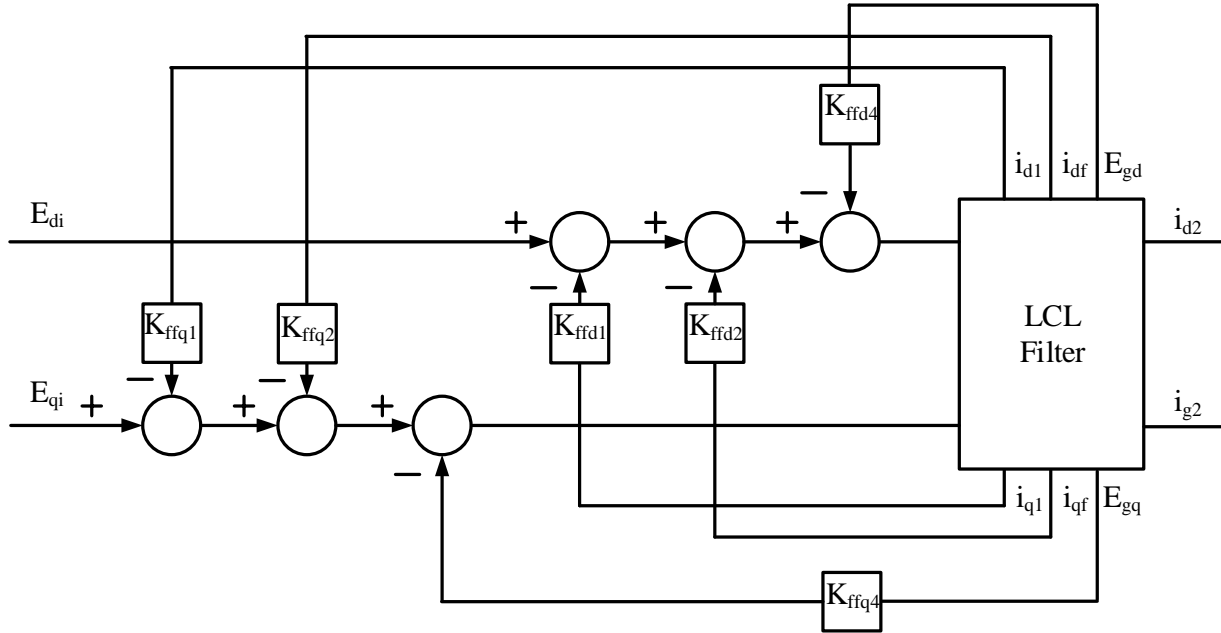


Figure 5. 5. Block diagram of the LCL filter in the synchronous reference frame

After feedforward compensation has been implemented for compensation of all three coupling states along with disturbance signal, decoupled state space model for each axis can be approximated by:

$$\frac{d}{dt} \begin{bmatrix} i_{dq1} \\ i_{dq2} \\ V_{dqf} \end{bmatrix} \approx \begin{bmatrix} -\frac{R_1 + R_c}{L_1} & \frac{R_c}{L_1} & -\frac{1}{L_1} \\ \frac{R_c}{L_2} & -\frac{R_2 + R_c}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_{dq1} \\ i_{dq2} \\ V_{dqf} \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} [E_{dqi}] \quad (5.32.)$$

The approximated equivalent block diagram of the LCL filter in the synchronous reference frame with a feedforward compensation for axis decoupling and disturbance compensation is presented in Fig. 5.6.

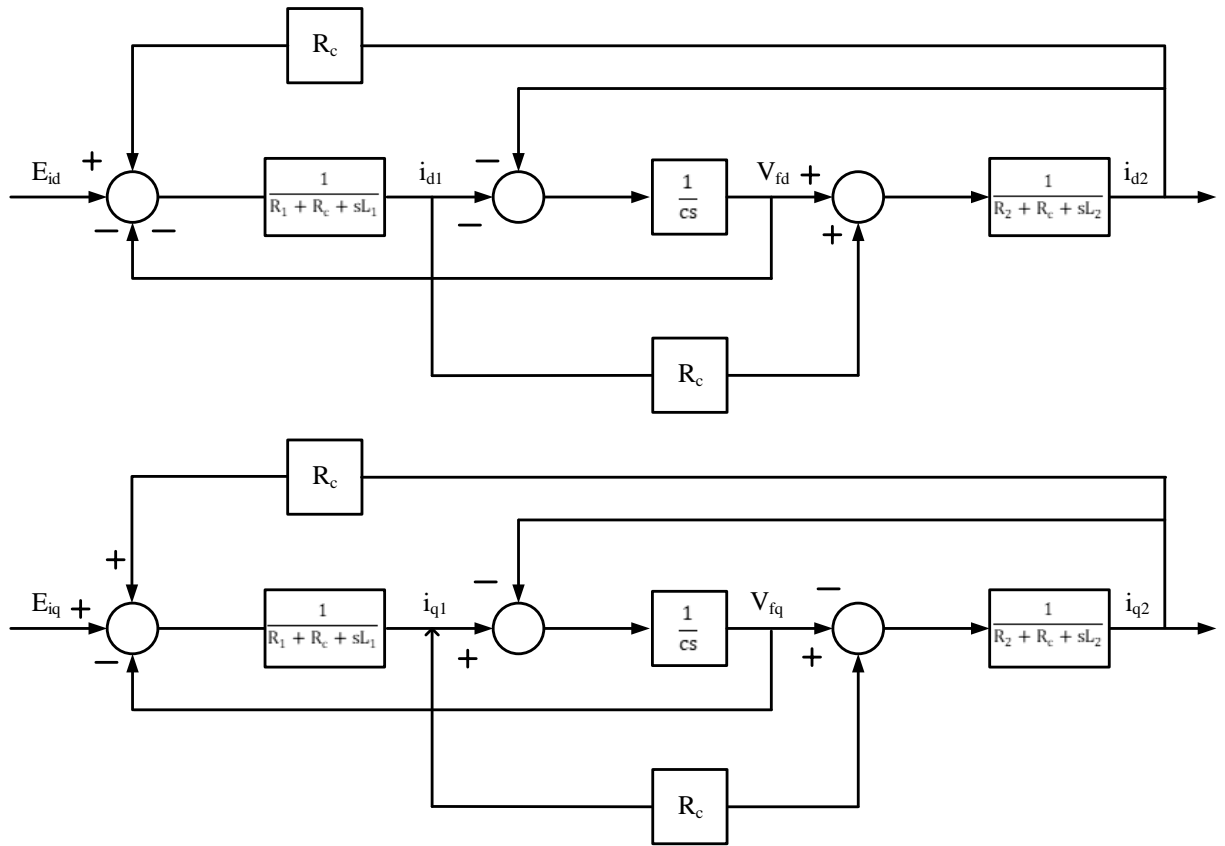


Figure 5. 6. Approximated equivalent block diagram of the LCL filter in the synchronous reference frame

5.1. Decoupled Control of DQ Axis Current Components

Introduction of decoupling allows the dqo filter model to be analyzed on a per axis basis, which is useful for derivation of closed loop system equations. Comparison in response to a consecutive step function in I_{d2} and I_{q2} reference between no solution and proposed decoupling solution are shown in figure 5.7. for an ideal non-switched model of a system, with all the system and controller parameters used as selected in previous chapter. Reference step functions were applied at different time instances in each axis and the output current responses were observed.

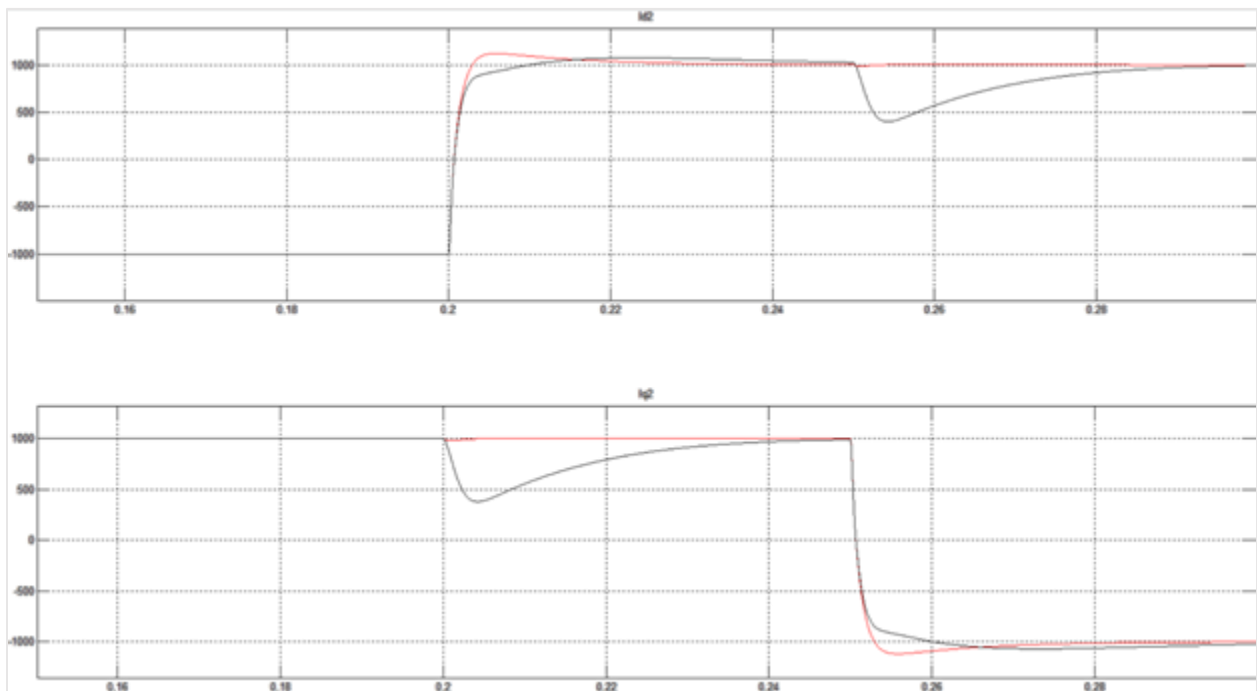


Figure 5. 7. I_{d2} and I_{q2} response to consecutive reference step change for no solution and feedforward based decoupling solution

As opposed to no solution, newly proposed decoupling solution practically shows no impact of a reference step change in one axis on a response in another axis. In order to evaluate the actual response of a switched system, Figure 5.8. compares a reference step response of a switched to a non-switched system. Switched system is implemented with all the nonlinearities and physical limitations, described in chapter 2.5, that non-switched system does not include.

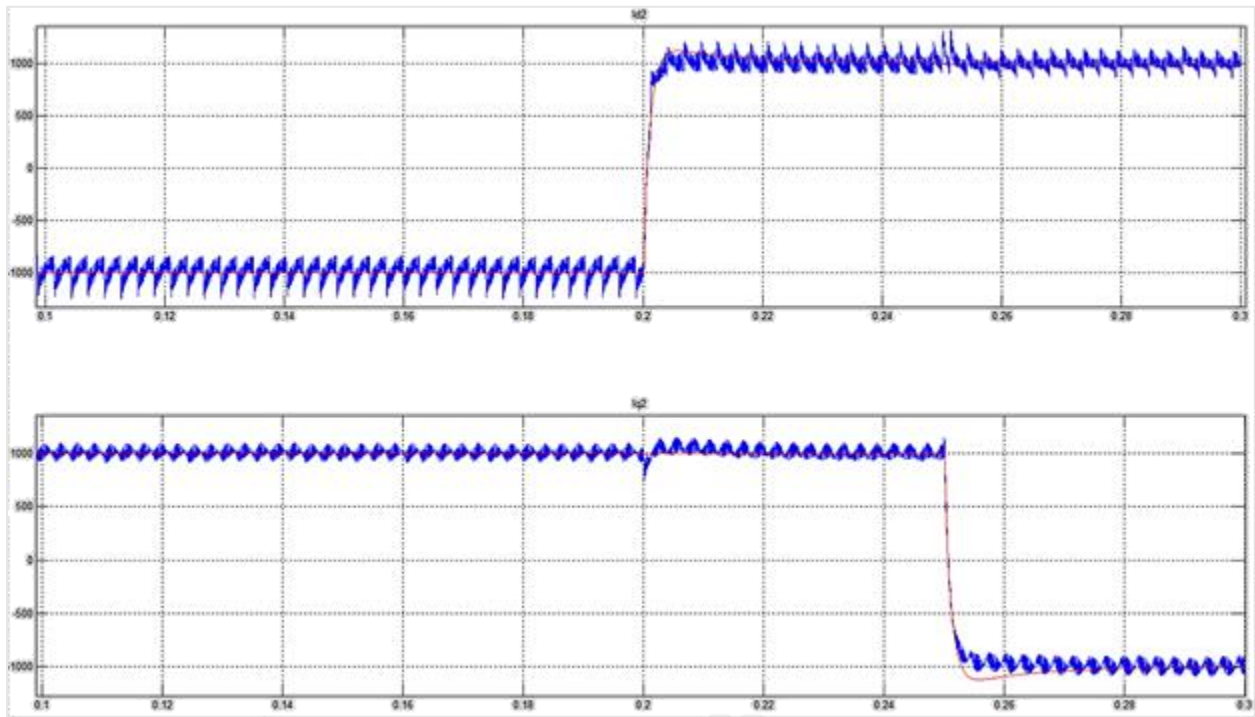


Figure 5. 8. I_{d2} and I_{q2} response to consecutive reference step change for a switched and non-switched system

Switched system shows more coupling between axes, which is a consequence of impact that reference step changes have on a switching ripple component of the waveform. However, fundamental component of I_{d2} and I_{q2} current is affected in the same manner as with non-switched model, which allows a further usage of non-switched model for analysis of proposed decoupling technique.

Even though significantly simpler and less effective than decoupling technique presented in this work, previous investigations have shown that existing decoupling techniques are particularly sensitive to time delays in the control loop [7], [8], [13], [14], [15]. Therefore, Figure 5.9. shows an impact that control loop time delay has on the I_{d2} and I_{q2} values, for $0 < T_d < \frac{1.5}{4140}$

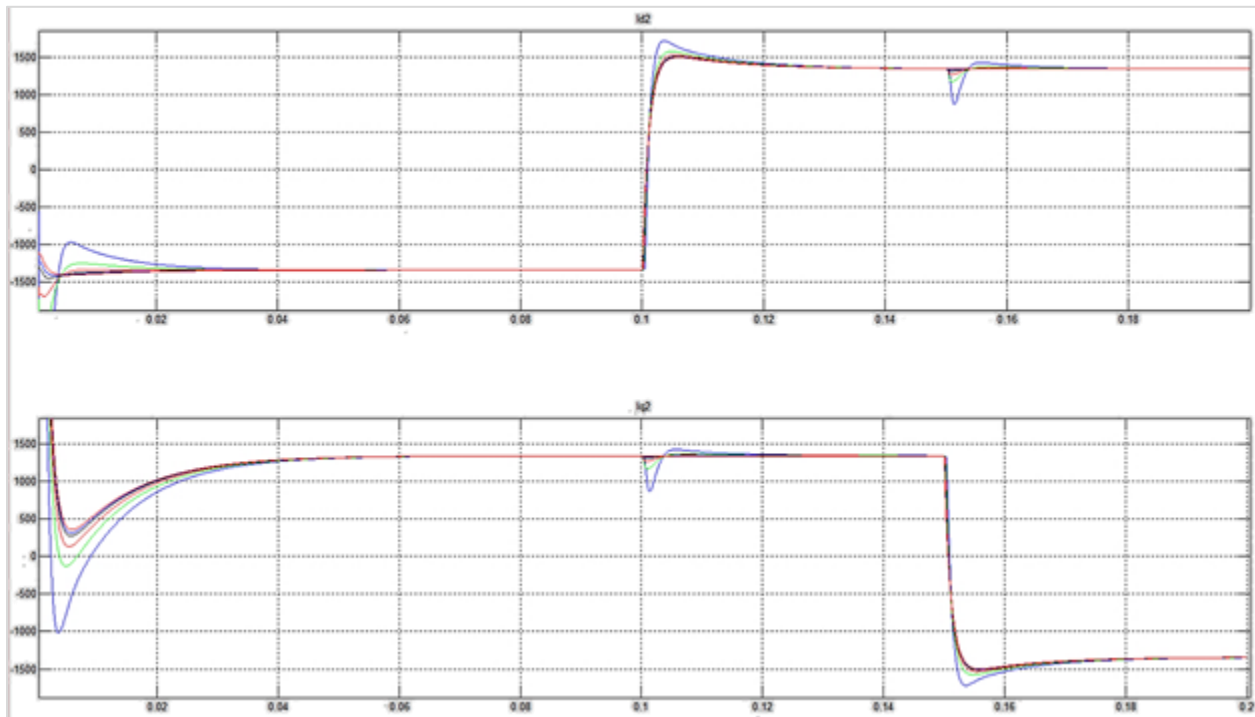


Figure 5. 9. I_{d2} and I_{q2} response to consecutive reference step change for T_d variation

Similar to active damping technique, delay in control loop shows to have a significant impact on the effectiveness of the proposed decoupling technique. Higher values of time delay will basically lead to higher coupling between phases and are therefore undesirable.

Another parameter whose impact on the effectiveness of the decoupling technique needs to be evaluated is the angular frequency ω_c of compensation pole. ω_c represents an angular frequency of a newly introduced pole into the decoupling terms for I_{d2} and I_{q2} . Figure 5.10. shows an impact of ω_c on decoupling for $2\pi * 100 < \omega_c < 2\pi * 2000$.

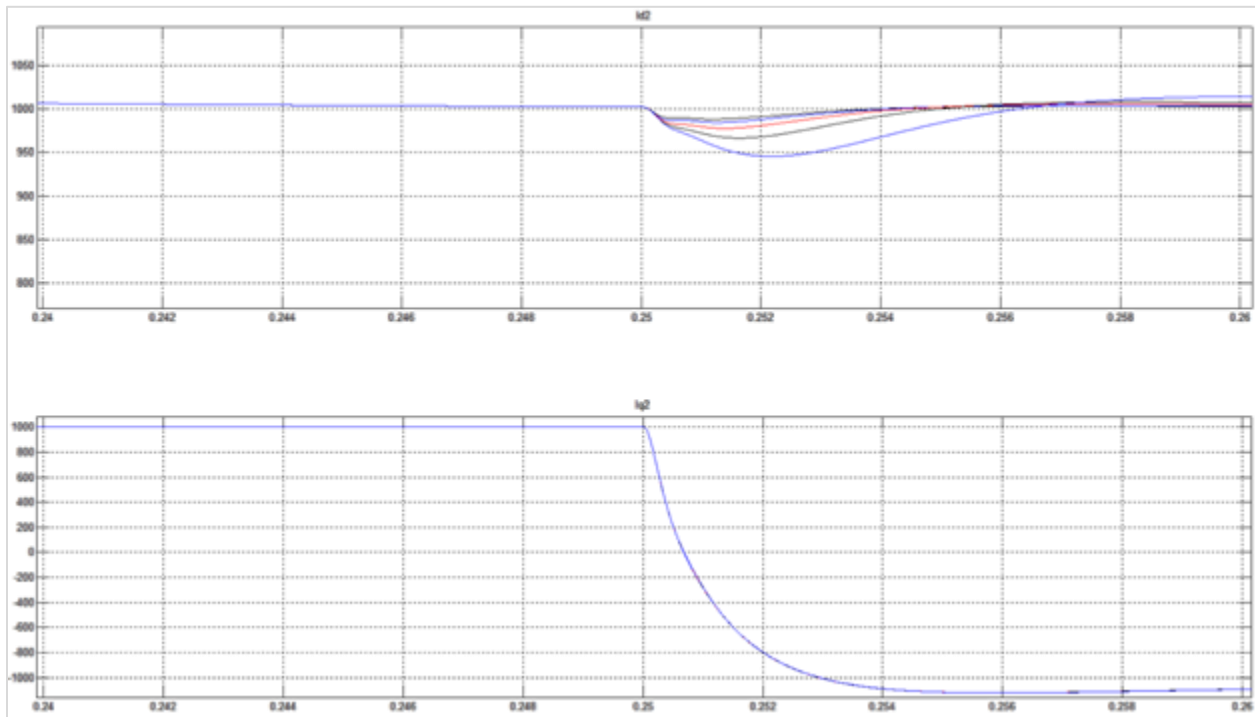


Figure 5. 10. I_{d2} response to I_{q2} reference step change for ω_c variation

Based on results shown in Figure 5. 10., it can be concluded that low angular frequency values ω_c lead to poorer performance of the decoupling technique. Therefore, in order to have an effective implementation of the decoupling, a minimum requirement for ω_c value is to be higher than the closed loop system bandwidth.

It has already been discussed previously in this work, that MTI system needs to be designed with the variation in line impedance value taken in consideration. Consequently, impact of line impedance variation between $0 < L_g < 20\%$ on decoupled system is shown in Figure 5.11.

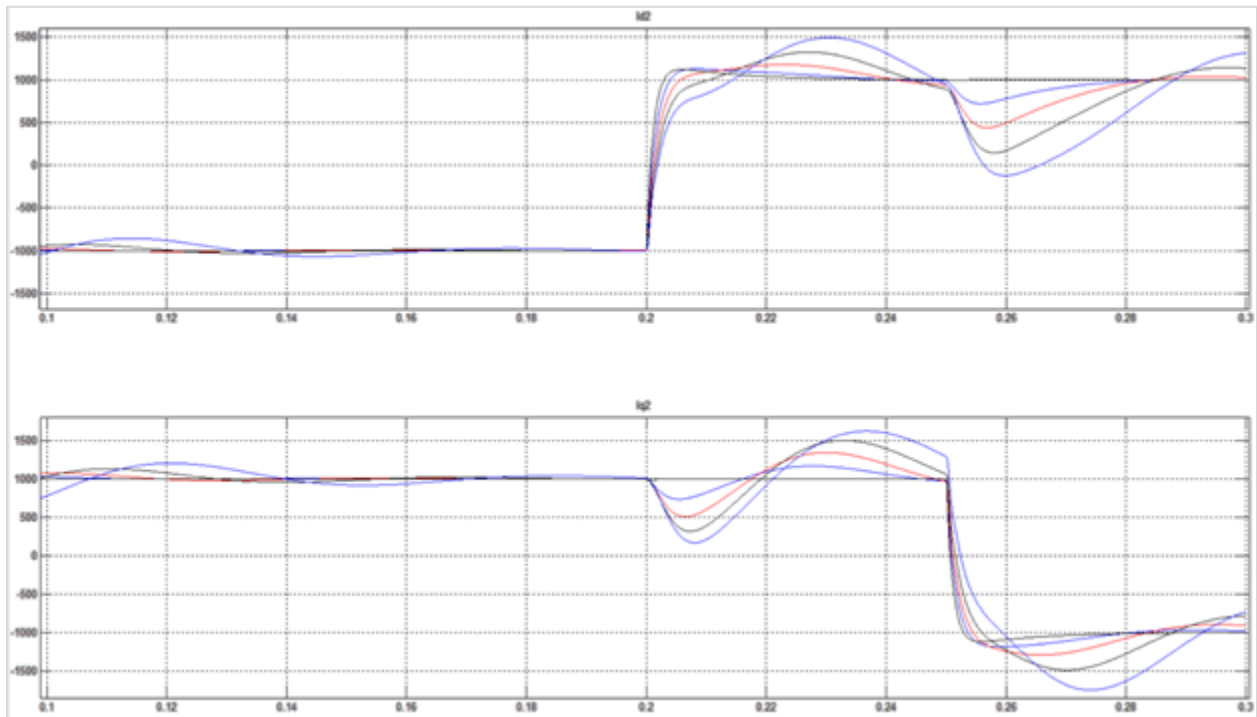


Figure 5. 11. I_{d2} and I_{q2} response to consecutive reference step change for L_g variation

The effectiveness of the proposed decoupling technique is highly impacted by the value of line impedance, where higher impedance values lead to higher coupling values. Line impedance impact is so large that the system performance may be considered unacceptable in cases where high values of line impedance are present. The impact is related to the fact that with additional line impedance causes a change in a voltage at point of common coupling that acts as an additional disturbance that is not compensated. In case where grid voltage feedforward is implemented in addition to decoupling terms, impact of line impedance is shown in Figure 5.12.

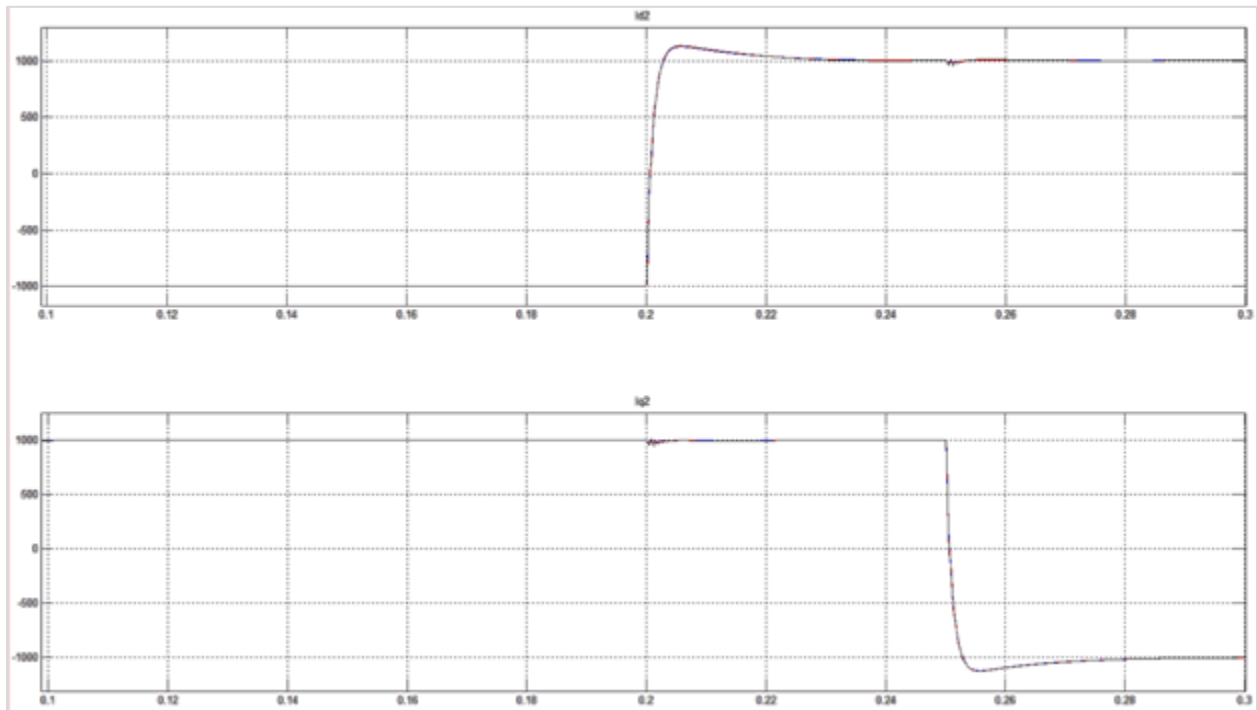


Figure 5. 12. I_{d2} and I_{q2} response to consecutive reference step change for for L_g variation with grid voltage feedforward

Results in figure 5.12. show that with proper implementation of voltage feedforward term, effectiveness of decoupling technique is practically unaffected by the value of line impedance, thus making it highly robust.

5.2. Parasitic Parameter Impact

In MTI system it may be hard to properly estimate the values of parasitic parameters sometimes. For instance, equivalent series resistance of filter inductors should represent all the losses inside the inductor. Those losses are related to winding and core losses, which are a nonlinear function of current magnitude and frequency, as well as the operating temperature. Therefore, equivalent series resistor represents a simple approximation of the losses that occur in the inductor and is not accurate for all operating conditions. Similar conclusion can be derived for equivalent series resistor in the filter capacitor branch. Since R_1 , R_2 and R_c values are used as part of the decoupling technique, it is necessary to evaluate an impact that inaccuracy of these parameters has on decoupling performance. Figure 5.13. and 5.14. show an impact of R_1 and R_2 on decoupling, with actual values being 1, 10, 20, 30, 40 and 50 times what is used in decoupling algorithm.

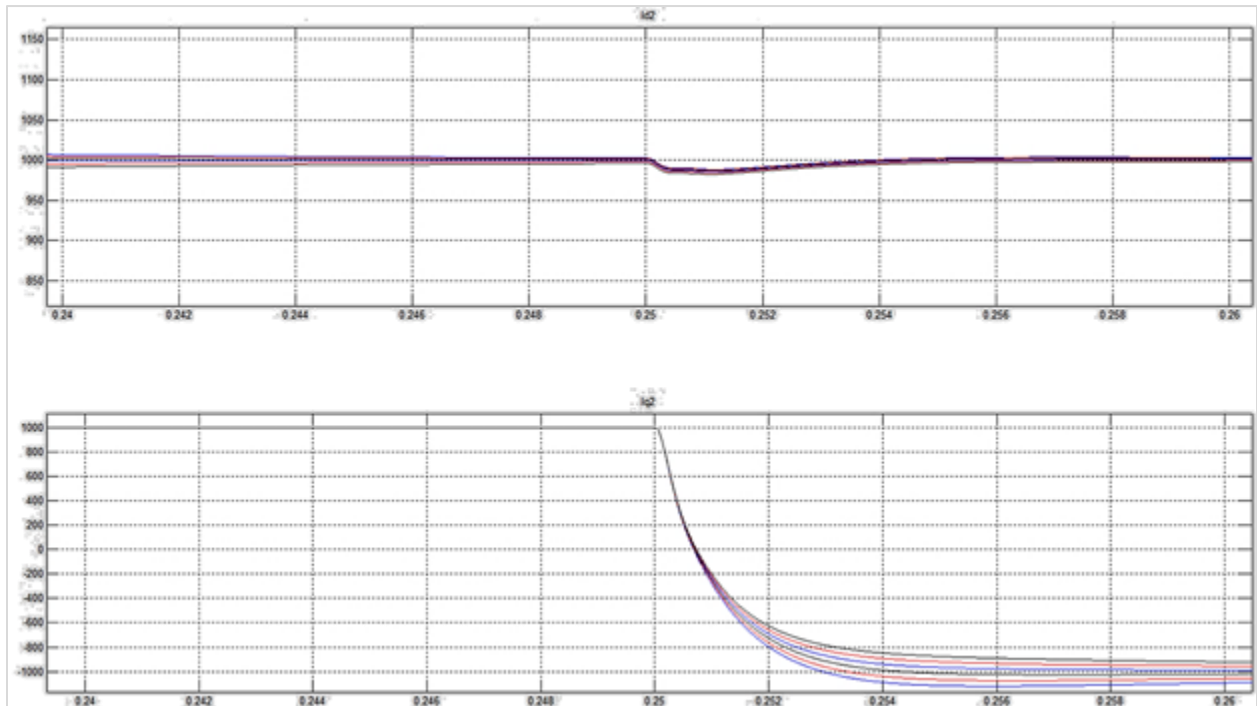


Figure 5. 13. I_{d2} response to I_{q2} reference step change for R_1 variation

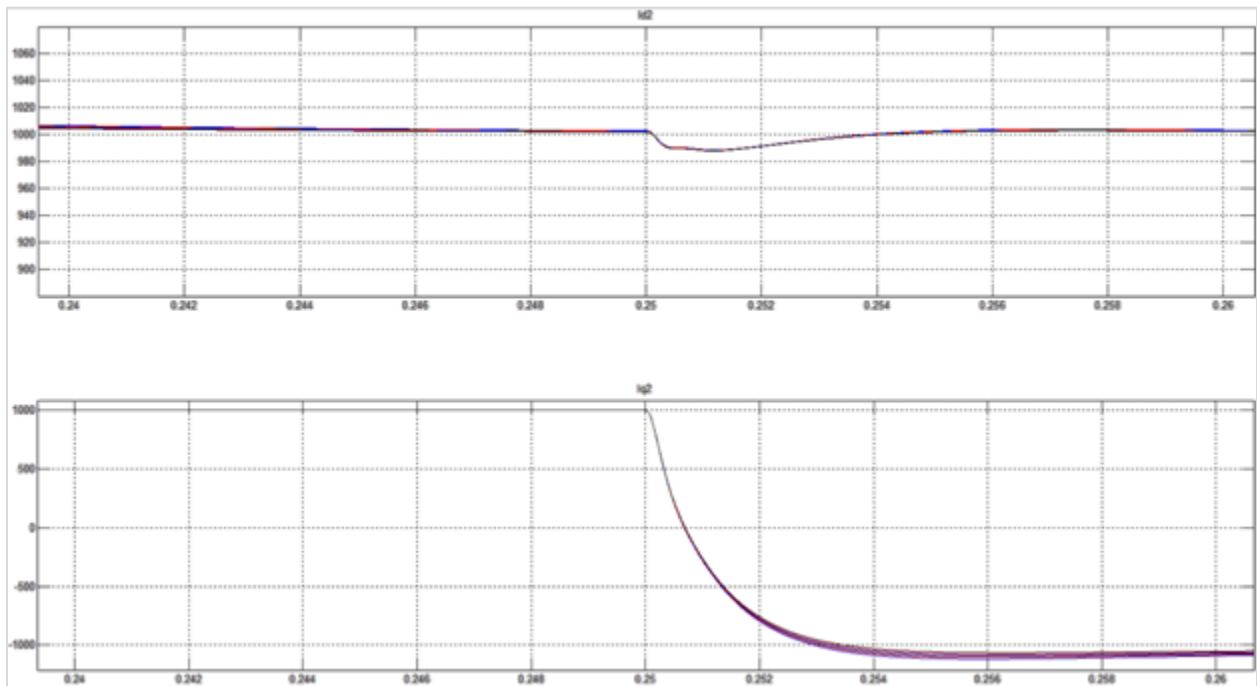


Figure 5. 14. I_{d2} response to I_{q2} reference step change for R_2 variation

Figures 5.13. and 5.14. show that the impact of increased series resistance in the circuit affects the time constant of the circuit, but it has almost no effect on the performance of decoupling algorithm. Figure 5.15. represents a family of actual I_{d2} and I_{q2} waveforms with actual values of filter capacitor ESR being between 50% and 200% of the resistance used in the decoupling algorithm.

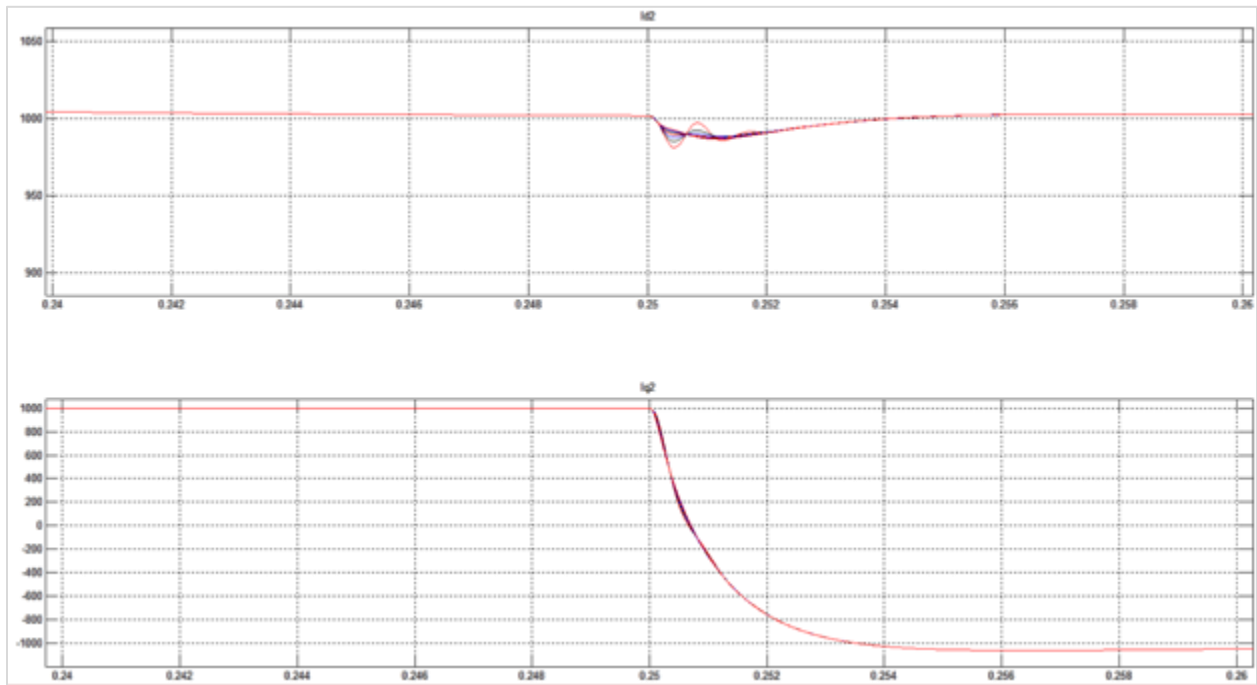


Figure 5. 15. I_{d2} response to I_{q2} reference step change for R_c variation

Low values of R_c in the circuit cause ringing in I_{d2} and I_{q2} due to undamped resonance poles of the closed loop system, which is an expected response of an undamped system, regardless of the decoupling technique used. If resonance oscillations in the response are neglected, mismatch between actual and used R_c value has negligible effect on the performance of the decoupling algorithm. Therefore, it can be concluded that the proposed decoupling algorithm is very robust against the variation of parasitic parameter values in the system.

5.3. Decoupling for Active Damping

So far all the analysis of the new decoupling algorithm has been performed on a passively damped system. However, actively damped system by means of capacitor current feedback requires changes to the decoupling terms derived previously. Therefore, with the neglect of a control loop time delay, a new state space model of an inner control loop for each axis is considered:

$$\frac{d}{dt} \begin{bmatrix} i_{dq1} \\ i_{dq2} \\ V_{dqf} \end{bmatrix} = \begin{bmatrix} \frac{R_1 + R_c + Kr Kpwm}{L_1} & \frac{R_c + Kr Kpwm}{L_1} & -\frac{1}{L_1} \\ \frac{R_c}{L_2} & -\frac{R_2 + R_c}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_f} & -\frac{1}{C_f} & 0 \end{bmatrix} \begin{bmatrix} i_{dq1} \\ i_{dq2} \\ V_{dqf} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} [E_{dqi}]$$

$$+ \begin{bmatrix} 0 & -/+ \omega & 0 & 0 \\ -\frac{1}{L_2} & 0 & -/+ \omega & 0 \\ 0 & 0 & 0 & -/+ \omega \end{bmatrix} \begin{bmatrix} E_{dqcc} \\ i_{qd1} \\ i_{qd2} \\ V_{dqf} \end{bmatrix} \quad (5.33.)$$

By applying the previous derived decoupling terms onto the state space equations for d and q axis, the following decoupling terms are obtained:

$$K_{ffd1} = -\omega L_1 = -K_{ffq1} \quad (5.34.)$$

$$K_{ffd2} = -\omega C \frac{sL_1 + R_1 - R_c + Kr Kpwm}{sC_f R_c + 1} = -K_{ffq2} \quad (5.35.)$$

$$K_{ffd3} = -\omega L_2 \frac{s^2 C_f L_1 + sC_f (R_1 + R_c + Kr Kpwm) + 1}{(sC_f R_c + 1) \left(\frac{s}{\omega_c} + 1 \right)} = -K_{ffq3} \quad (5.36.)$$

$$K_{ffd4} = \frac{s^2 C_f L_1 + sC_f (R_1 + R_c + Kr Kpwm) + 1}{(sC_f R_c + 1) \left(\frac{s}{\omega_c} + 1 \right)} = K_{ffq4} \quad (5.37.)$$

From the equations above it can be concluded that the gain of the capacitor current feedback acts as a virtual resistor added in series with filter capacitor, which only affects the dynamics of the inverter current I_1 , and can be treated as a partial filter capacitor series resistor based damping.

5.4. Feedforward Control of Grid Voltage

There is a large number of studies [16-23] that utilize feedforward control in order to provide better harmonic performance and dynamic response of grid tie inverter systems. In cases where output currents were used [16-18], feedforward technique has shown to be insufficient for suppressing output current harmonics caused by grid voltage distortion. Therefore, the grid voltage feedforward strategy has been accepted as the most effective solution. First paper that introduced grid voltage feedforward strategy was presented in [19] and was applicable to single phase inverters. Single phase solution presented in [19] got extended extend to the three-phase inverters [3], [20]. The major issue with these two proposed solutions is that they contain derivative terms, which are highly impractical for implementation due to noise amplification [21]. In order to address that issue, [22] proposed an improved grid voltage estimator, but the complexity and effectiveness of the solution represent major disadvantages. Also, another option for suppressing grid voltage induced harmonics is to use a simple proportional gain based grid voltage feedforward strategy, which has been presented and utilized since the early beginnings of usage of PWM inverters in grid tie inverter applications [23]. However, this solution will result in inferior performance as compared to the other strategies proposed. Also, all the proposed strategies lack detailed analysis of the impact that various parameters have on the performance of the system.

As already discussed in chapter 4.7, LCL filter has an input impedance characteristic that depends on the selection of filter parameters. It has also been presented that the closed loop system has a different input impedance characteristic that can be further tuned by the proper selection of controller parameters. The addition of grid voltage feedforward component into the control loop further affects the input impedance, and needs to be evaluated.

When closed loop system with proposed grid voltage feedforward is considered, input impedance per each of the d_q axis becomes:

$$Z_{indq}(s) = -\frac{E_g(s)}{i_2(s)} = -\frac{1 + K(s) D_d(s) k_{pwm} R(s) G_i(s)}{G_g(s) - g_{ff}(s) D_d(s) k_{pwm} R(s) G_i(s)} \quad (5.38.)$$

For single loop controlled, passively damped system final input impedance transfer function turns out as:

$$Z_{indq}(s) = \frac{\frac{T_d}{2} A s^5 + \left(\frac{T_d}{2} B + A\right) s^4 + \left(\frac{T_d}{2} C + B + F\right) s^3 + \left(\frac{T_d}{2} D + C + G\right) s^2 + (D + H)s + K_I k_{pwm} \frac{\frac{s}{\omega_c} + 1}{\left(\frac{s}{\omega_c} + 1\right) - D_d(s)}{E_2 \frac{T_d}{2} s^4 + \left(E_2 \frac{T_d}{2} + F_2 \frac{T_d}{2}\right) s^3 + \left(F_2 + \frac{T_d}{2}\right) s^2 + s} \quad (5.39.)$$

A comparison of the frequency characteristic of input impedance of a closed loop system with and without grid voltage feedforward control is shown in Figure 5.16. Parameters used are

$$K_p = \frac{0.1}{K_{pwm}}, K_i = \frac{12}{K_{pwm}}, R_s = 60\%, T_d = \frac{1.5}{20 \cdot 4140}$$

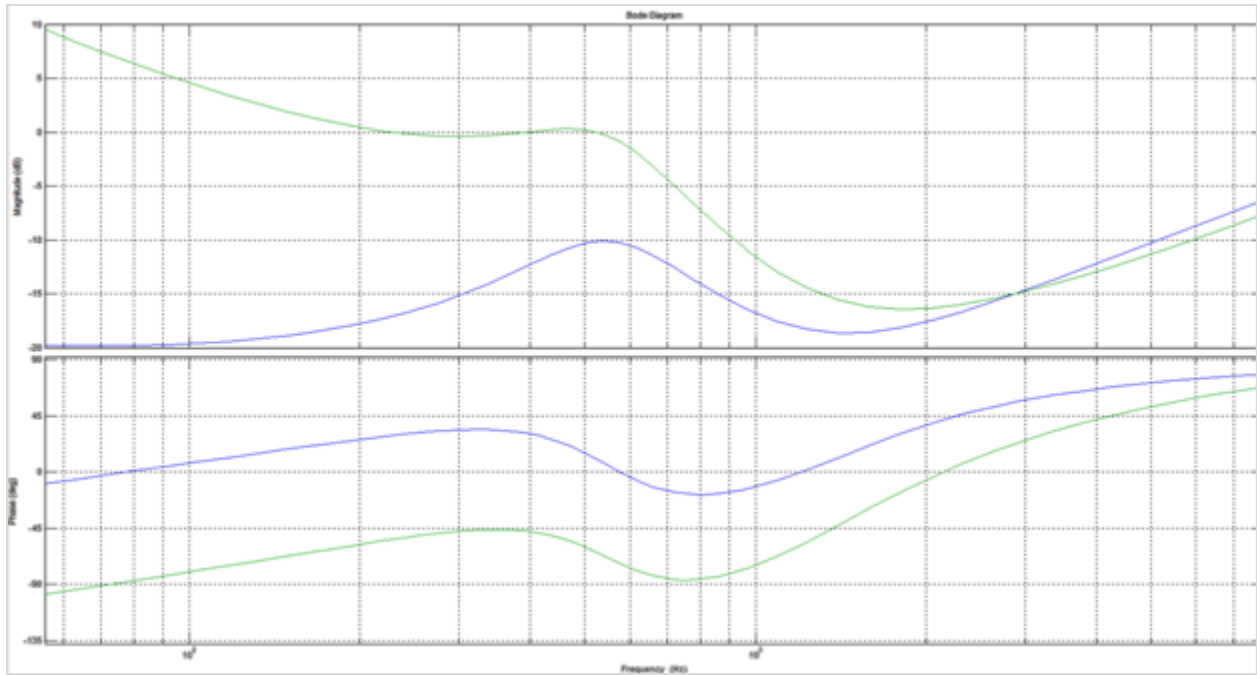


Figure 5. 16. Frequency characteristic of Input impedance Z_{indq} for a closed loop system a) With Feedforward b) Without Feedforward Control

Input impedance of feedforward based system shows higher magnitude values throughout the whole frequency range. That causes closed loop system to become more robust to disturbances present in the grid voltage, as well as to provide better current harmonic performance in presence of grid voltage harmonics. Since feedforward based system shows a drastic difference in terms of input impedance value, it is of interest to investigate the impact of the angular frequency ω_c of a newly introduced pole into the feedforward terms for each axis. Figure 5.17. shows an impact of ω_c on decoupling for $2\pi * 100 < \omega_c < 2\pi * 40000$.

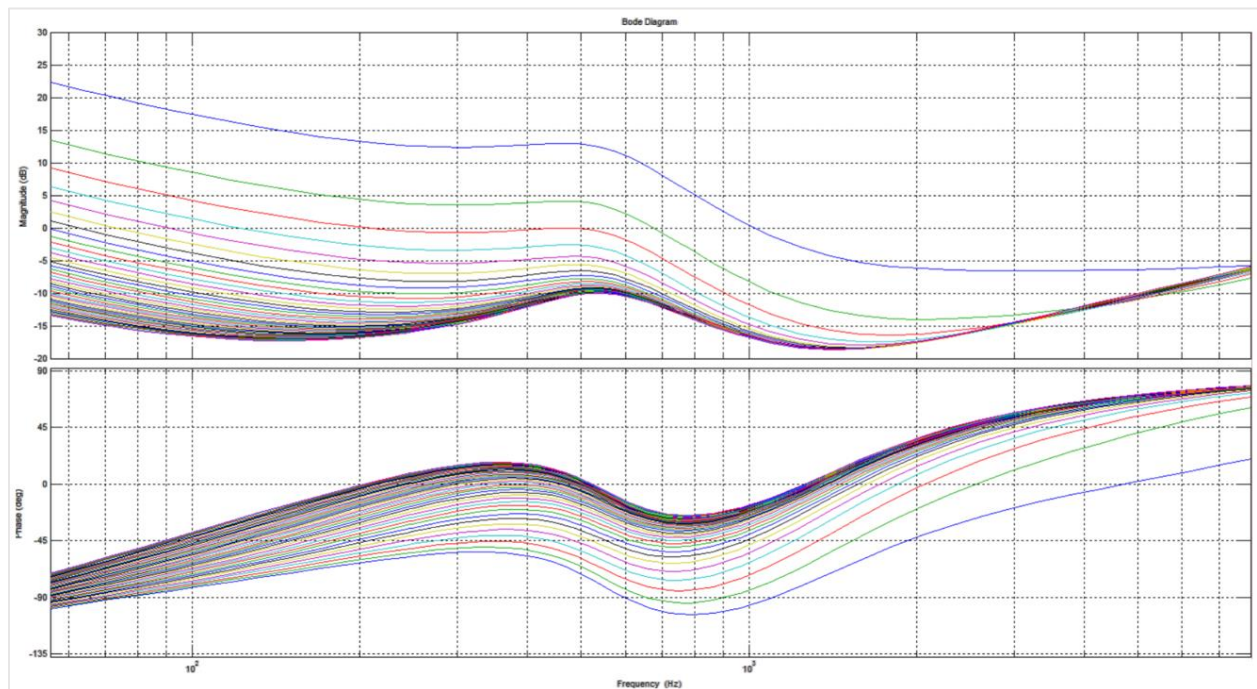


Figure 5. 17. Set of Frequency characteristics of Input impedance for ω_c variation

Based on Figure 5.17., it can be concluded that low angular frequency values ω_c lead to decreased values of input impedance, thus decreasing the effectiveness of the feedforward control. Therefore, a recommendation is to use the highest practical values of ω_c .

Since decoupling technique has shown to be particularly sensitive to control loop delay parameter, it is expected for feedforward control to perform similarly. Therefore, Figure 5.18.

shows an impact that control loop time delay has on the input impedance value, for $\frac{1.5}{4140} < T_d <$

$$\frac{1.5}{20 \times 4140}$$

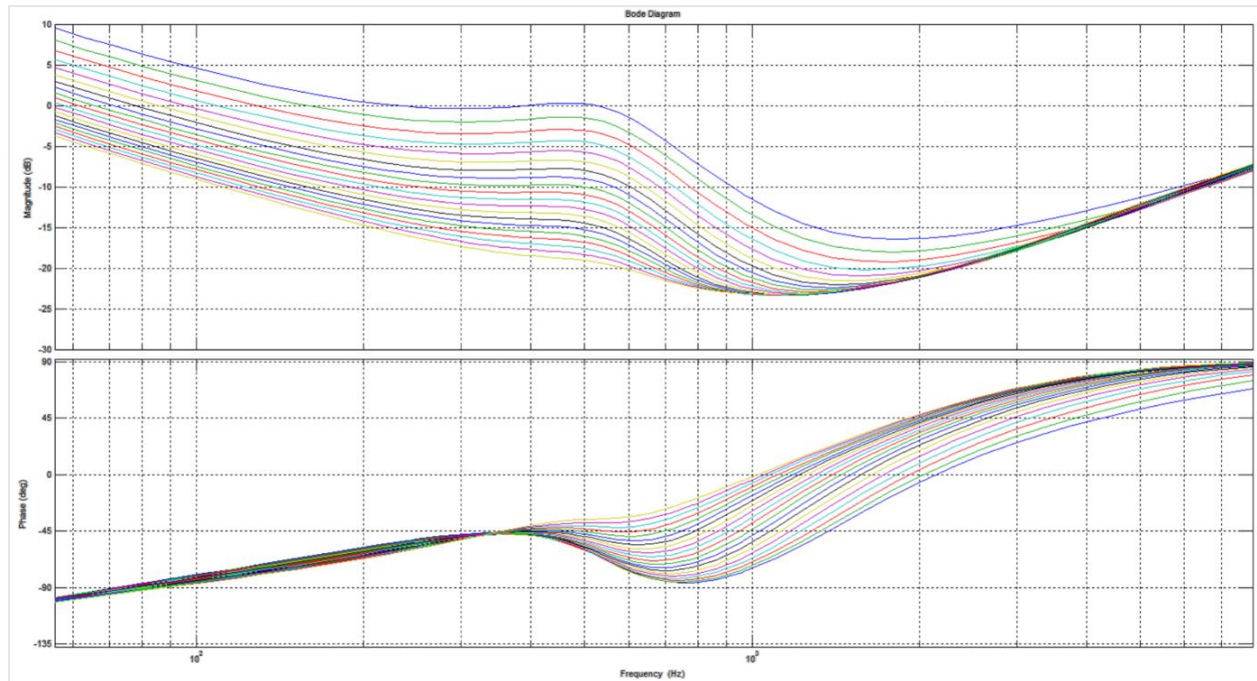


Figure 5. 18. Set of Frequency characteristics of Input impedance for T_d variation

Based on results in Figure 5.18., time delay in control loop has a significant impact on the performance of proposed feedforward control technique, where higher values of time delay decrease the input impedance throughout the frequency range, thus becoming undesirable.

By observing the grid voltage feedforward transfer function, one can notice that line side inductance and/or resistance do not play a role in the function. That is really important from the standpoint of robustness against line impedance variation.

In order to test for input harmonic performance of a MTI system under distorted input voltage condition, system was simulated with added 5th and 13th harmonic at 10% of the fundamental voltage. Figure 5.19. compares 5th and 13th harmonic value of line current I_2 for cases where no solution and proposed feedforward solution were implemented. Current harmonic values

are represented as a percentage of rated fundamental current, and are simulated for cases of 0%, 5%, 10%, 15% and 20% of added line impedance.

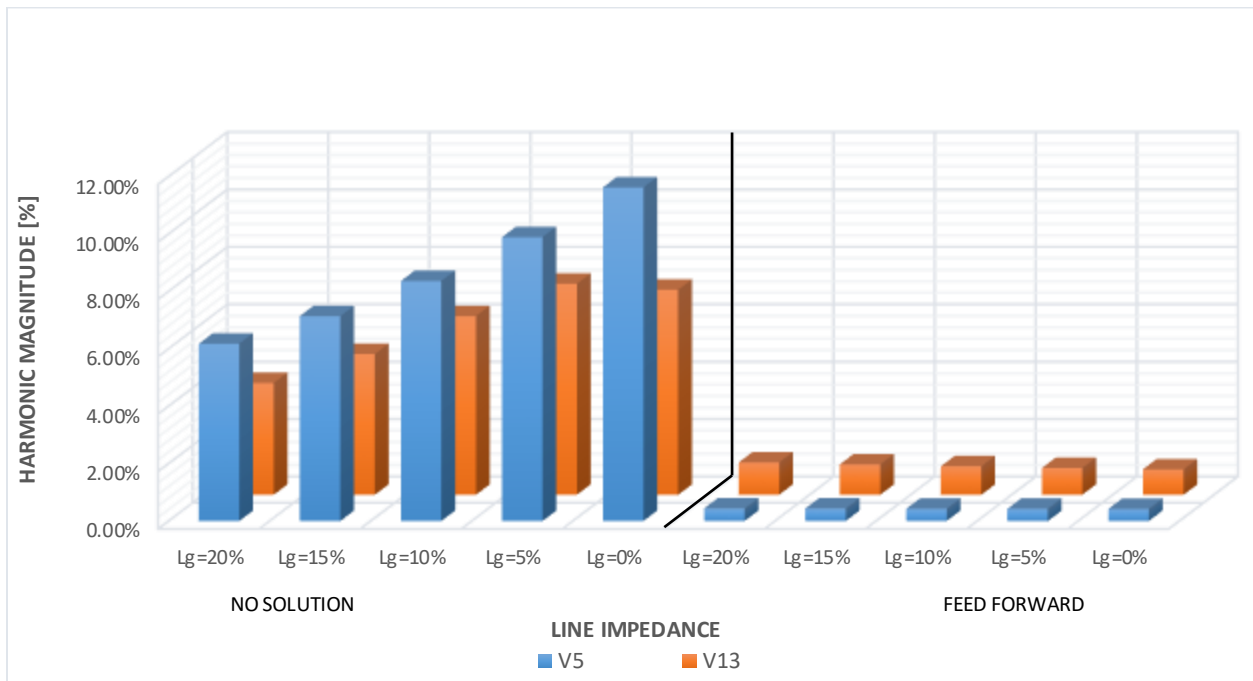


Figure 5. 19. 5th and 13th order current harmonic response comparison between a) Feedforward based algorithm b) No Solution

Feedforward based algorithm shows a drastically improved rejection of grid voltage harmonics. Also, as opposed to no solution case, feed forward based solution provides consistent harmonic performance over a wide range of line impedance values, therefore showing to be robust against line impedance variations.

Except for the harmonic performance, which is considered a steady state performance of the inverter, there is also dynamic performance requirement. Basically, system needs to perform robustly against the dynamic changes in the magnitude of the line voltage. In ideal case, grid side current, which is regulated by the controller, should not get affected by dynamic changes on the line.

Comparison in response to a consecutive step function in grid voltage magnitude, reflected thru V_d component, between no solution and proposed feedforward solution are shown in figure 5.20. for an ideal non-switched model of a system. Positive and negative grid voltage step functions at 10% rate were applied at different time instances in each axis and the output current I_{d2} and I_{q2} responses were observed.

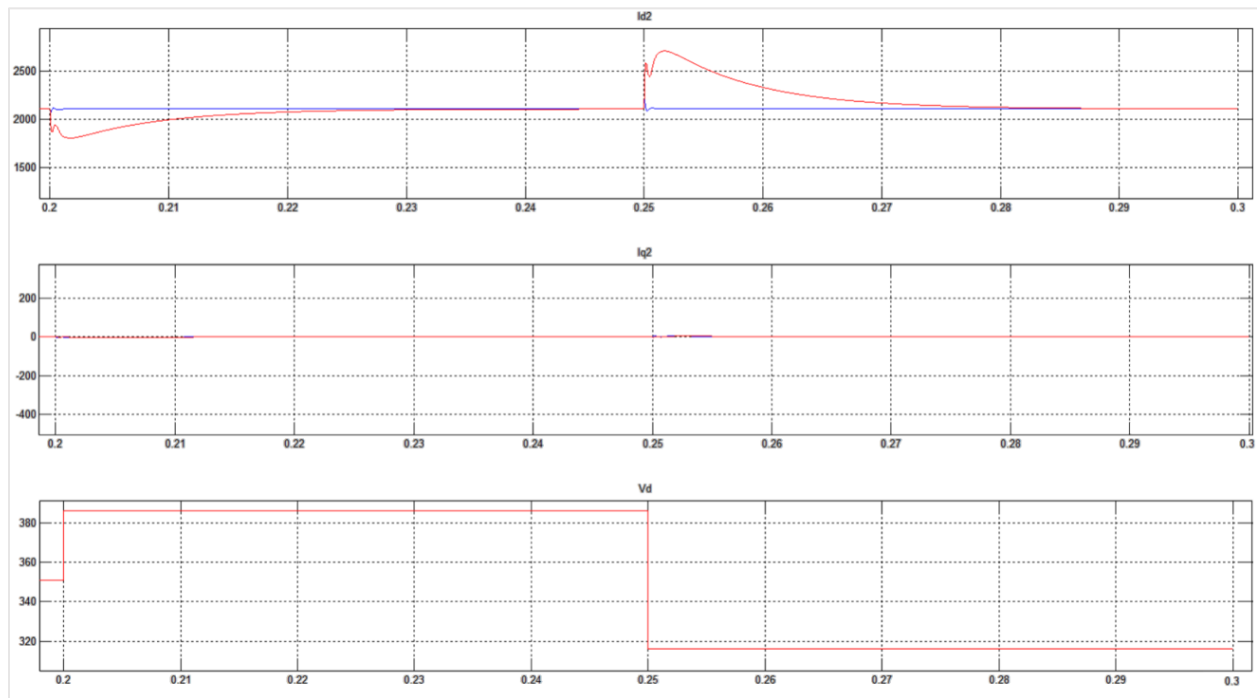


Figure 5. 20. I_{d2} and I_{q2} response to consecutive grid voltage step change for no solution and feedforward based decoupling solution

As opposed to no solution, which gets highly impacted by the voltage disturbance, newly proposed feedforward solution practically shows no impact of a grid voltage step change on a regulated output current. Also it is useful to evaluate the actual response of a switched system, which is shown in Figure 5.21. for the same case as Figure 5.20. Figure 5.21. compares an output current response to a step change in grid voltage for a switched and a non-switched system. Switched system is implemented with all the nonlinearities and physical limitations that non-switched system does not include.

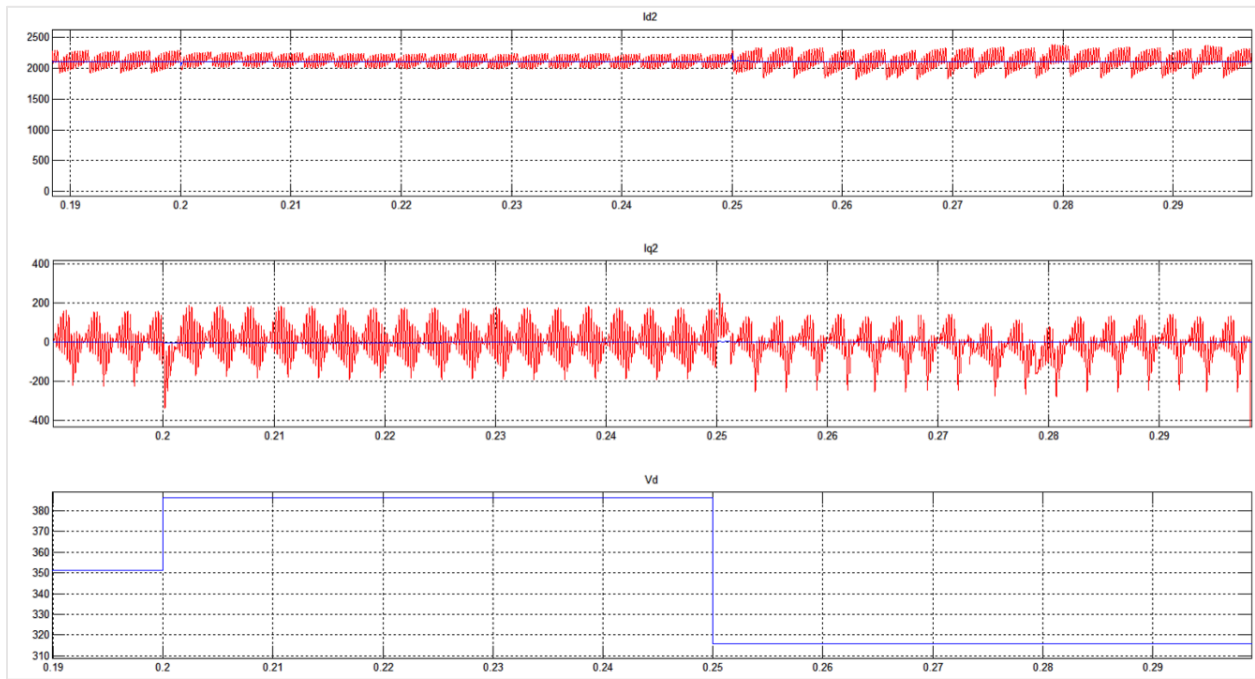


Figure 5. 21. I_{d2} and I_{q2} response to consecutive grid voltage step change for a switched and non-switched system

Switched system shows to be more sensitive to step changes in the grid voltage, but the fundamental component of I_{d2} and I_{q2} current is affected almost equally as with non-switched model. The major difference is in the ripple current, which gets affected as a consequence of a modulation index change of the inverter, therefore having nothing to do with the proposed feedforward technique.

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6. Experimental Setup

6.1. General Setup Description

This section describes the experimental setup built for performance verification of proposed MTI system. The setup consists of two inverters connected thru common DC bus connection, in a so called “back to back” configuration. One inverter acts as load for MTI by operating as motor drive connected to a test dyne system. Another inverter operates as MTI connected to utility grid by means of LCL filter. MTI is responsible for DC bus voltage regulation, so active power is indirectly controlled via motor drive loading. On the other hand, MTI has autonomous control of reactive power on grid side. The overall block diagram of an experimental setup is shown in figure 6.1.

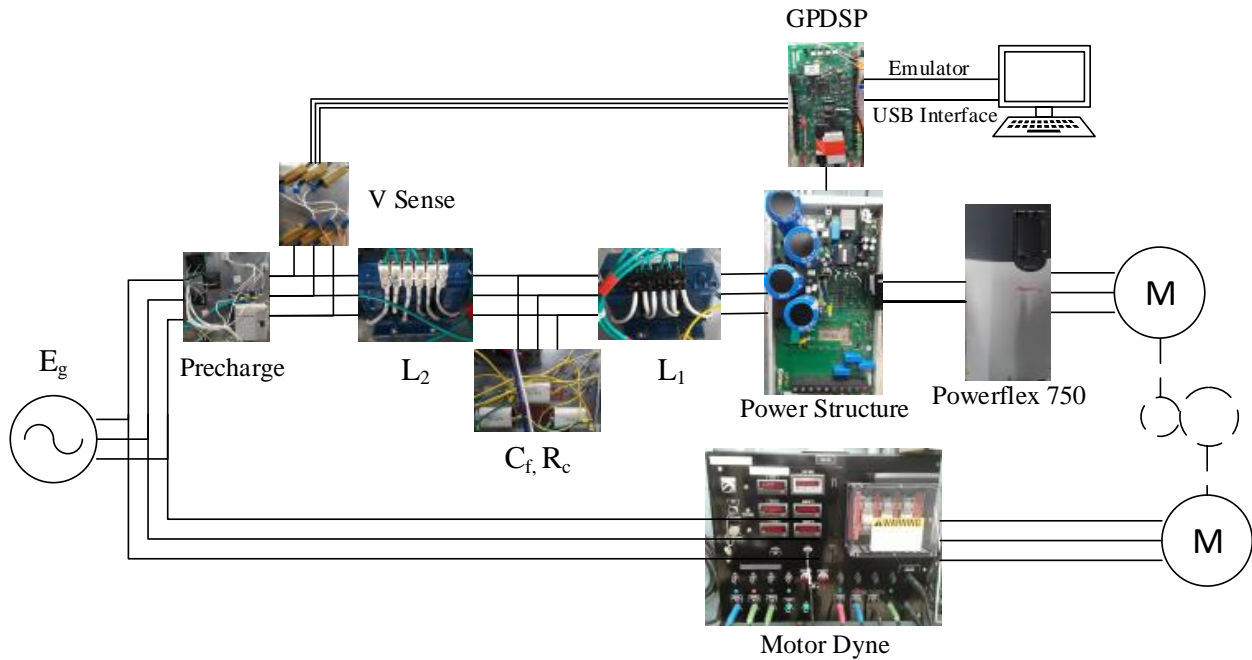


Figure 6. 1. Block diagram of MTI setup

The source is connected to inverter power structure via LCL filter. The picture of the actual setup is shown in figure 6.2.

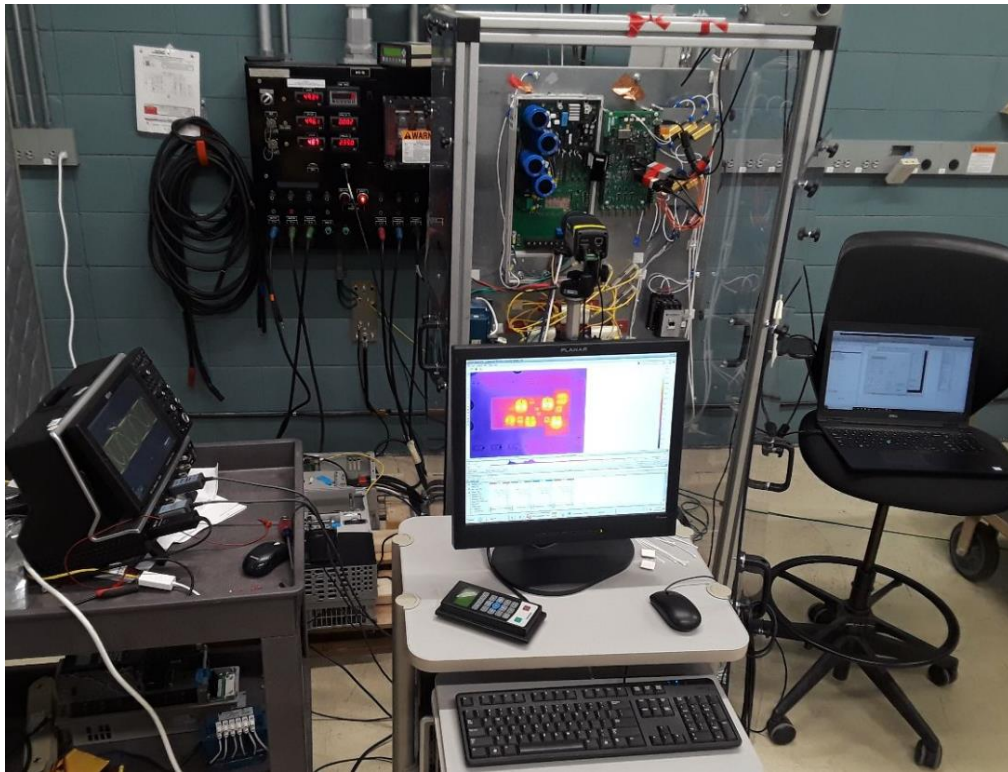


Figure 6. 2. Actual MTI test setup

Each Inverter uses Rockwell Automation Powerflex 750 Frame 4 drive power structure.

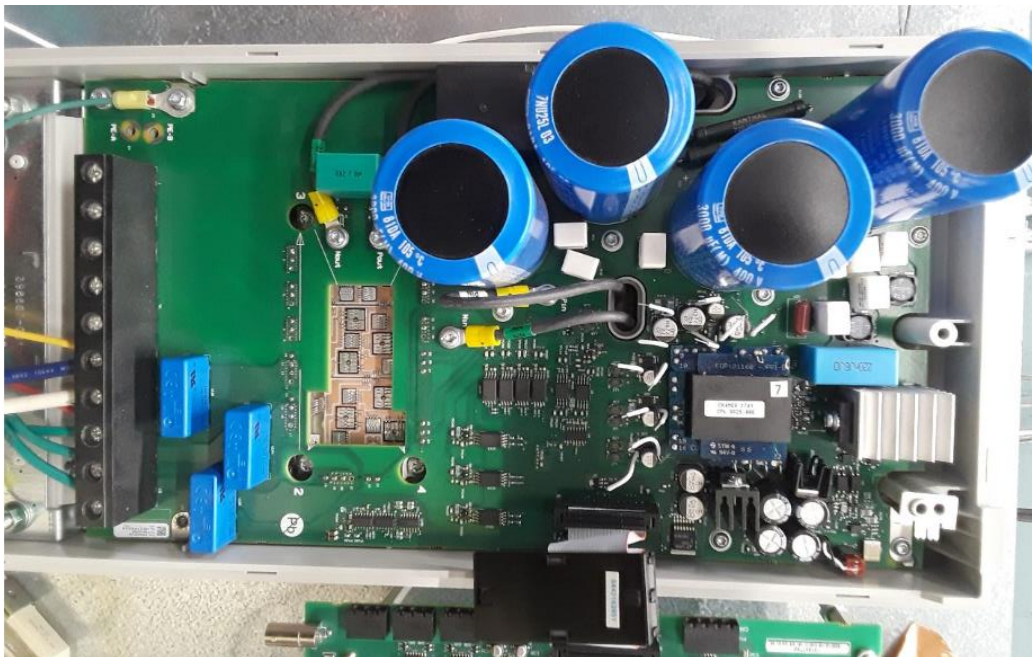


Figure 6. 3. Powerflex 750 Frame 4 power structure

Power Flex 750 Frame 4 power structure is shown in Figure 6.3 and mainly consists of power module (3 phase IGBT/Diode H bridge), gate drive circuits, current sensors, voltage, current and power module sensing circuits, along with heat sink and fan. The control is based on GPDSP (General Purpose Digital Signal Process) board, which utilizes the Texas Instrument Fixed Point DSP TMS320F2812, as shown in Figure 6.4.

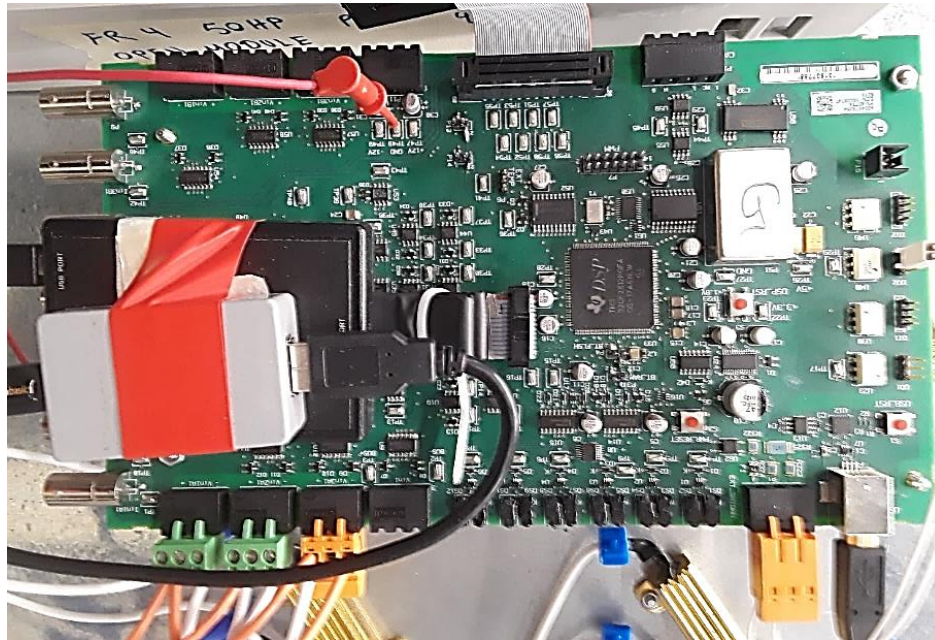


Figure 6. 4. GPDSP board with DSP TMS320F2812

Board consists of 3 current sensing, 3 voltage sensing , DC bus voltage sensing and power module temperature sensing circuits along with 6 PWM output channels.

Additional built-in features such as DC bus over voltage and instantaneous over current protection are present.

GPDSP is connected to power structure via 50 pin interfacing connector, from which it sources low voltage power necessary for operation. In order to compile code from host PC, Spectrum Digital XDS510USB emulator with optical isolator is used.

Texas Instrument Code Composer Studio is used to communicate and program the GPDSP board. GPDSP board control is realized in Matlab Simulink environment, which is a model based programming environment that requires usage of Real time embedded coder, Simulink Coder, DSP toolbox, Fixed point toolbox and Simpower system toolbox for control implementation. Therefore, Matlab real time embedded coder interfaces with Code Composer Studio to convert the Simulink program into the C code. Also, an opto-isolated USB interface is used to provide a communication interface between the control firmware and a host computer through a USB port.

USB interface allows for real time control and monitoring of various variables and status signals of interest via communication interface created in Matlab as shown in Figure 6.5

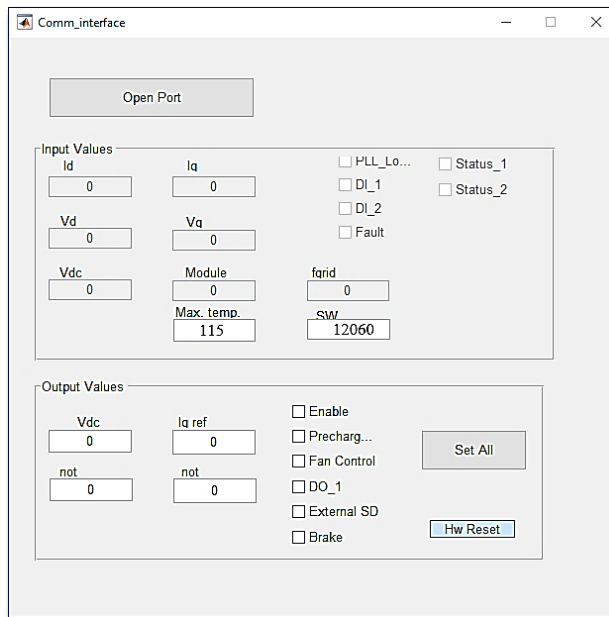


Figure 6. 5. Matlab based communication interface

Critical instantaneous overcurrent and ground fault detection are implemented as hardware based circuits in charge of disabling PWM signals in case of faulty condition. Grid side three phase voltage feedback, inverter side three phase current feedback, power module temperature and DC bus voltage feedback signals are sensed for control and monitoring purposes. Three phase grid line to line voltages are stepped down using an external voltage resistor divider network to 120V rms. Currents are sensed by Hall effect sensor and scaled to range from -5V to 5V as part of power

structure. Dc bus voltage is stepped down using a voltage resistor divider network to 0-5V range as part of power structure. Temperature sensing is realized using thermistor internal to power module and scaled to 0-5V range. All sensing signals are fed as analog inputs to GPDSP board, where they are further conditioned to 0-3V ADC range.

6.2. Inverter Setup Parameters

The inverter is designed for following parameters:

V_b [V]	S_b [KVA]	f_{sw} [Hz]	I_b [A]
480	39	12060	52.12

Table 6. 1. Parameters of 39 KVA rated microgrid tie inverter

A maximum peak to peak current ripple on the inverter side inductor L_1 is calculated as 14% of the rated current per (3.7.):

$$\Delta I_{L_{max}} = 9.5 A$$

Inverter side inductance L_1 is calculated based on (3.4.) as:

L_1 [mH]	L_1 [%]
1.2	8.5

Table 6. 2. Inductance L_1 calculation

Therefore, the resulting ripple attenuation and grid side ripple current is calculated per (3.9.).

Ripple Attenuation	I_{ripple} [A]	I_{ripple} [%]
0.038	0.3	0.43

Table 6. 3. Ripple attenuation and grid side ripple current calculation

Capacitance C_f is selected as:

C [μF]	C [%]
12	2.4

Table 6. 4. Capacitance C_f calculation

However, capacitance in actual circuit is delta connected with $4\mu F$ of capacitance between two lines.

Grid side inductance L_2 is selected as:

$L_2[mH]$	$L_2[\%]$
0.4	2.8

Table 6. 5. Inductance L_2 calculation

Finally, the resonant frequency is calculated by (3.11.) as:

$$f_{res} [Hz] = 2,670$$

Also, additional series damping resistor needed to be introduced into the circuit at value of 1Ω in series with delta connected capacitors representing 6.2% of base impedance.

As discussed previously, control is implemented in Matlab Simulink, and includes of ADC signals for voltage, current and temperature sensing, Phase locked loop (PLL) for synchronization, current and voltage regulators and PWM modulator. The input voltage range to ADC converter is 0-3V, where signals are fed to the inbuilt 12 bit ADC of the DSP. The voltage sense circuit scaling and calibration is required in order to avoid DC offset asymmetries in measurements. Therefore, signals are compensated for offsets and converted to fixed data type (1, 32, 26) format as shown in figure 6.6.

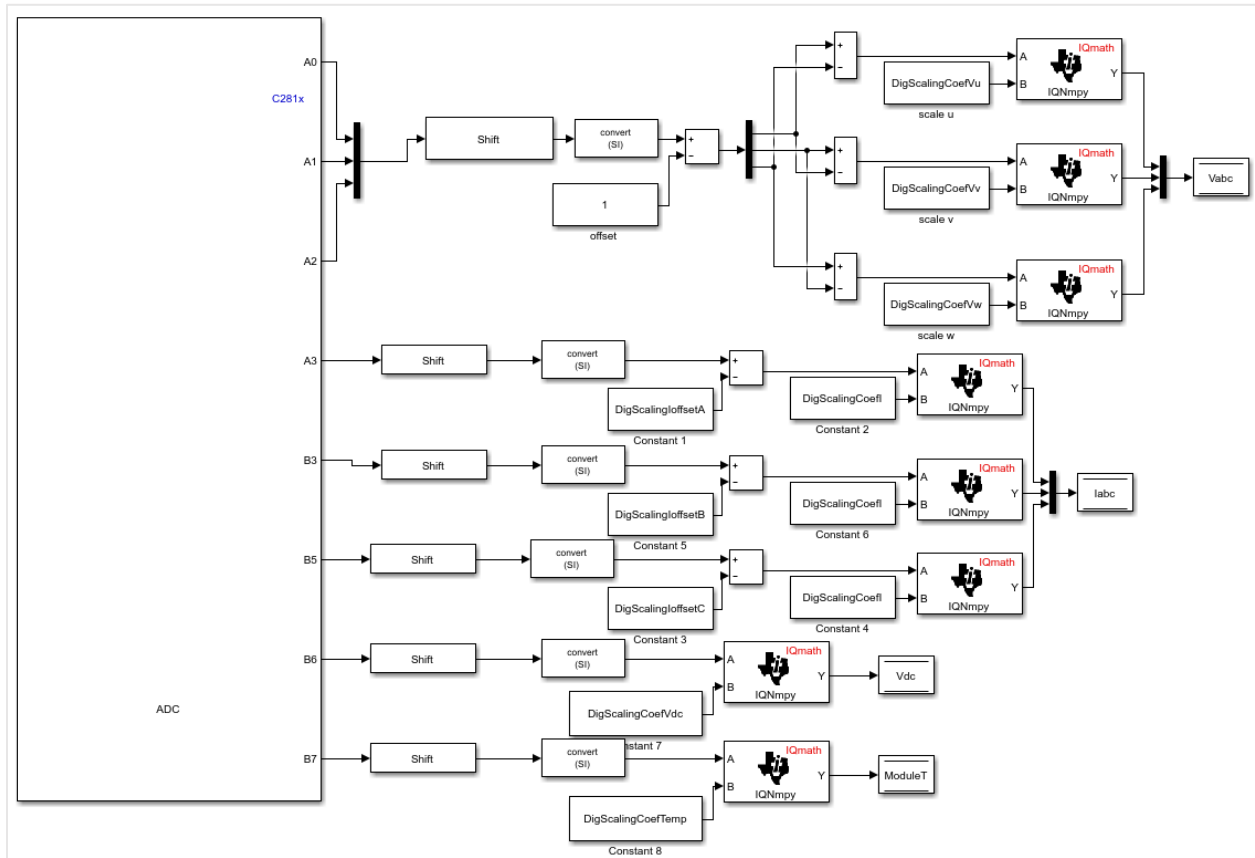


Figure 6. 6. ADC, conversion of input ADC signals

The PLL implementation in synchronous reference frame is shown in figure 6.7.

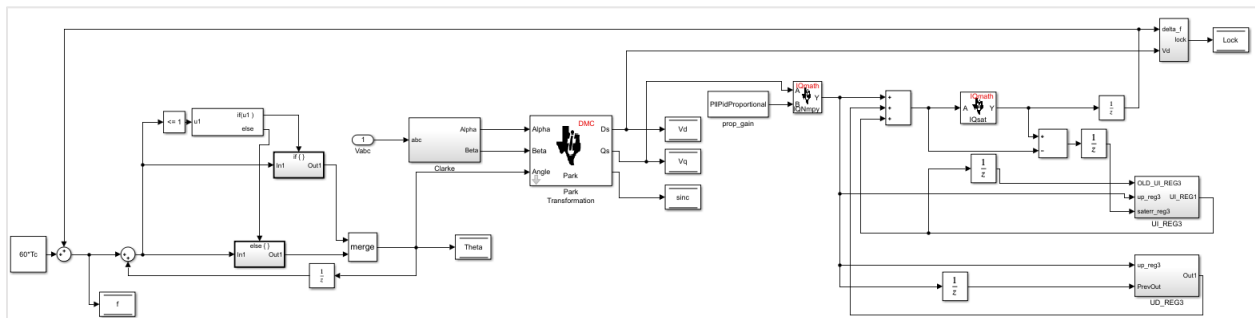


Figure 6. 7. PLL implementation

Three phase voltages and currents are converted to rotational dq reference frame values using three phase to two phase stationary (Clark) transformation and stationary to rotational (Park) transformation.

The DC voltage and current control loop implementation using discrete PI regulators is shown figure 6.8.

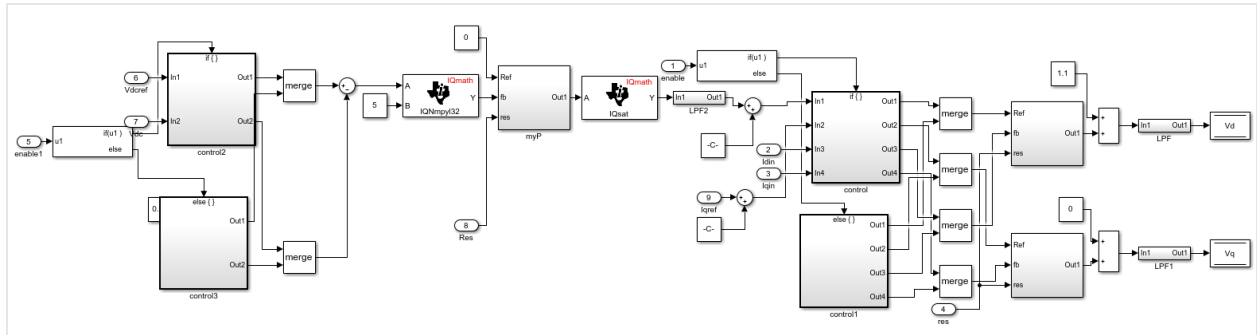


Figure 6. 8. DC Voltage and Current regulator

DC voltage control loop is used to create reference for active current component I_d in current control loop. Reactive current component I_q is controlled via external reference set by user. Current control loop includes decoupling and feed forward terms. Outputs of PI regulators create rotational reference frame voltage references V_d and V_q , which are transformed back to stationary reference frame and fed to DDPWM modulator block. DDPWM modulator block is shown in Figure 6.9.

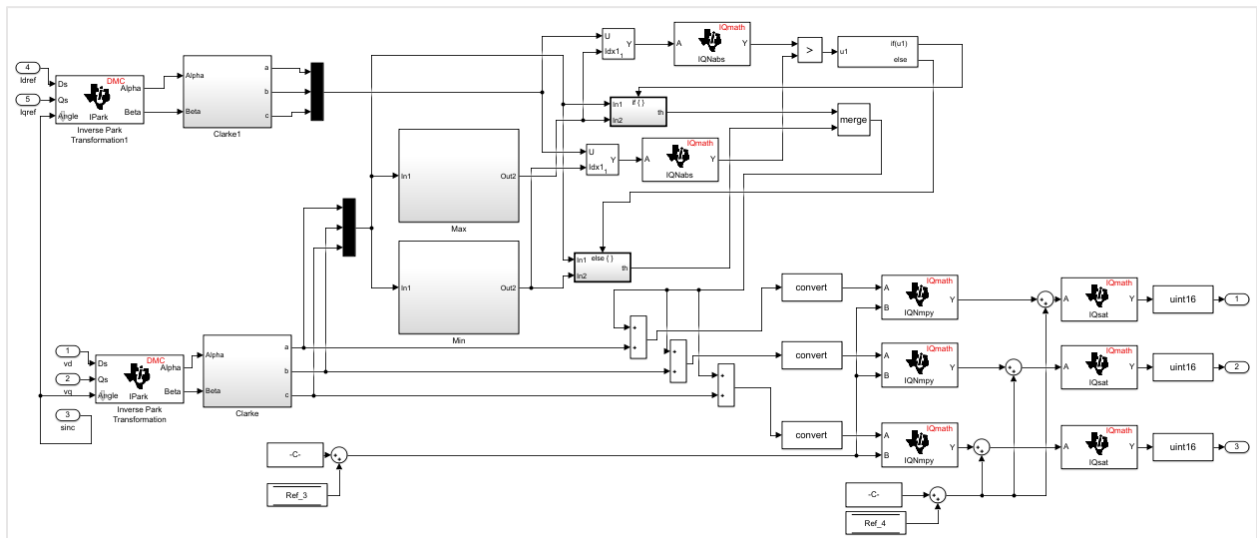


Figure 6. 9. DDPWM Modulator

DDPWM creates stationary voltage references which are scaled and fed as a duty cycle input to PWM block. PWM block generates 6 pulses to drive the gates of the 6 IGBTs. PWM

switching frequency is set to 12.06 kHz with variable dead time setting. Due to limitations of TMS320F2812 DSP, synchronized sampling of ADC for multisampling or peak and valley sampling was not possible. Therefore, ADC sampling has been synchronized with PWM at valley only (counter underflow), and overall sampling and control has been implemented at PWM frequency of 12.06 kHz.

6.3. Thermal Performance Testing

In order to evaluate thermal performance of DDPWM algorithm, thermal test on power module is performed as per setup shown in Figure 6.2. For accurate measurement of transistor (IGBT) and freewheeling diode junction temperatures under various operating conditions, thermal evaluation procedure called “open module” testing is adopted. Open module testing procedure consists of direct measurement of junction temperatures inside power module using infrared camera. Since standard power modules are potted and encapsulated, a custom module with thin layer of potting material and no encapsulation needs is prepared. Also, printed circuit board in which power module is pressed or soldered is custom designed in order to provide a cutout window for thermal imaging using infrared camera. Detailed picture of the open module test unit and FLIR 655 camera is shown in figure 6.10

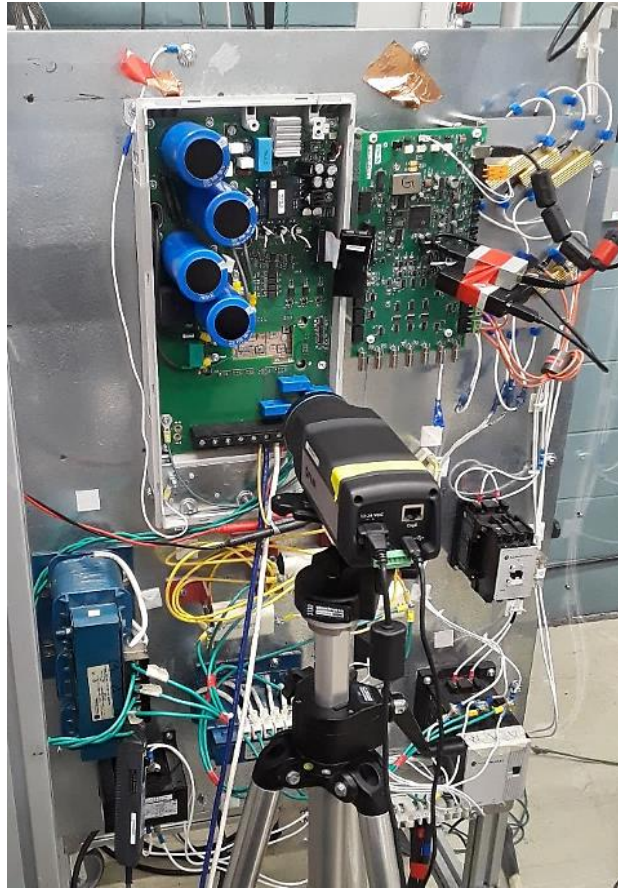


Figure 6. 10. Thermalopen module test setup

Electrical and thermal impedance parameters of power module used for thermal evaluation are the following:

I_r [A]	V_{ft} [V]	R_{ft} [Ω]	$E_{on} + E_{off}$ [mJ]	V_{fd} [V]	R_{fd} [Ω]	E_{rr} [mJ]
100	0.875	0.011875	15.55	0.90	0.0065	3.80

Table 6. 6. Power Module - Electrical Parameters

R_{jci} [K/W]	R_{csi} [K/W]	R_{jcd} [K/W]	R_{csd} [K/W]	R_{csm} [K/W]	R_{sa} [K/W]
0.29	0.13	0.5	0.225	0.041	0.072

Table 6. 7. Power Module - Thermal Impedance Parameters

Infrared camera is connected to host computer which contains real time thermal measurement software used for surface temperature evaluation and analysis. Total of four measurement boxes are set in software to cover the area of top and bottom transistor and diode

dies in each inverter leg, as per DDPWM example at $\theta = 90^\circ$ and $V_{dc} = 750V$ shown in Figure 6.11

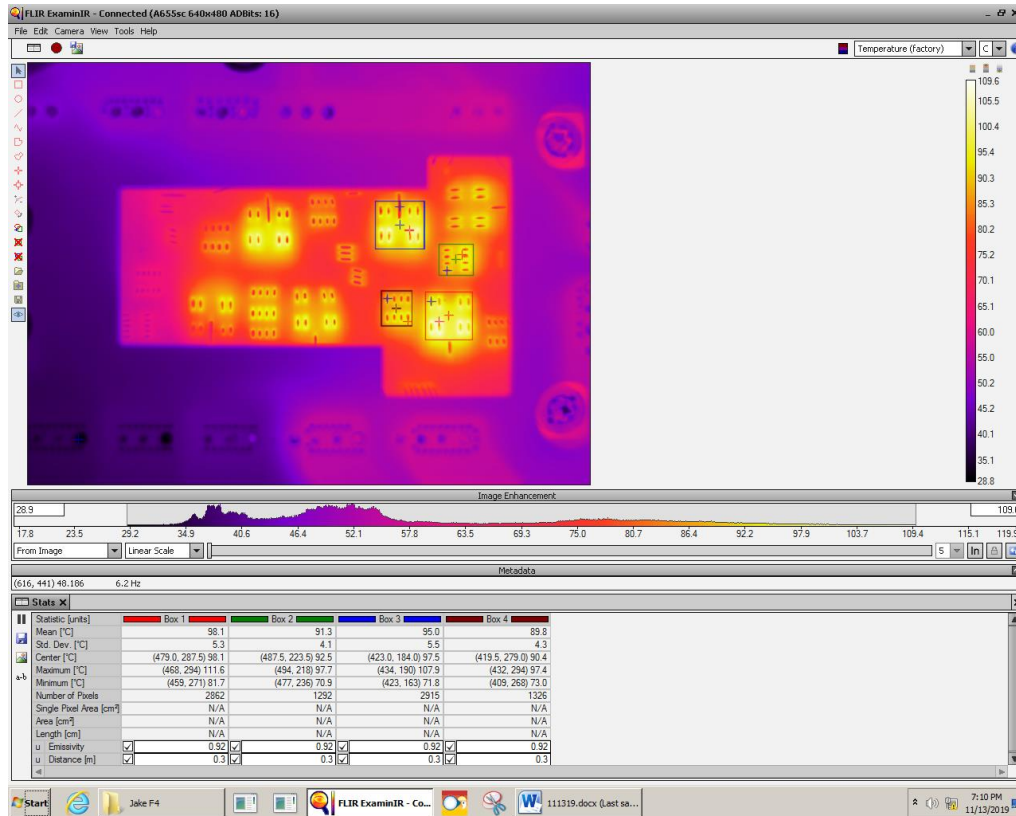


Figure 6. 11. Measurement Box Settings for each inverter leg

Each measurement box provides various thermal information of interest such as maximum/minimum and mean temperature values inside the box. Thermal testing was performed at rated conditions listed above at varying load angle $-180^\circ < \theta < 0^\circ$ to compare thermal performance of DDPWM and SVPWM modulation. Also, DDPWM was tested at two different dc bus voltage setpoints $V_{dc} = 700V$ and $V_{dc} = 750V$ to reflect the incremental contribution of elevated dc bus voltage on switching losses. Selected test results for DDPWM and SVPWM at $\theta = 0^\circ$, $\theta = -180^\circ$ and $V_{dc} = 700V$ are shown in Figures 6.12.-6.16. respectively.

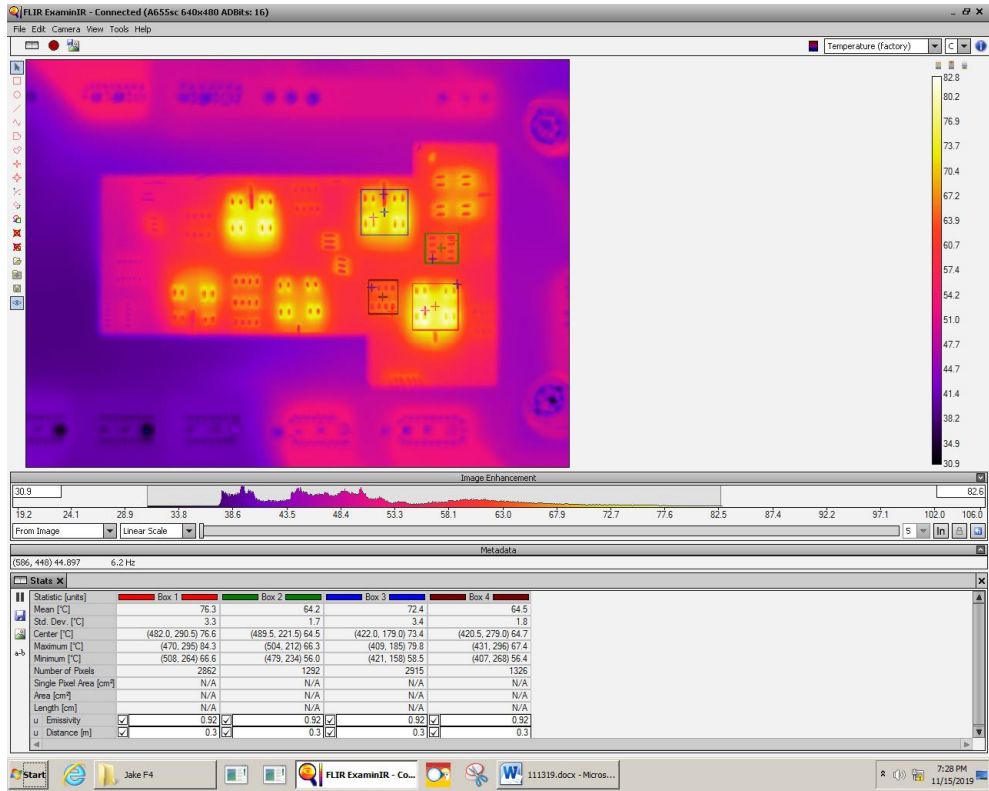


Figure 6. 12. DDPWM at $\theta = 0^\circ$ and $V_{dc} = 700V$

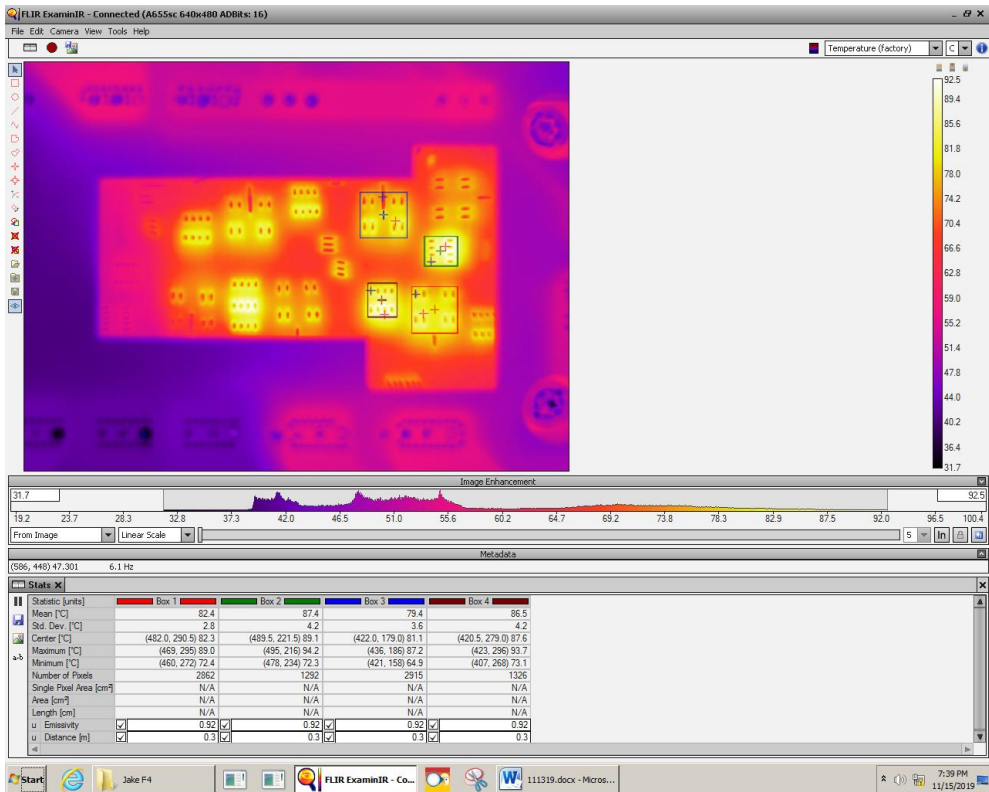


Figure 6. 13. DDPWM at $\theta = -180^\circ$ and $V_{dc} = 700V$

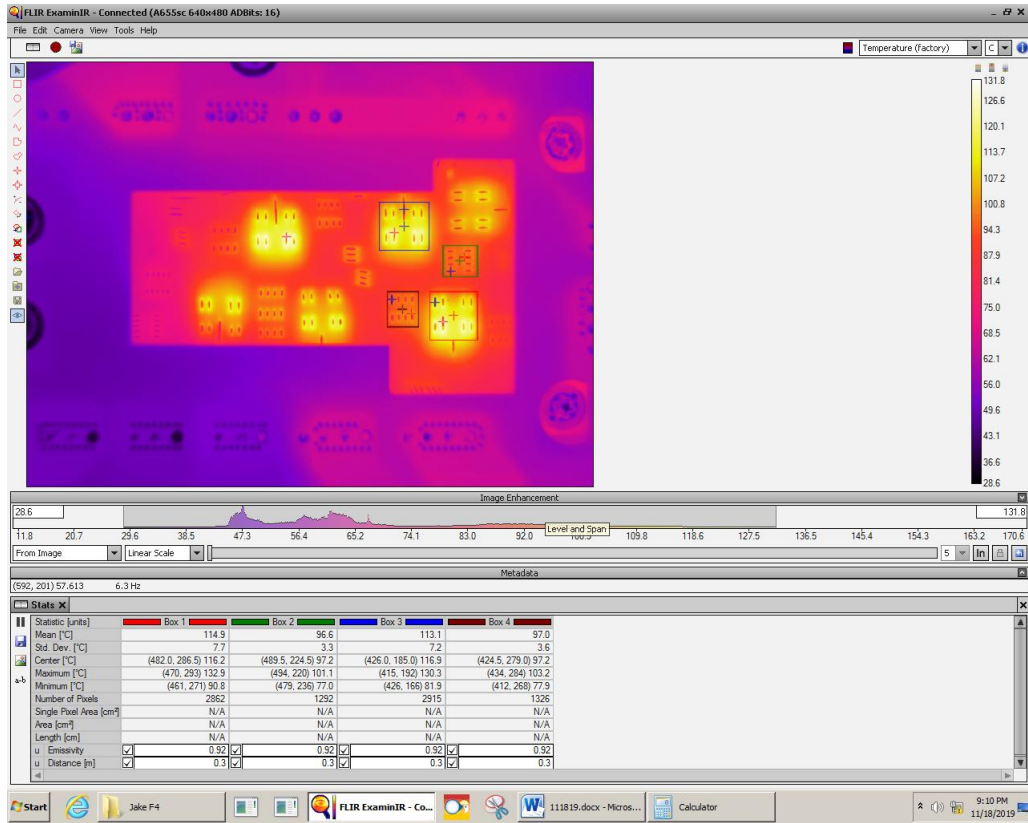


Figure 6. 14. SVPWM at $\theta = 0^\circ$ and $V_{dc} = 700V$

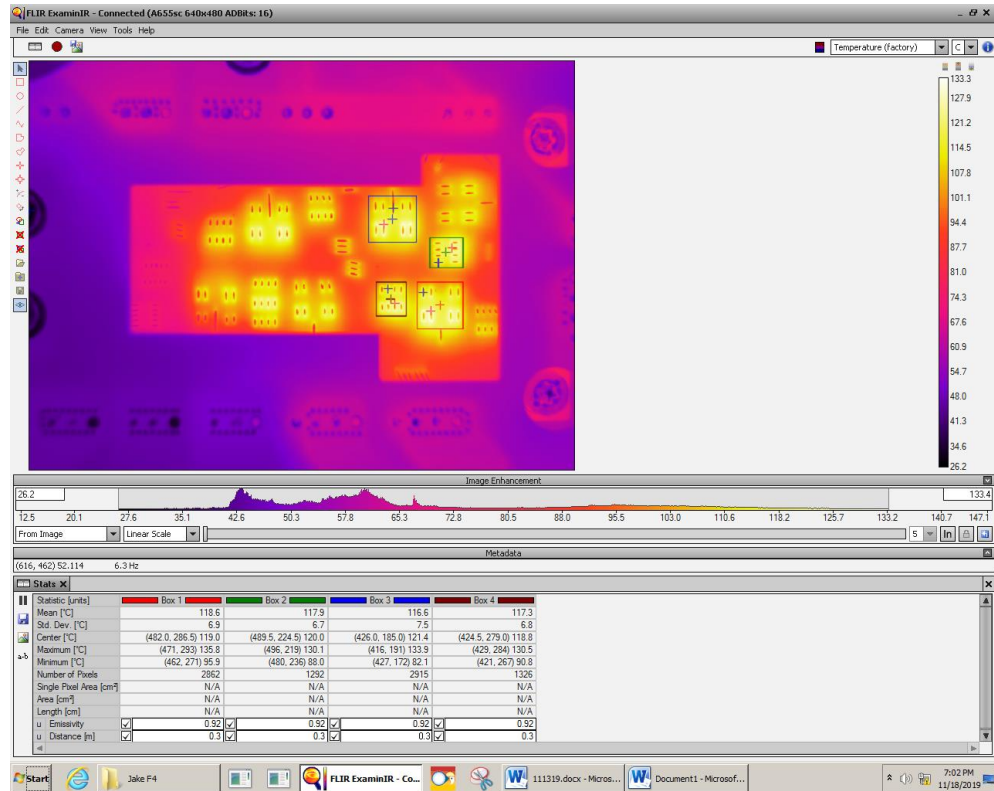


Figure 6. 15. SVPWM at $\theta = -180^\circ$ and $V_{dc} = 700V$

Summarized average junction temperature results for transistor and diode in single leg are shown in Figures 6.16 and 6.17. Only single transistor and diode are selected because of the symmetry between top and bottom leg in one phase. Thermal results are recorded at rated conditions listed in Table 6.1 for DDPWM and SVPWM at varying load angle $-180^\circ < \theta < 0^\circ$.

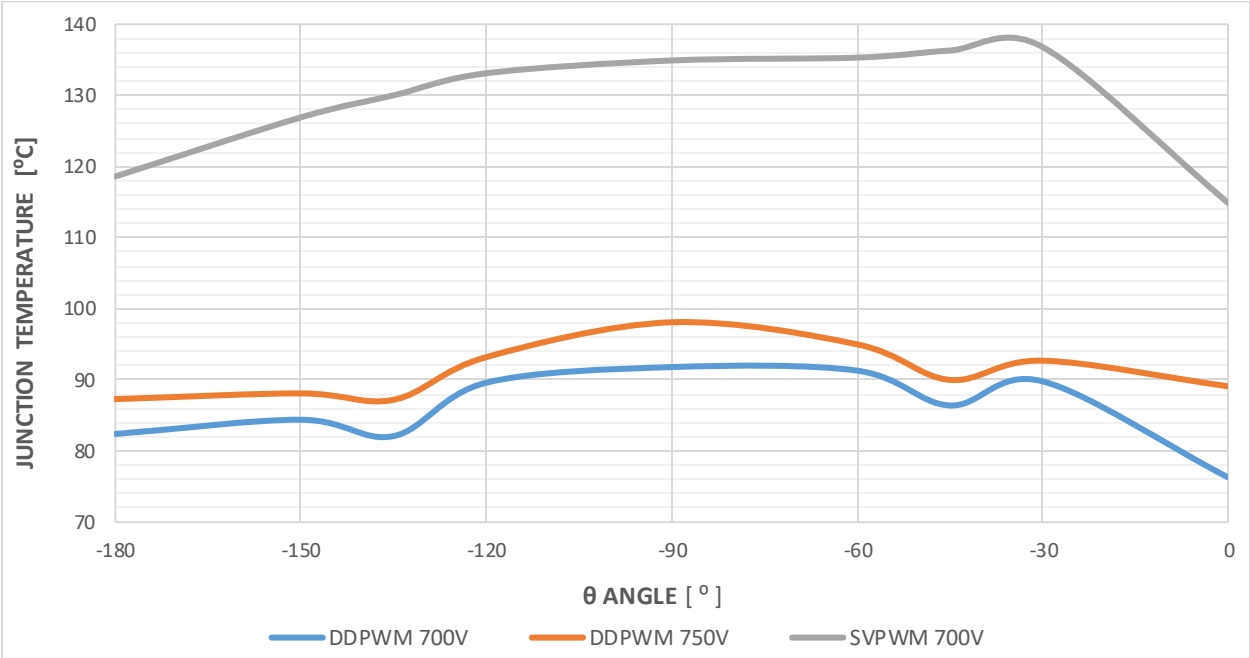


Figure 6. 16. Average Transistor Junction Temperature for range of θ values

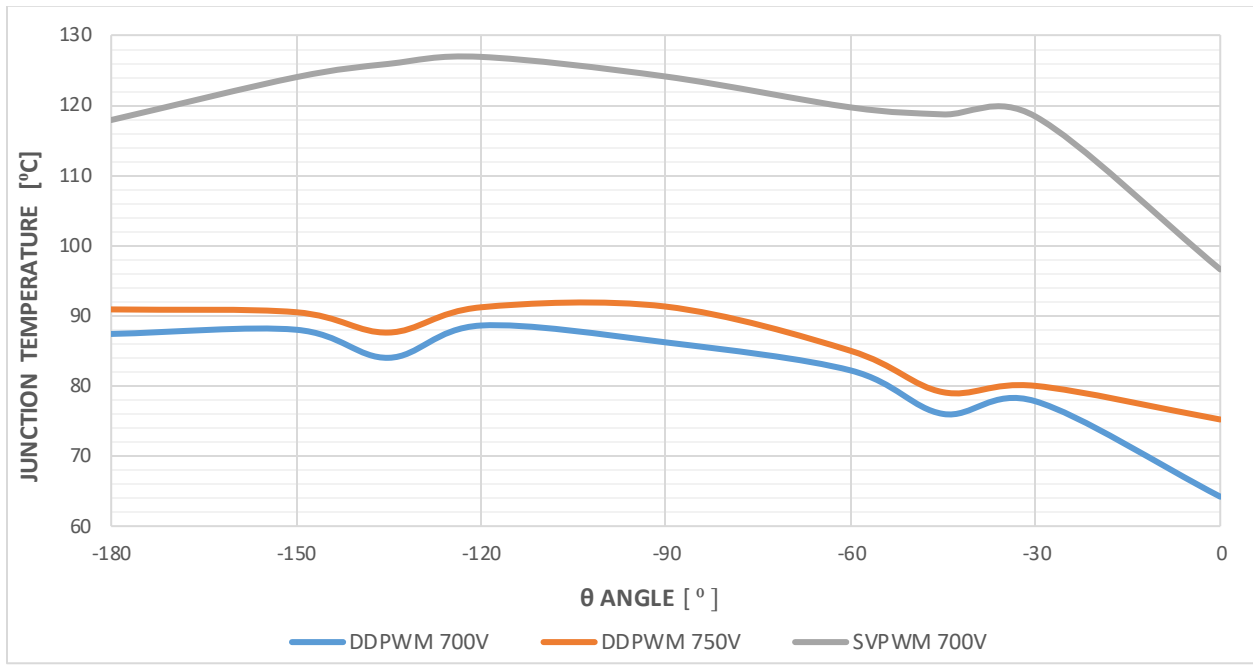


Figure 6. 17. Average Diode Junction Temperature for range of θ values

DDPWM was tested at two different dc bus voltage setpoints, but because of thermal limitations of power module, reflected through maximum allowable junction temperature, SVPWM could only be tested at $V_{dc} = 700V$. Since line voltage of 480V is set at fixed value during testing, in order to keep operation within linear mode of modulator, only negative values of phase angle are tested. As shown in Figures 2.14 and 2.15 of chapter 2, at fixed modulation index value m , symmetry in power losses for transistor and diode exist between $-180^\circ < \theta < 0^\circ$ and $0^\circ < \theta < 180^\circ$, thus justifying testing in negative range based on symmetry. As already described in chapter 2, Transistor peak average losses occur at $\theta=0^\circ$ while diode peak losses occur at $\theta=-180^\circ$. Power losses of individual switches contribute to final junction temperature values by creating a temperature rise over individual thermal resistances R_{jc} and individual R_{cs} . and that trend can be clearly seen in Figures 6.16 and 6.17. On the other hand, common thermal resistance R_{csm} and R_{sa} form temperature rise based on the total module losses as demonstrated in Figure 2.16, where module peak power losses occur around $\theta=-90^\circ$. That is reflected in Figures 6.16 and 6.17 thru maximum junction temperature for both transistor and diode peaking around

reactive power operating condition for DDPWM. Additional impact to consider is that modulation index m is not constant throughout the full range of $-180^\circ < \theta < 0^\circ$, and will be highest at $\theta=0^\circ$ and $\theta=-180^\circ$ and lowest at $\theta=-90^\circ$, which will also have an effect final temperature distribution, and lowering peak temperature values. By comparing DDPWM to SVPWM junction temperature values and distribution for transistor and diode, it is clear that DDPWM provides significant advantage in thermal performance across the full phase angle θ range, which will increase efficiency, power density and/or rating of the MTI.

6.4. Harmonic Performance Testing

In order to evaluate harmonic performance of DDPWM algorithm, performance test is performed as per setup shown in Figure 6.2. For accurate measurement of harmonic data, Lecroy Waverunner oscilloscope with compatible current clamp and differential voltage probes is used. Three phase current measurement data is saved in comma separated value form and used further for analysis by importing into Matlab first. After that, Simulink model is used for processing of harmonic data, which is then recorded back in excel datasheet form using Matlab script. All harmonic testing results are recorded at rated conditions listed in Table 6.1 at varying load angle $-90^\circ < \theta < 90^\circ$. An example of the three-phase current waveforms captured at $\theta = -90^\circ$ is shown in Figure 6.18.

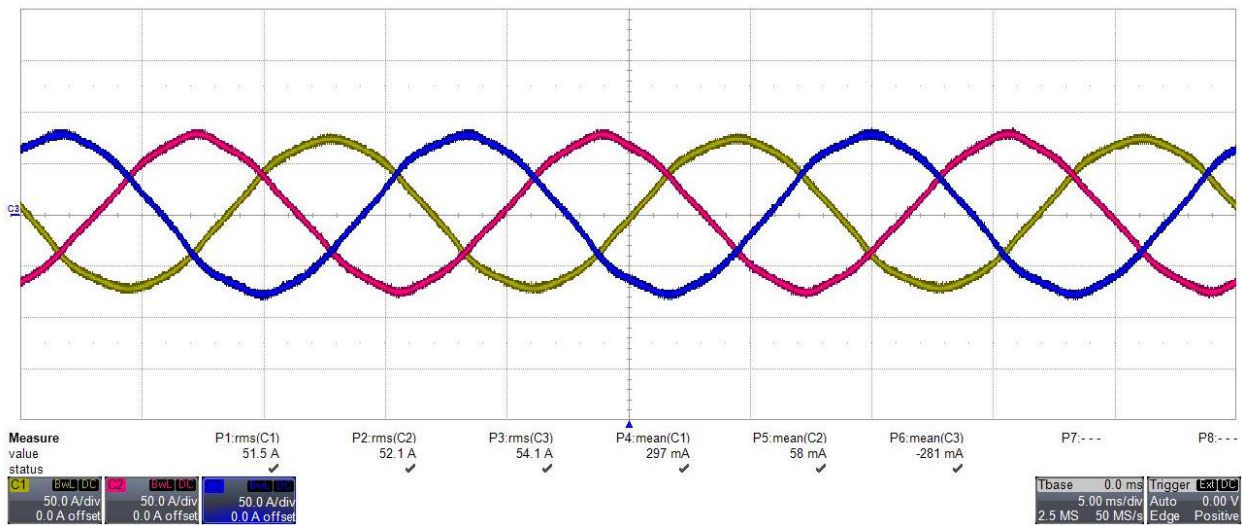


Figure 6. 18. Three-phase currents at $\theta = -90^\circ$

In order to demonstrate clamping action of DDPWM algorithm at different load angles, additional voltage measurement between positive DC bus terminal and output phase terminal is introduced. Voltage clamping measurement in combination with current measurement in the same phase shows periods where switching is omitted. Such waveforms for $\theta = -90^\circ$, $\theta = 0^\circ$ and $\theta = 90^\circ$ are shown in Figure 6.19., 6.20. and 6.21. respectively.

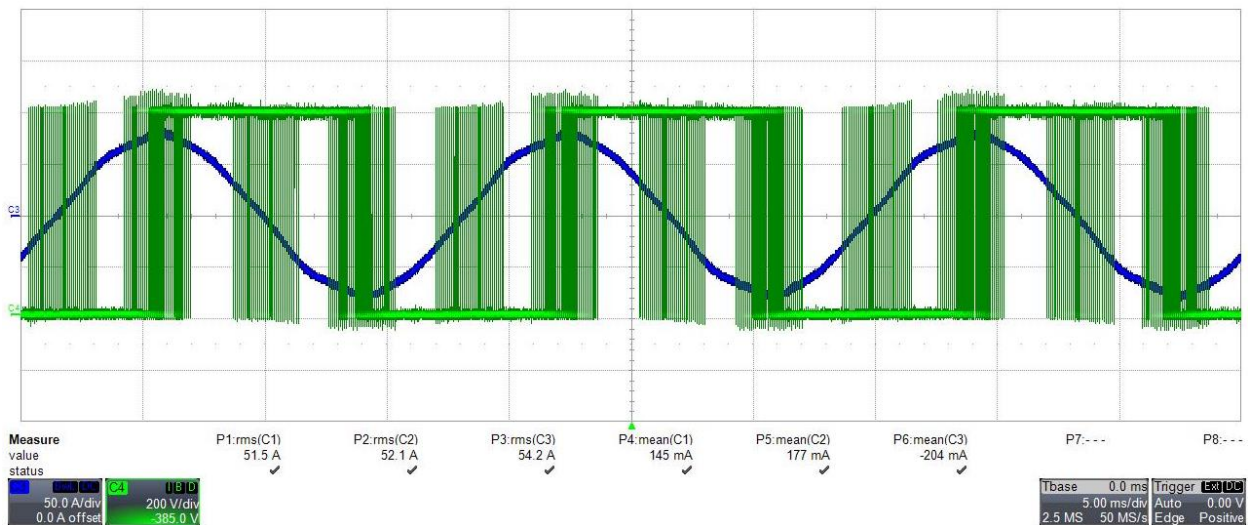


Figure 6. 19. Clamping voltage and current at $\theta = -90^\circ$

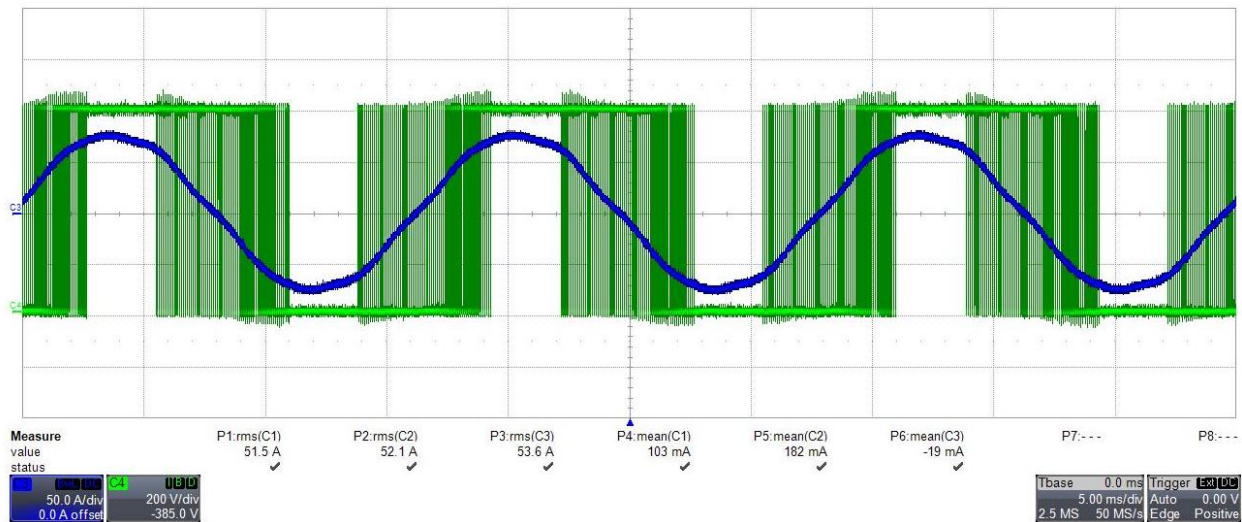


Figure 6. 20. Clamping voltage and current at $\theta = 0^\circ$

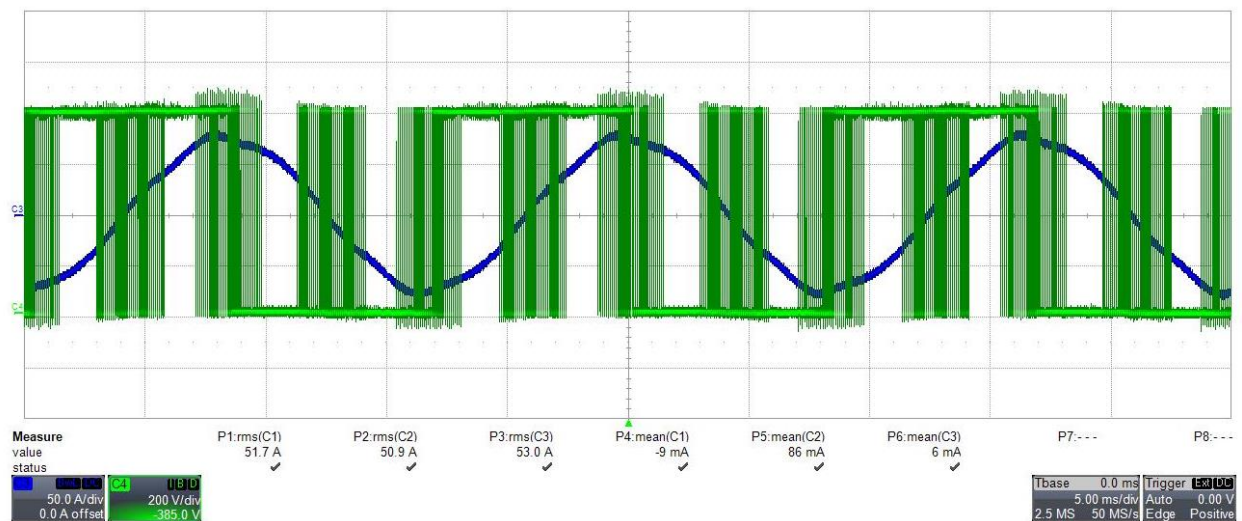


Figure 6. 21. Clamping voltage and current at $\theta = 90^\circ$

Thermal testing was tested in $-180^\circ < \theta < 0^\circ$ range and did not require testing in positive angle range due to symmetry in thermal behavior of semiconductor elements. However, for harmonics testing symmetry, it is required to test $-90^\circ < \theta < 90^\circ$ range, as per DDPWM pattern shown in Table 2.1 of chapter 2. Therefore, it means that for harmonics testing it is necessary to provide full reactive power support, which for given line condition requires elevated dc bus voltage to avoid overmodulation. Since power structure used has a strict operating dc bus voltage limit of

800V, all harmonics testing was performed at $V_{dc} = 790V$. Because of that, reactive power supporting condition at $\theta = 90^\circ$ is in initial overmodulation range and produces additional low order harmonics that are noticeable in Figure 6.21. Summarized plot of the low order current harmonic spectra for full angle range $-90^\circ < \theta < 90^\circ$ is shown in Figure 6.22.

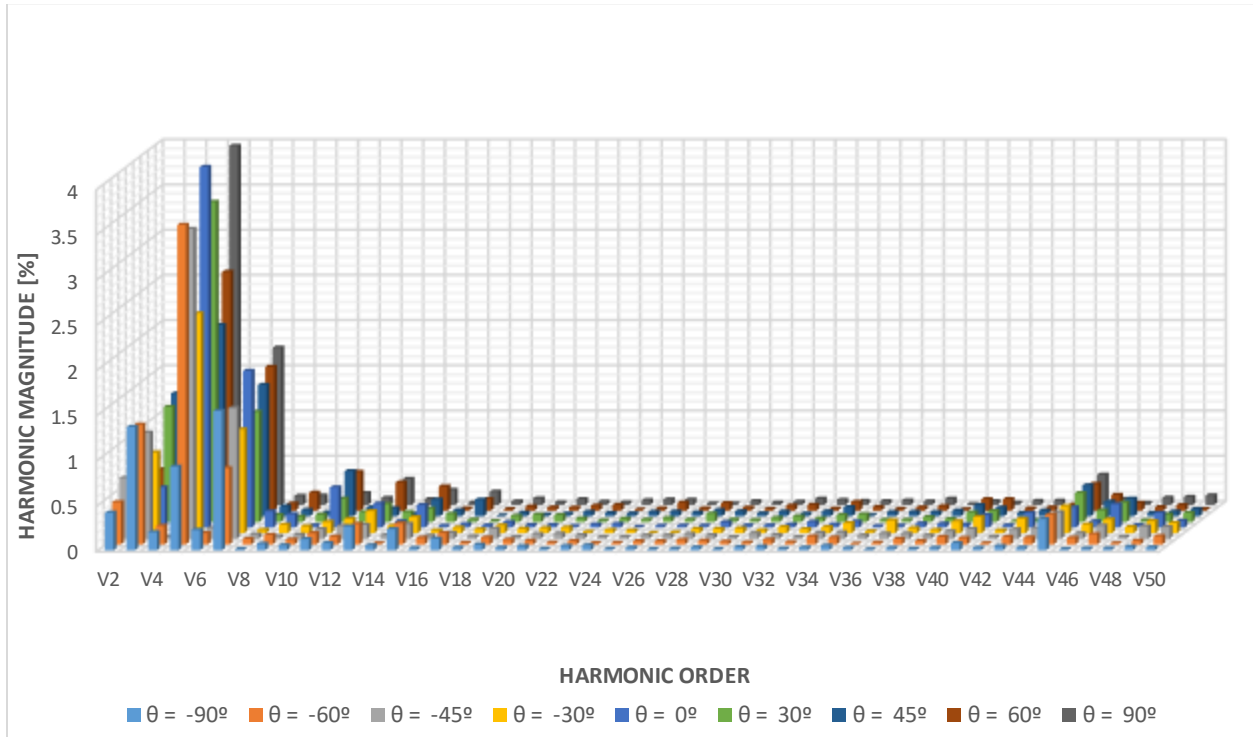


Figure 6. 22. Low Order Current Harmonic Spectra for $-90^\circ < \theta < 90^\circ$

Individual values of all harmonics meet requirements listed in first row of table 3.1. Test setup is connected directly to 2 MVA transformer on the grid utility side, which makes line impedance lower than 0.5%, and meets $I_{sc}/I_L < 20$ requirement, which is reflected in Tables 3.2 and 3.3. Filter resonance is present around 45th harmonic for all operating angles, and with the addition of external damping resistor, was hardest one to reach limit of $< 0.3\%$, as per table 3.2. Due to aforementioned processor limitation leading to synchronized sampling, active resonance damping was not implemented, and harmonic performance solely relies on passive damping.

Summary of TRD along with the STHD for first 10, 15, 20, 30, 40 and 50 harmonics is shown in Figure 6.23.

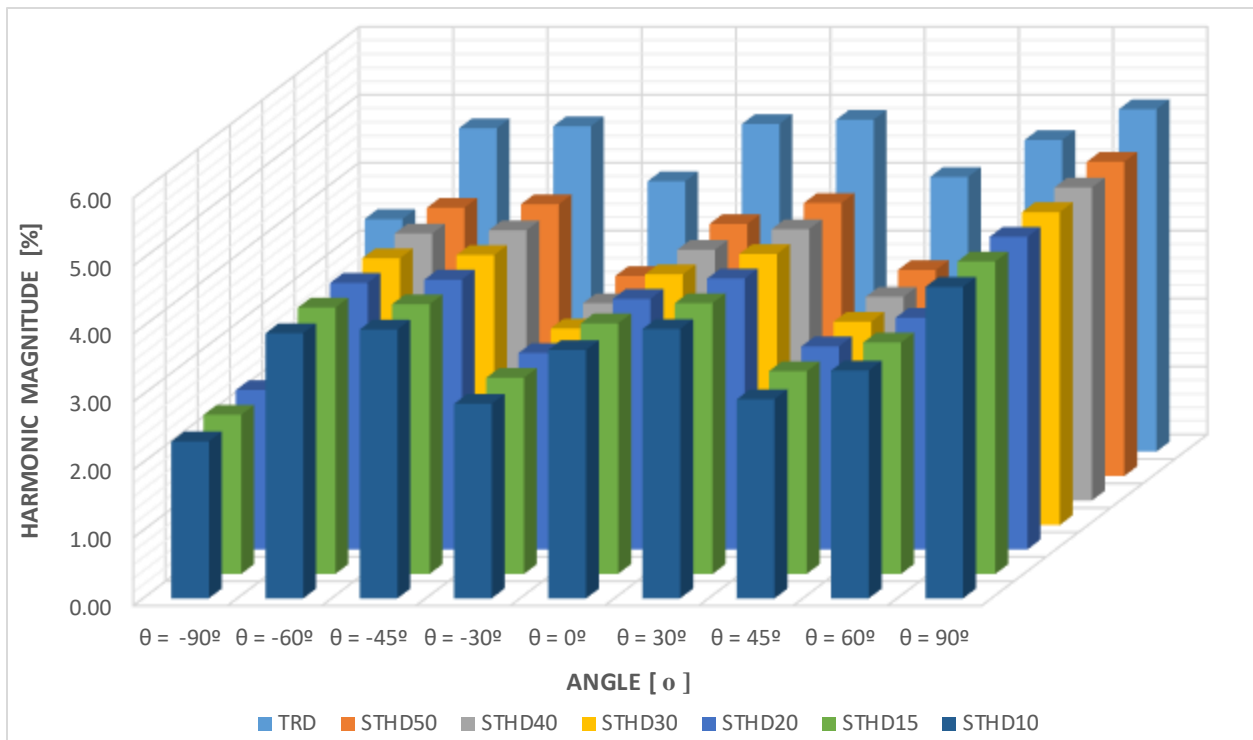


Figure 6. 23. TRD and STHD10/15/20/30/40/50 for $-90^\circ < \theta < 90^\circ$

Harmonic performance for all various phase angle values meet $TRD < 5\%$ limit as defined in Table 3.2. Clearly, lower order harmonics, especially 5th and 7th, within the first 50 harmonics are dominant, as per conclusions in chapter 3.1. As dead time T_d is defined as the major parameter affecting low order current harmonic performance, testing at different dead times is performed. Initial dead time setting for previous harmonic testing was set at $T_d = 0.64\mu s$. Multiplication factor of 2, 4 and 6 is used for comparison at $\theta = -90^\circ$ condition, low order harmonic spectra is summarized in Figure 6.24.

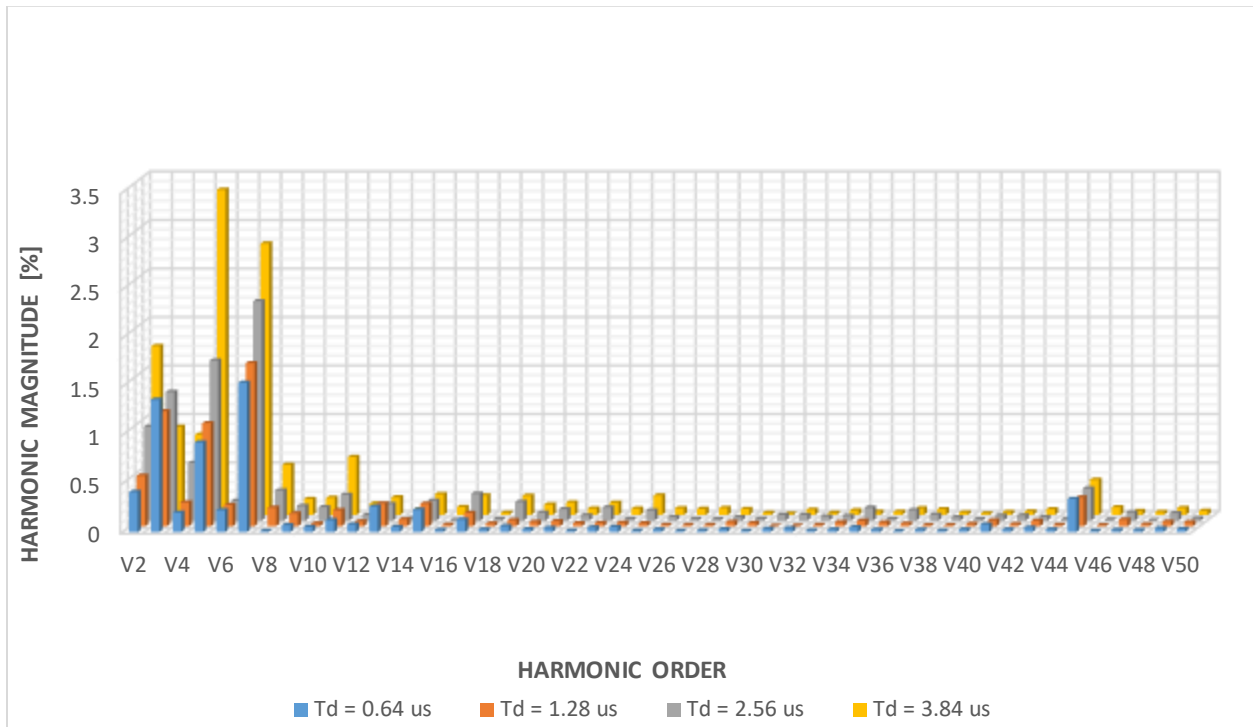


Figure 6. 24. Low Order Current Harmonic Spectra for $0.64\mu s < T_d < 3.84\mu s$

Harmonic Measurement data in Figure 6.24. shows that dominant low order harmonics have a characteristic that can be approximated as linear in relation to dead time value, which is in line with conclusions made in chapter 2.5.3. One major observation is the presence of even harmonics that also exhibit similar behavior and almost linearly increase with changes in dead time. Carrier frequency for testing is selected as large odd triplen multiplier of fundamental frequency, as per table 6.1, which should eliminate possibility of even harmonics being created by modulation, as per chapter 2.5.1. However, even harmonics are unique to experimental setup, and are consequence of DC offset present in measurements that are not fully being compensated in control loop. Three-phase current waveforms captured at $\theta = -90^\circ$ and $T_d < 3.84\mu s$ is shown in Figure 6.25.

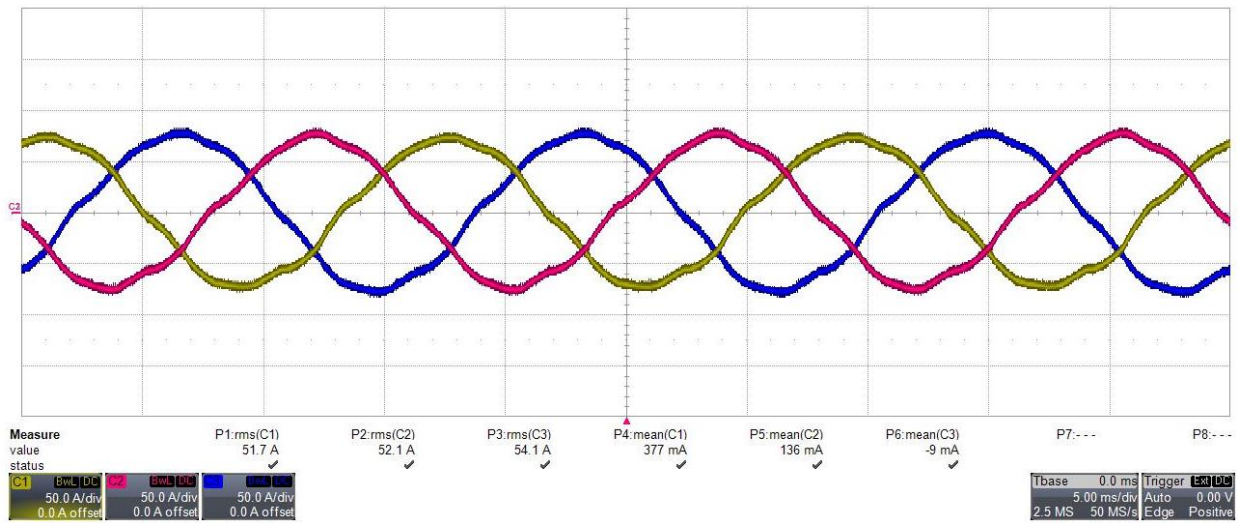


Figure 6. 25. Three-phase currents at $\theta = -90^\circ$

As compared to Figure 6.18, three phase current waveforms look significantly distorted, and with calculated TRD=5.96% do not meet required harmonic limits.

7. Conclusions and Future work

To best of authors knowledge, this is first published work analyzing impact of microgrid performance requirements on holistic microgrid tie inverter design. Despite inverter design commonalities, there are many unique design requirements imposed on microgrid tie inverters, which are dictated by the nature of microgrid system. Those major challenges listed below, along with full state of the art review, have been analyzed in details as part of this work:

- Capability for full rated reactive power support
- Stable closed loop operation free of power oscillations
- Operation under reduced power quality
- Decoupled control of active and reactive power
- Operation under varying input impedance
- Limited harmonic performance

In response to the listed challenges, following nonconventional control and modulation techniques that provide performance improvements of the microgrid tie inverters are proposed and analyzed:

1. Dynamic Discontinuous Pulse Width Modulation (DDPWM) as a primary inverter modulation technique used for more efficient inverter operation under full power factor range
2. Grid Voltage Feedforward control for improved harmonic performance of inverter under distorted microgrid voltage condition
3. Decoupled Power Control for independent active and reactive power control of the inverter, free of mutual coupling.

As part of DDPWM, simple implementation algorithm with specific adjustments to MTI application is proposed. Derivation of semiconductor loss expressions along with full thermal study is performed. Complete harmonics study with major parameter impact analysis is considered. Low pass filter design guidelines for DDPWM along with parameter influence is introduced. Impedance and circuit-based analysis of the filter is performed. State space models of various filter types is derived for both reference frames.

Under digital control system modeling and implementation portion of the work, closed loop system performance and stability is analyzed for various control topologies. Universal current controller parameter selection guideline is presented. Input impedance expression of a closed loop system is included. Newly proposed grid voltage feedforward and decoupled power control techniques are analyzed, and derivation of controller parameters and performance of each technique is fully evaluated.

Finally, experimental test setup and results for microgrid tie inverter is presented as proof of concept.

Opportunity for future work comes naturally due to greater utilization of wide bandgap devices in microgrid tie inverter applications in future. Wide bandgap devices introduce higher carrier and sampling frequencies, which create different performance challenges and opportunities at the same time. Topics like electromagnetic compatibility or active harmonic compensation, for instance, are some of the topics that would require further research in future.

CURRICULUM VITAE

ZELJKO R. JANKOVIC

ACADEMICS

UNIVERSITY OF WISCONSIN-MILWAUKEE (UWM), Milwaukee, WI

- Ph.D. Electrical Engineering, June 2020 Cumulative GPA: 3.8/4.0
 - Concentration in Power Electronics
 - Minor in Mechanical Engineering (Control Systems)

UNIVERSITY OF BELGRADE, Belgrade, Serbia

- B.S. Electrical Engineering, July 2009 Equiv. Cumulative GPA: 3.5/4.0
 - Department of Power Electronics & Electric Drives

PATENTS, ACHIEVEMENTS & HONORS

- 3 Patents and 7 Rockwell Automation Innovation Awards
- Chancellors Awards in 2010, 2011, 2012 - excellent performance in graduate school at UWM
- 2nd Place Winner, Electric Machines Field - Elekrijada 2008, International student contest in Electrical Engineering, Budva, Montenegro

PROFESSIONAL EXPERIENCE

ROCKWELL AUTOMATION – LOW VOLTAGE DRIVES, Mequon, WI

Project Hardware Engineer (May 2018 – current)

- Engineering lead for Hardware Design Projects supporting Existing and Legacy Low Voltage Drives products.
- Engineering lead for Failure Analysis and Engineering Support on Complex Customer Issues.

ROCKWELL AUTOMATION – LOW VOLTAGE DRIVES, Mequon, WI

Senior Hardware Engineer (May 2015 – May 2018)

- Engineering Hardware Design Projects supporting Existing and Legacy Low Voltage Drives products.
- Failure Analysis and Engineering Support on Complex Customer Issues.

ROCKWELL AUTOMATION – LOW VOLTAGE DRIVES, Mequon, WI

Electrical Engineer, Intern (May 2014 – May 2015)

- Prototyping, testing and evaluation of Parallel IGBT Modules in Drive applications.
- Design and testing of a Precharge Circuit for Panel Mount Active Front End drives.

UNIVERSITY OF WISCONSIN – POWER ELECTRONICS AND MOTOR DRIVES LABORATORY, Milwaukee, WI

Research Assistant (September 2009 – May 2015)

- Modeling and Implementation of a Microgrid-tie Power Inverter.
- Integrated Alternative Power Systems (IAPS) – collaboration between UWM and Eaton Corporation.
- Modeling of a complex DFIG based wind turbine system coupled with Zinc-Bromide battery energy storage.

ROBERT BOSCH – RESEARCH AND TECHNOLOGY CENTER, Palo Alto, CA

Electrical Engineer, Intern (May 2013 – September 2013)

- Assembled and tested a complex real time control and testing system for high capacity Li-Ion cells.
- Testing and Analysis of multiple battery types.

EATON CORPORATION – INNOVATION CENTER, Milwaukee, WI

Electrical Engineer, Intern (May 2012 – September 2012)

- Analysis and prototyping of a new type of AC-to-AC converter.
- Developed novel control strategy and modulation technique.

ABS MINEL TRAFU, Mladenovac, Serbia

Electrical Engineer, Intern (May 2009 – September 2009)

- Successfully performed multiple transformer prototype tests along with the data analysis.

SKILLS

- Relevant Graduate coursework: Digital control of electric drives, Advanced power electronics, Advanced machine design modeling, Advanced linear systems analysis, Optimal control, Adaptive control, Robust control

- Technical Interest: Power Converter design, Controls applied in Power Applications, Magnetics design
- Modeling & Simulation Software: Matlab, Simulink, PSCAD, Psim, Simplorer
- Rockwell Automation Software: Drive Observer, Drive Executive, RSLogix 5000
- Programming Software: C, Pascal
- Controller Development Package: dSpace, GPDSP Board, eZdsp
- General Software: Microsoft Office Suite
- Multilingual: Fluent in English and Serbian