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MODELING AND VALIDATION OF COMMON-MODE EMISSION IN SILICON CARBIDE BASED VOLTAGE SOURCE CONVERTERS

by

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ABSTRACT

MODELING AND VALIDATION OF COMMON-MODE EMISSION IN SILICON CARBIDE BASED VOLTAGE SOURCE CONVERTERS

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Under the Supervision of Professor Robert M. Cuzner

Electromagnetic compatibility (EMC) issues have become one of the most difficult challenges in power converter designs. With the invention of wide bandgap (WBG) power semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) power MOSFETs, the power converter designs are provided with the potential to be significantly more power dense than older generation converters using silicone IGBTs. However, the majority of spectral contents of the switching waveforms are moved from the very-low-frequency (VLF, 3 kHz to 30 kHz) range to low-frequency and up to the very-high-frequency (VHF, 30 MHz to 300 MHz) range. Moreover, due to the design traits of WBG-based converters, common-mode (CM) emission dominates the EMC problems. Conventional electromagnetic interference (EMI) modeling methodologies in the frequency range in and above VHF were mostly developed for applications where the power level is relatively low. For high-power and highly power-dense applications, new EMI modeling methodologies, especially in CM, need to be developed to allow more accurate analysis, more efficient design processes, and more optimal designs.

This doctoral dissertation documents the author's development of a novel CM emission modeling methodology with a set of CM model segments that form canonical SiC-based voltage source converters and the surrounding electrical environment, such as filter structures. The accuracy of all these model segments is validated with two applicational scenarios at frequencies up to 30 MHz. These modulized building blocks and the methodology using these blocks to construct full converter system CM models are lightweight and insightful, thus enabling more optimal design processes for SiC-enabled high-voltage and high-power-density converters such as virtual prototyping processes and multi-objective optimization. Furthermore, the discoveries of this dissertation will help power electronics designers to understand better the potential and challenges of the utilization of SiC semiconductors in voltage source converters.

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NOMENCLATURE

Abbreviations

AFE	Active front-end (converter)
CEM	Common-mode equivalent model
CM	Common-mode (voltage, current, impedance, *etc*.)
DEM	Differential-mode equivalent model
DM	Differential-mode (voltage, current, impedance, *etc*.)
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FEM	Finite element method
HF	High frequency (ITU designation, 3 MHz to 30 MHz)
MF	Medium frequency (ITU designation, 300 kHz to 3 MHz)
MM	Mixed-mode (voltage, current, impedance, *etc*.)
RF	Radio-frequency
VFD	Variable-frequency drive

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VHF	Very high frequency (ITU designation, 30 MHz to 300 MHz)
VSI	Voltage-source inverter
VSR	Voltage-source rectifier
WBG	Wide Bandgap (Semiconductors)

Other symbols

λ	Wavelength
$\mathcal{R}$	Magnetic reluctance
ω	Frequency (angular)
C	Capacitance
f	Frequency (in Hertz)
j	Unit imaginary number $\sqrt{-1}$
L	Inductance
R	Resistance
s	Frequency (complex) $j\omega$
V_x, I_x	Voltage and current expressions in Frequency-domain
v_x, i_x	Voltage and current expressions in Time-domain
Z	Impedance (complex)

Physics constants

μ_0	Permeability in vacuum
ε_0	Permittivity in vacuum

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Chapter 1

Introduction

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1.1 Research background and motivation

1.1.1 Wide bandgap device enabled power converters and electromagnetic compatiblity

Electromagnetic compatibility (EMC) in wide bandgap (WBG) semiconductor-enabled power converters has drawn increased attention in recent years. The trend is guided by two main factors: the introduction of new power switches and the paradigm shift of power systems. With the introduction of WBG power switches, features such as high edge rate and high switching frequency enabled power converter designs with better power density and power quality. However, with these features, the WBG power switches generate dominating switching harmonics and other induced noises over a much higher frequency range compared with older-generation power switches. These nuances have changed the focus of signal filtering for power converters from the power quality requirement spectrum (below 20 kHz [22–24] in VLF range) to the electromagnetic interference (EMI) mitigation spectrum (up to 20 MHz for conducted emission and up to VHF range for radiated emission [21, 25–27]). Figure 1.1 shows a comparison between the spectrum contents of a Si IGBT and a SiC WBG MOSFET in similar operating environments. Entering the new frequency ranges challenges to design optimal EMI mitigations also arise. The conventional methodology for designing filters is getting obsolete, and engineers can easily come up with under-optimal filter designs.

At the same time, a paradigm shift in power system design is taking place regarding the role of power electronic converters. Instead of only serving as motor drives for the majority of the applications in the past, power electronic converters are taking up roles as interfaces among subsystems and power grids in environments such as microgrids and smart grids. In many cases, these subsystems can contain numerous pieces of equipment, such as high-speed digital devices and radio-frequency (RF) communication devices, which are much more vulnerable to EMI than loads such as electric motors. To

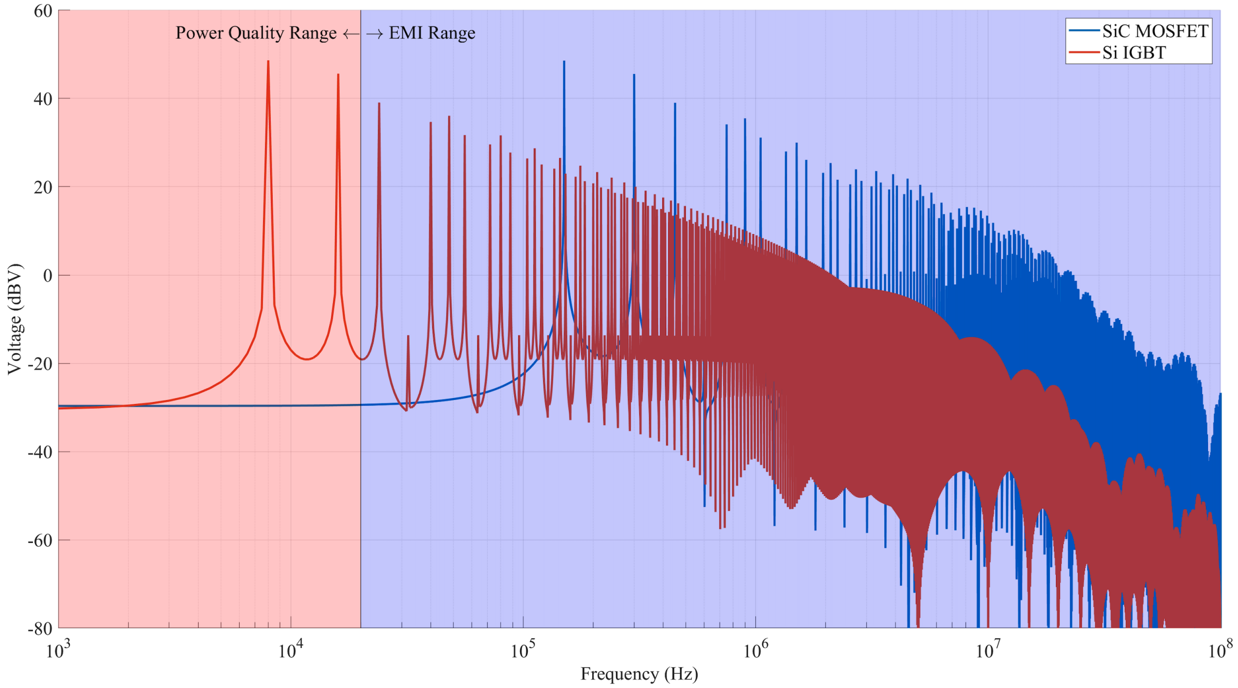

Figure 1.1: Idealized switch voltage spectrum content comparison of Si IGBT (Red, 600 V, switching frequency $f_{sw} = 8$ kHz, voltage rising edge $t_r = 30$ ns, voltage falling edge $t_f = 80$ ns) and SiC WBG MOSFET (Blue, 600 V, $f_{sw} = 150$ kHz, $t_r = 34$ ns, $t_f = 22$ ns).

better understand the EMI emitting sources, identify these sources, and establish closed-form expressions to predict EMI characteristics can make design-optimized EMI mitigation for newly designed power converters much more effortless and efficient.

Generally speaking, for a system to achieve EMC with respect to itself, *i.e.* intra-system compatibility, and its surrounding environment, *i.e.* inter-system compatibility, it has to generate no EMI that jeopardizes the functionality of both within itself and its surrounding environment. On the other hand, the system must also be capable of sustaining EMI from its surrounding environment, *i.e.* EMI susceptible. These interference sources can be intentionally designed (*e.g.*, gate signal of a power switch, RF communication signal) and un-intentionally designed (*e.g.*, high-frequency contents of a power switch waveform). The EMI both generated by and received by this electric system can travel via paths and frequencies that are intentionally designed (*e.g.*, existing circuits) and not intentionally

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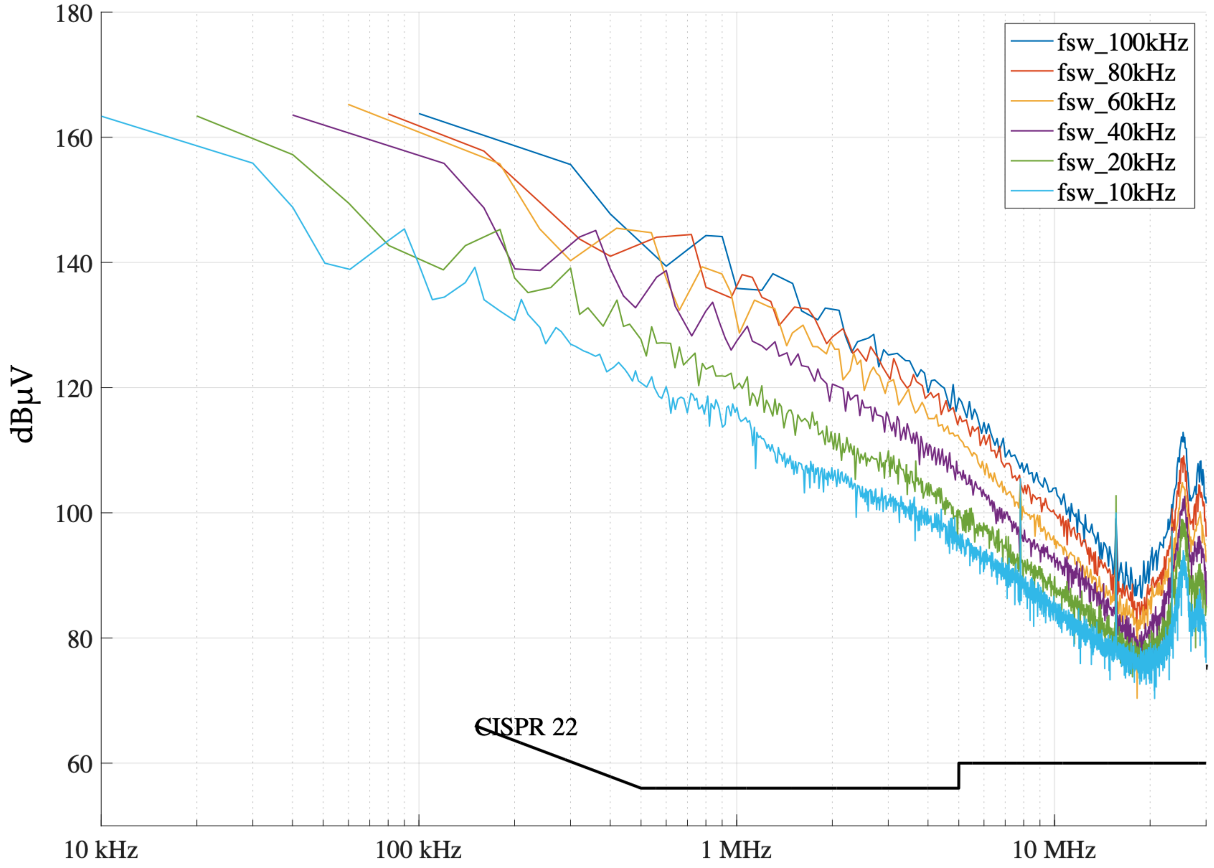

Figure 1.2: Switching voltage (source to drain voltage of a MOSFET) in an unfiltered three-phase full-bridge voltage source inverter operating under different switching frequencies (450 V dc, 60 Hz modulation, 10 kW load, Wolfspeed XM3 module)

designed (*e.g.*, leakage paths, system ground) [28].

1.1.2 Power converter EMI characterization methodology

EMI characterization with accurate mathematical or empirical-based modeling techniques provides quantified insights into the EMC design challenge. The quantification and identification of EMI sources can bring the potential for optimizing mitigation design and EMI reduction. The design process can also be more efficient by reducing the scale and number of physical experiments, reducing simulation time, and reducing unnecessary margin (*e.g.*, over-designing in filters). Moreover, when a method quantifies the EMI with very light-weighted computation, the iteration operation can become affordable to allow the implementation of automated optimization algorithms.

One of the most important pieces in characterizing the EMI produced by a power electronic converter is the modeling of the converter and its surrounding system with accuracy that suffices the system requirement. To ensure compatibility and convenience in filter and control designs, the model is mostly developed into an electric circuit representing the dominant EMI-producing behavior (utilizing switching waveform, parasitic elements, *etc*.) of the physical system. With power-dense converter designs, the relatively small physical dimension provides many conducting and radiating paths for common-mode currents. Almost all EMI of power converter related study available presents some modeling methods for common-mode EMI. But it is dangerous to perform common-mode EMI analysis separately from different-mode EMI. It is discovered that circuit asymmetry will lead to cross-mode coupling between common-mode and differential-mode currents [29, 30]. However, circuit asymmetry is occasionally inevitable, and circuit symmetry does not guarantee less EMI [31]. Closed-form expressions of the EMI source in common-mode and differential-mode offer great potential to identify and quantify EMI sources. Engineers can utilize these analytical methods to discover possible trade-offs between circuit structure and EMI, prevent mitigation over-design, and avoid excessive trial-and-error style experiments.

1.1.3 Power converter EMI mitigation requirement

The increased availability of WGB power semiconductor MCPMs has correlated to the emergence of an increasing number of conference papers and journal manuscripts aimed at understanding the true impact of WBG devices on filter volume minimization across a range of three-phase grid-connected Power Electronic Converter (PEC) applications, generally, in the past decade. Most of this work applies across a range of applications, with a major caveat being whether or not the closed-loop control approach is considered

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part of the filter design methodology. The control considerations for the grid-forming inverter do not apply to this study, but the grid-following inverter control and filter design requirements closely align with those associated with the AFE. Prior to 2016, the majority of the literature covering AFE filtering, with some exceptions, was directed toward Power Quality (PQ) filtering without consideration of EMI filtering. Research published on EMI filtering, especially those that emphasize the mitigation of CM EMI, has become more popular with the increment of WGB power semiconductor utilization. The distinction between the PQ and EMI mitigation is the range of frequencies that are covered by their corresponding industrial or military standards. These distinctions are delineated considering the frequency range break-outs of Figure 1.3. PQ filters work in conjunction with the AFE controls to meet Individual Harmonic Distortion (IHD), and Total Harmonic Distortion (THD) limits dictated by the PQ standards, such as IEEE 519 [24], which are applied to low-order harmonics of the fundamental frequency and switching frequency induced content up to 50^{th} harmonic of the fundamental frequency (*e.g.*, 3 kHz for a 60 Hz system, ELF to ULF in ITU designations [32]). The industrial conducted emission EMI requirement, such as the emission limits defined in CISPR 11 [21], EN 55011 [27], and FCC Part 15 [26] cover the frequency range of 150 kHz to 30 MHz (LF, MF, and HF in ITU designations [32]). The military standards, such as MIL-STD 1399 section 300b for PQ and MIL-STD 461G for EMI, divide these frequency ranges differently. These design requirements will be discussed in detail in the section 2.4.1.

In general, the PQ filter design has only a secondary impact on the low-order harmonics and principally impacts the IHD associated with switching frequency-induced spectral content. The EMI filter design addresses harmonics and other noises up to the MHz range, with the lower-end frequency limit established by the particular standard and application. Until the recent decade and excluding specialized space-constrained applications such as shipboard and aerospace applications, the conventional approach has been to separate AFE PQ and EMI filters into two separate assemblies so that each can

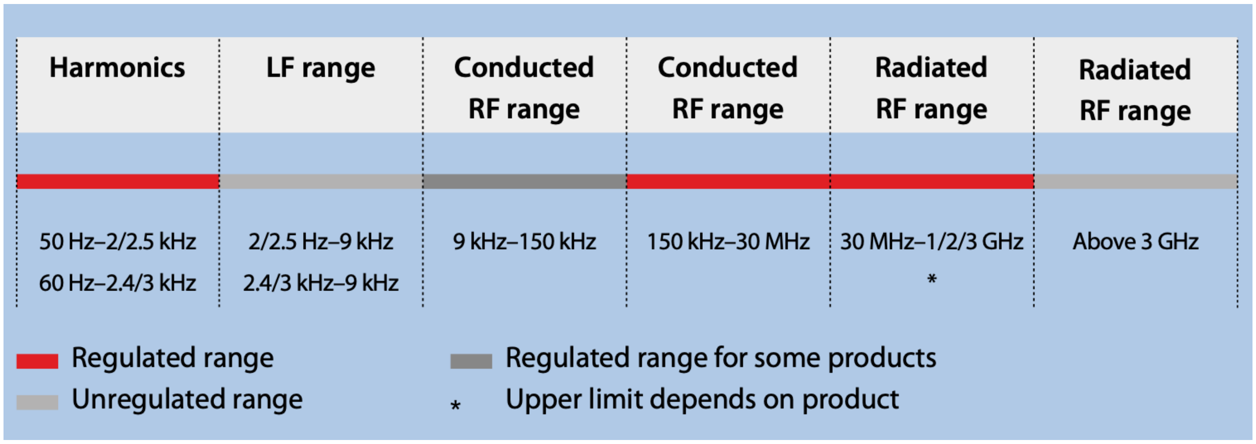

Figure 1.3: Frequency ranges defined by mainstream industrial standards [1]

be optimized over the frequency range that is covered. Applications demanding a high power density necessitate combining the PQ/EMI filtering into a single assembly. The integration of WBG devices into drive systems to achieve both higher power and, depending on the application, lower cost necessitates the application of the latter approach due to the fact that the switching frequency spectral content is driven into the range covered by the EMI standard, as shown in Figure 1.3.

With the utilization of WBG semiconductors, the spectral nuances generated by the converters no longer exist only in the lower frequencies (< 3 kHz, below ULF in ITU designation [32]) addressed by power quality standards. The high edge rate and switching frequencies enabled by these semiconductors are pushing these nuances towards frequencies covered by EMI standards that start at 150 kHz for most industrial standards. While the frequency range between 3 kHz and 150 kHz is unregulated by industrial standards, it does not mean the nuances should be ignored. Functional compatibility issues are still harmful to the system regardless of the absence of standard enforcement. Military standards, especially for the shipboard system, cover 60 Hz to 20 kHz for harmonic control, and EMI starts as low as the 2nd harmonic (120 Hz). Attenuation of conducted emissions in the spectral range of most EMI standards produced by the WBG-based VSR/VSI operating with higher switching frequencies will tend to drive up the required filter corner frequency(s), leading to smaller inductor-capacitor (LC) values and potentially smaller filter size, leading to increased power density. At the same time, the implementation of the control methodology, particularly for the AFE, places an upper limit on the filter corner frequency(s) and, hence, a lower limit on LC values and a corresponding reduction of filter size. These control constraints apply to the DM filtering requirements. On the other hand, the limits on achievable CM filtering requirements are constrained by other factors, such as the maximum allowable ground current imposed by the end-use installation. More challenges need to be overcome during the filter design. These challenges include the frequency-dependent characteristics of the physical realization of the filter, efficiency objectives, loss management, and component reliability.

The bulk of the research associated with VFD-BE filter design is aimed at mitigating the impacts of high $\mathrm{d}v/\mathrm{d}t$ on the motor winding insulation and CM current on the motor bearings. With the integration of WBG devices into VFDs to increase efficiency the seminal work discovering the impact of IGBT-based VFDs on motor insulation systems of the mid-1990s is being re-visited due to a significant increase in $\mathrm{d}v/\mathrm{d}t$ from WBG SiC MOSFET based VFD-BE, compared to IGBT-based. This consideration is the focus of the majority of the present-day VFD-BE filter design. However, there is a growing trend toward recognition of the impact of filter mitigation at the back end of the drive (VFD-side) on the PQ/EMI measurements made against required limits at the front end (AFE-side). As a result, there is a future trend toward more integrative approaches optimizing the roles of both VFD- and AFE- side filters together.

From the existing literature, it is apparent that significant room is left to research the optimal implementation of the voltage-source inverter (VSI) filters for WBG power semiconductor-based (principally SiC MOSFET) power converters. The opportunity to achieve high power density through increasing switching frequency has only barely been exploited. With the exception of the work by Boillat *et al*. [33] (which utilizes a 3L IGBT-based converter), the achievement of high power density at switching frequencies in excess of 40kHz has only been achieved through the use of SiC MOSFETs. All other applications utilize IGBTs. (Detailed review is included in Chapter 2.2.)

The most striking conclusion is that no studies were found that come to conclusive results regarding the optimization of AFE filter designs as a function of power rating and, in fact, the bulk of the reported work with physical hardware results is limited to $P_i \leq 10$ kW. Additionally, there has been no conclusive work on the optimization of the control approach and control hardware in order to fully exploit the use of SiC MOSFETs and (in the future) GaN MOSFETs to reduce overall size, weight, and cost of the VFD system. This gap in the research presents a tremendous opportunity and a critical need for the VFD industry if, indeed, the true value proposition of WBG power semiconductors to the VFD application is to be discovered.

1.2 Research overview

Motivated by the background described above, the author of this dissertation developed a set of lightweight, accurate, and modulized common-mode models. These common-mode analysis building blocks will enable power electronic designers to precisely understand the EMI behavior of WBG-enabled voltage source converters and to optimize EMI mitigation design accordingly. The set of common-mode model sections (*e.g.*, switching modules, common-core inductors) developed covers essential segments that form up a usual voltage source converter. When rearranged in applicational need, the common-mode behavior of a WBG-enabled voltage source converter, the operating environment (*e.g.*, test fixture, loads) attached differential-mode, and common-mode filters can be analyzed accurately and efficiently. Two major applicational scenarios were also utilized to validate all the developed common-mode model sections.

1.3 Document overview

Upon completion, this dissertation comprises five main chapters, one nomenclature table, two appendixes, and a bibliography. The first chapter describes the research background and motivation. Chapter two covers state-of-the-art reviews of various topics within the author's discipline of research. Chapters three and four documents the development and validation of the common-mode models in detail. Chapter five summarizes this dissertation.

Appendix A illustrates the author's engineering efforts that were made to support the modeling and validation process. Appendix B.1 covers some of the essential programming codes used during the validation process.

Chapter 2

State of the art review

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2.1 Conducted EMI characterization methodology review

This part reviews the state-of-the-arts methodologies of conducted EMI characterization for power electronic system. Various styles of EMI characterization methodologies have been invented by researchers around the globe [2,5–7,29,34–40]. In this dissertation, these methodologies are grouped under three categories based on their methods of deriving behavioral models: white-box based modeling, black-box based modeling, and "Gray"-box based modeling. The features and problems of these methodologies are also illustrated.

Conventionally, EMI induced by electronic equipment can be categorized into conducted emissions and radiated emissions. Because of the application requirement and operating frequency of the power switches, occasionally reaching the MHz range, most research efforts for EMI induced by power electronic equipment concentrates on conducted emission.

2.1.1 White-box Based Modeling

White-box based modeling comprises direct circuit modeling and finite element method (FEM) assisted modeling. Direct circuit modeling builds up the circuit with as many details as possible. Information required to develop these models includes data-sheet

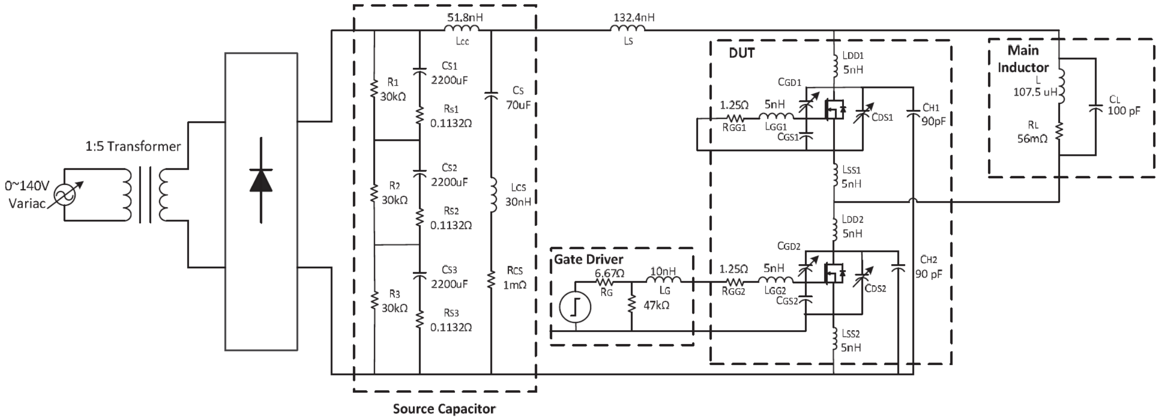

Figure 2.1: Circuit simulation with data-sheet details and measured parasitics. [2]

obtained gate-drive resistance and inductance, power switch on-state resistance, and directly measured equivalent series resistance (ESR) and equivalent series inductance (ESL) of capacitors (Figure 2.1) [2]. Circuit simulation with such a model would provide EMI prediction throughout the system, but data-sheet information is not always valid in different operation conditions and often contains misleading values. The level of detail is also fairly dependent upon the researcher's own bias. For example, Figure 2.1 shows a complex behavior model for the DC link capacitor but does not include information for common ground coupling amongst different sections. As a result, this model is missing important CM voltage and current information.

Modern electromagnetic FEM analysis software allows researchers to virtually construct a part of, if necessary entire, power electronic system and compute the electromagnetic response of the virtual model within a designated frequency span. FEM solver geometrically breaks virtual model surfaces into small triangles called a "mesh" (Figure 2.2). The solver calculates the field propagation through the shared boundaries of adjacent triangles with information such as permeability and other physical parameters of the material [3]. The solution acquired by such a process is extremely difficult if it is solved by hand, considering the size of mesh triangles needs to be at least two times smaller than the wavelength of targeted frequency in the material. EM Information obtained from FEM analysis can be used towards the structural redesign of system parts like bus bar to reduce EMI induced from the geometry of the physical structure (Figure 2.4) [4]. Some of these FEM tools also provide an automatic circuit generation function that translates the electromagnetic behavior of a physical model into an electric circuit model, or at least impedance information for certain parts. This modeling process can provide a very accurate behavior model within a designated frequency span [4, 41].

Despite the accuracy provided by white-box based modeling, this methodology is lack of the necessary agility for system-level optimization. The modeling and modification process can be too complex and time-consuming. Every tuning of the virtual model re-

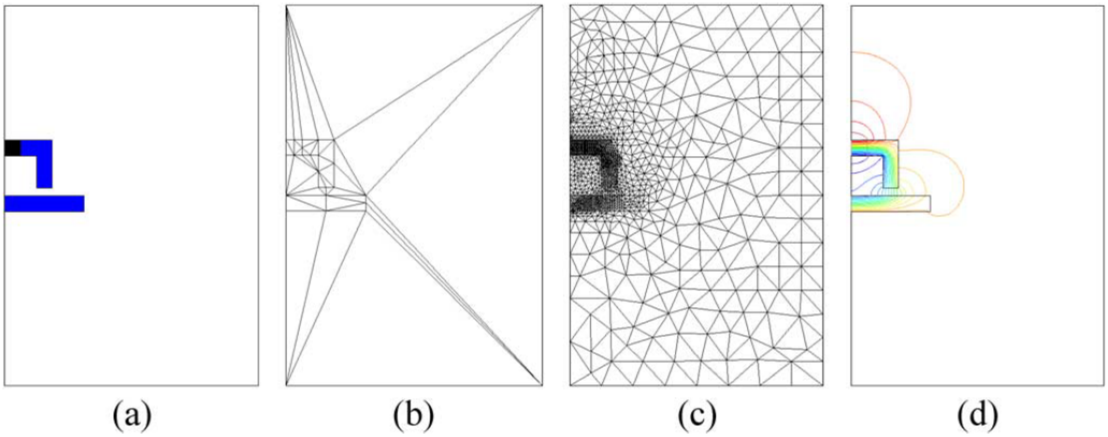

Figure 2.2: (a) Material composition of the problem (black-PM, blue (in online version)-ferromagnetic maternal, white-air). (b) Initialmesh. (c) Adaptive mesh after eight refinements (30% of the elements in the mesh are refined each time). (d) Equipotential lines of the solution. [3]

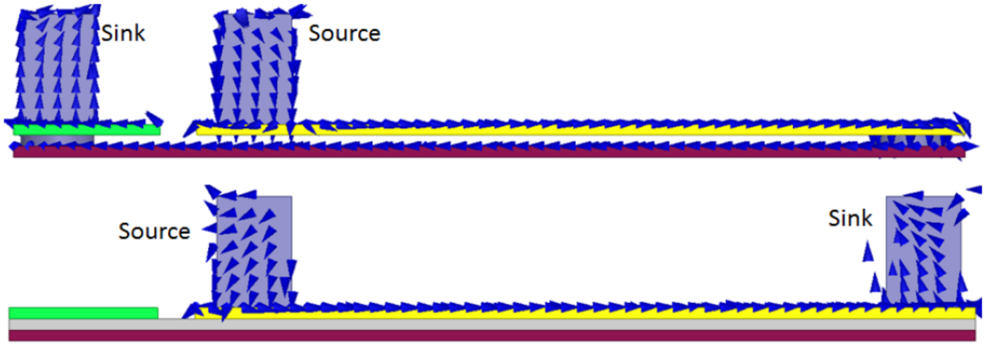

Figure 2.3: FEM simulation of current path configuration between source and sink [4]

quires manual manipulation and a completely new simulation of the entire model—the example in Figure 2.4 only contains a power module. The FEM model for an entire system, such as a motor drive, can be a significant burden for both the modeler and solver. The computational cost for either direct circuit modeling or FEM modeling is too high to achieve efficient iterating operation, an essential element for EMI mitigation optimization. Moreover, the white-box based modeling provides little insight into CM EMI analysis.

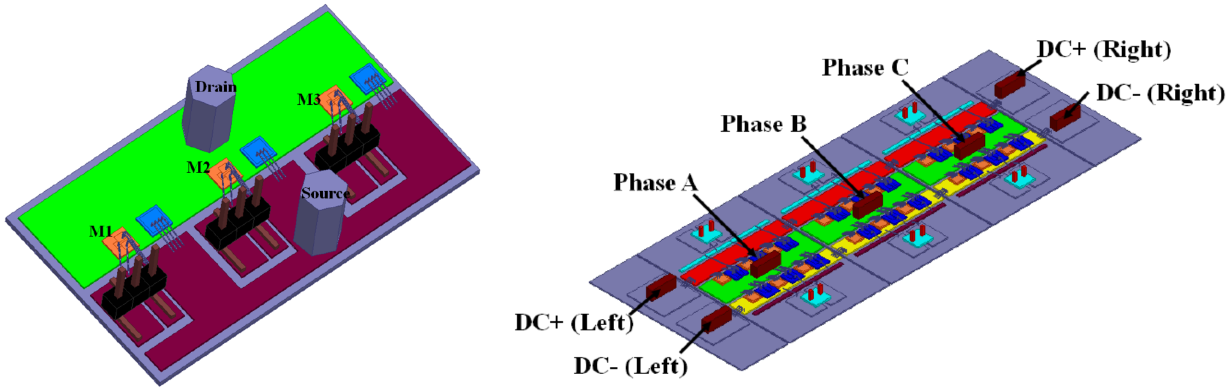

Figure 2.4: FEM simulation of single MOSFET and three switches power module. [4]

2.1.2 Black-box Based Modeling

Black-box based modeling utilizes vector network analyzers (VNA) or impedance analyzers to acquire scattering parameter (S-parameter) matrix of certain parts of a power electronic system. Based on the matrix and its corresponding transfer function, researchers can interpret a behavior circuit model, without more measurement or data-sheet information of individual details inside the measured network [5, 35, 42]. This method is widely used in radio-frequency (RF) researches and applications, where the multi-port network measurement can provide a relatively accurate reference over a designated frequency span.

When a section of a system has two ports (e.g., an one phase filter), a 2-by-2 scattering parameter matrix of this two-port network can be easily measured by a VNA. This scattering matrix stands for how the network's ports respond to EM wave injected into the network (e.g., S_{21} stands for the ratio of outward wave's amplitude on port two verses incident wave's amplitude on port 1.) [43].

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.1}$$

And this matrix can in turn transformed into an ABCD-network and apply to transfer function expressions [43].

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \tag{2.2}$$

where the voltages and currents are actual values on the port instead of wave amplitude. The transformation expression is as follows. Similar transformation can also apply to the impedance matrix.

$$A = \frac{(1+S_{11})(1+S_{22}) + S_{12}S_{21}}{2S_{21}} \tag{2.3}$$

$$B = Z_o \frac{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{2S_{21}} \tag{2.4}$$

$$C = \frac{1}{Z_o} \frac{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}{2S_{21}} \tag{2.5}$$

$$D = \frac{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}{2S_{21}} \tag{2.6}$$

The process, especially VNA measuring, requires the network under test to be terminated in turns with open, short, and matching loads (50 Ω in most RF system). For example, a "matching load" case will determine the terminated port has no "reflection" coming back from the load. Hence the returning power of said port is zero. From this assumption, the scattering parameter on the other port is isolated. By shorting and opening a port, other measurements can be isolated with a similar concept. However, the power systems are not usually designed to be impedance controlled like the RF system. A compromise was made in [5], which provides an extended black-box measurement process to improve the modeling accuracy. Another downside of this method is that the measurement is usually done without gating the switches, which loses vital information from switching waveform in EMI characterization. More details on the switching waveform will be discussed in the next section of this article.

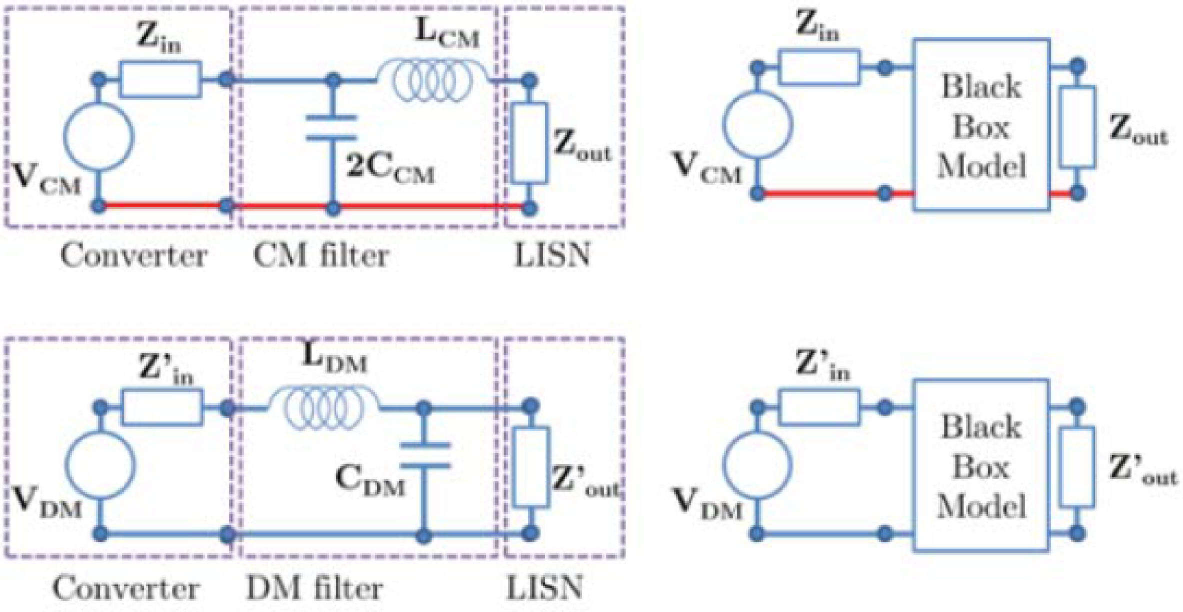

Figure 2.5: A black-box modeling example [5]

2.1.3 "Gray"-box Based Modeling

Unterminated Behavioral Modeling

The authors of this article categorize the methods developed in [6, 30, 44] as "Gray"-box based modeling. Instead of measuring a part of a system (e.g., an EMI filter) as in [5], [6] derived a behavioral model for the unterminated converter. Authors of [6, 30, 44] proved that a one-port terminated network model has limitations in accurately predicting DM and CM EMI. The one-port model utilizes measurement at the input end of the inverter while considering the entire system, including the load as a one-port network. This one-port modeling method, similar to some of the black-box based modeling methods, neglects the mutual effects between DM and CM noises.

[6, 30, 44] develops an unterminated behavior model. As shown in Figure 2.6, starting from a half-bridge behavioral model as Norton Equivalent current sources, the unterminated behavioral of a three-phase inverter can be used to predict EMI noise generated by the inverter itself in CM and DM. The authors used large capacitors to flood out the microscopic difference between parasitic Z_{PG} and Z_{NG}. This makes i_P and i_N only affected by I_{DM} hence isolating the CM current from DM current. The impedances in Figure 2.6 are retrieved by impedance measurement in the symmetric setup. Utilizing the model extracted from the symmetric setup, these impedances in asymmetric cases are retrieved by a curve-fitting process. This process provides an accurate prediction of EMI in CM and DM generated by an inverter. However, the curve-fitting process does not quantify the relation between EMI and circuit parasitics. This process also provides no modeling methods for the overall system containing filters and load.

Dominating Parasitics Based Modeling

Instead of mapping out all of the behavioral details like the direct modeling described above, [37] establishing a model where only major sources of EMI are measured and included can greatly save time and computational power. In addition, a circuit modeling technique is developed in [37] to mathematically decompose the system circuit into a common-mode equivalent circuit (Figure 2.7) and a differential-mode equivalent circuit. The equivalent circuits contain accurate information of CM/DM mutual coupling due to reasons such as circuit asymmetry and leakage current paths. This is a very powerful tool for CM and DM filter design and optimization [7, 45]. More details of the CM/DM decomposition method will be discussed in the next section of this article.

Furthermore, the method utilized accurately measurable on both the input and output side of the converter to induce a measurable current passage through the converter and ground. This makes it possible to isolate and measure the leakage current via converter chassis to the ground.

2.1.4 Supporting Analytical Tools

Besides circuit-level modeling and device-level FEM modeling, other analytical tools support EMI characterization. The authors select two of the essential tools and document them in this article: common-mode equivalent circuit modeling and switching waveform analysis.

Common-mode Equivalent Circuit Modeling (CEM)

CM EMI conducted emission has been a major problem since the introduction of WBG devices. [37] demonstrates a method to isolate the CM passages into an equivalent circuit model mathematically. This isolation is achieved by applying matrix manipulations to KVL and KCL equations of the mixed-mode circuit.

In general, any N-line circuit can be expressed with line currents (i_1, i_2, ... i_N)and line voltages to a designated reference point(v_1, v_2, ... v_n) on individual lines (Figure 2.8).

CM voltage and current are defined as:

$$v_{\text{CM}} \triangleq \frac{1}{N}\sum_{n=1}^{N} v_n \tag{2.7}$$

$$i_{\text{CM}} \triangleq \sum_{n=1}^{N} i_n \tag{2.8}$$

Differential-mode voltages are voltage drops between lines $v_{mn} = v_m - v_n$ and differential mode currents are $i_{mn} = \frac{1}{2}(i_m - i_n)$ as if line *n* is the "return path" of line *m*. With $N-1$ DM elements and one CM element, these definitions can be arranged into an $N \times N$ linear transformation so that the CM/DM derivation can be systematical as follows,

$$\underbrace{\begin{bmatrix} v_{12} \\ v_{23} \\ \vdots \\ v_{(N-1)N} \\ v_{\text{CM}} \end{bmatrix}}_{\mathbf{v}_{\text{DCM}}} = \underbrace{\begin{bmatrix} 1 & -1 & 0 & \dots & 0 \\ 0 & 1 & -1 & \dots & 0 \\ \vdots & & \ddots & & \vdots \\ 0 & \dots & 0 & 1 & -1 \\ \frac{1}{N} & \frac{1}{N} & \frac{1}{N} & \dots & \frac{1}{N} \end{bmatrix}}_{\mathbf{T}_v} \underbrace{\begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_{N-1} \\ v_N \end{bmatrix}}_{\mathbf{v}_n} \tag{2.9}$$

$$\underbrace{\begin{bmatrix} i_{12} \\ i_{23} \\ \vdots \\ i_{(N-1)N} \\ i_{\text{CM}} \end{bmatrix}}_{\mathbf{i}_{\text{DCM}}} = \underbrace{\begin{bmatrix} 1/2 & -1/2 & 0 & \dots & 0 \\ 0 & 1/2 & -1/2 & \dots & 0 \\ \vdots & & \ddots & & \vdots \\ 0 & \dots & 0 & 1/2 & -1/2 \\ 1 & 1 & 1 & \dots & 1 \end{bmatrix}}_{\mathbf{T}_i} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_{N-1} \\ i_N \end{bmatrix}}_{\mathbf{i}_n} \tag{2.10}$$

Left multiply the inverse matrix of $\mathbf{T}_v$ and $\mathbf{T}_i$, (2.9) and (2.10) become, ($\mathbf{T}_v^{-1}\mathbf{T}_v = I$, where I is the identity matrix.)

$$\mathbf{v}_n = \mathbf{T}_v^{-1}\mathbf{v}_{\text{DCM}} \tag{2.11}$$

$$\mathbf{i}_n = \mathbf{T}_i^{-1}\mathbf{i}_{\text{DCM}} \tag{2.12}$$

Applying this linear transformation (2.9) and (2.10) to any KCL or KVL expression of a circuit, a common-mode equivalent model (CEM) or differential-mode equivalent model (DEM) can be generated. Utilizing this method, one can easily examine the cross-coupling between CM voltages and differential mode voltages. The diamond-shaped "dependent" voltage source represents the DM influence in the CEM circuit (Figure 2.7). Moreover, with the CM voltages and currents accurately modeled, the design of CM filters and differential-mode filters can be optimized separately without losing the said inter-mode cross-coupling information.

Switching Waveform Analysis

One of the major sources of EMI in WGB-enabled power electronic systems is the fast edge rate of the power switch voltage. In addition to the high switching frequency introduced by WGB, a detailed analysis of the switching waveform becomes very important when characterizing the EMI in such systems [8]. In [8], the switch voltages are represented by a series of delta impulses in the third time-derivative (or forth, depending on the proposed signal shape). The derivative is easily reversed in the frequency domain. This simplification makes spectrum analysis of switch voltages very simple. It also provides a valuable tool to model the noise sources in EMI characterization mathematically. Voltage sources in behavioral models, such as shown in Figure 2.7, can be replaced with a mathematically generated model instead of measurement data to reduce the computational cost significantly.

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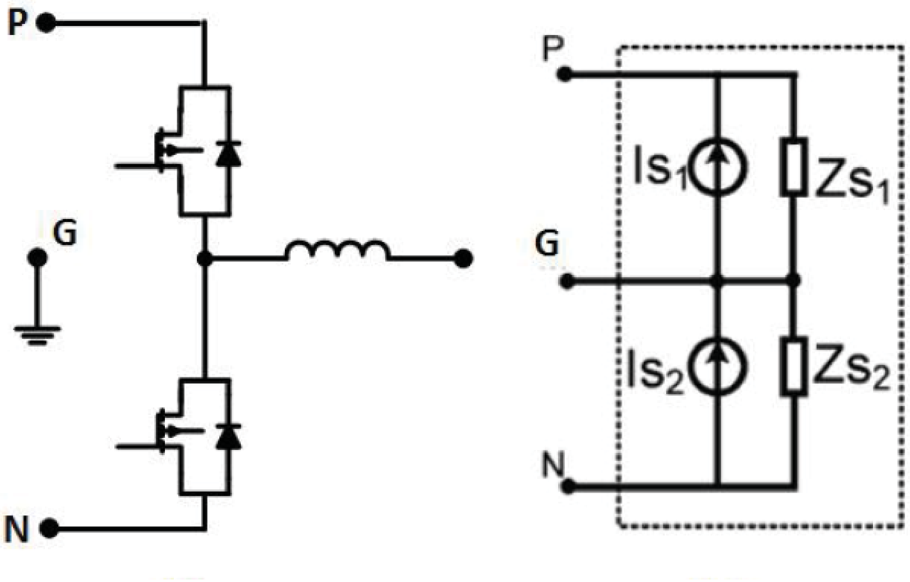
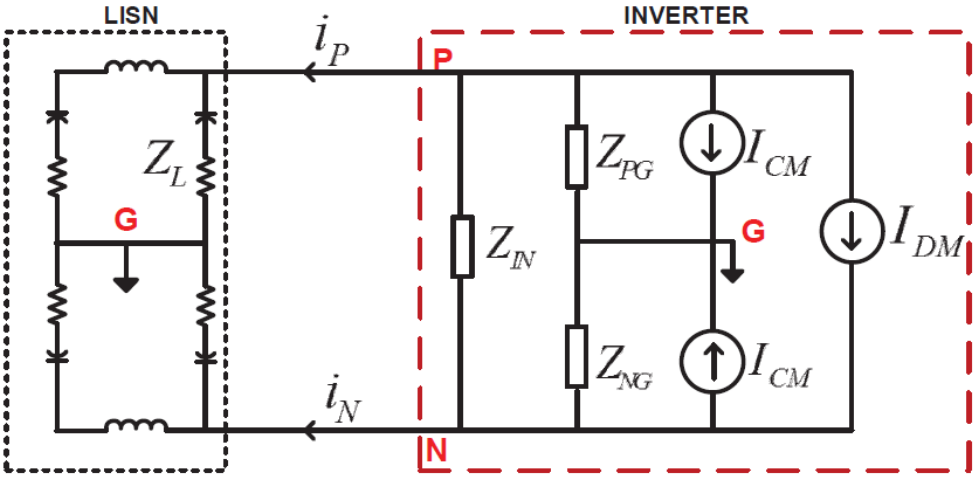
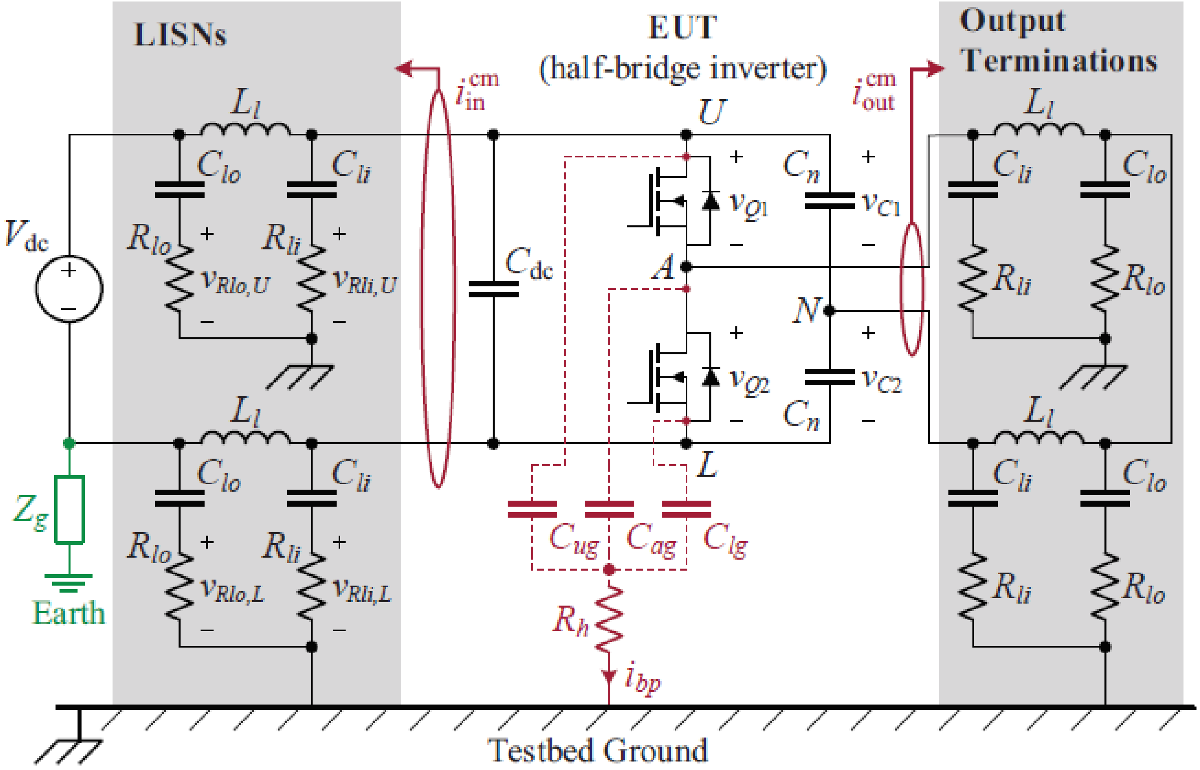


(a) Behavioral model

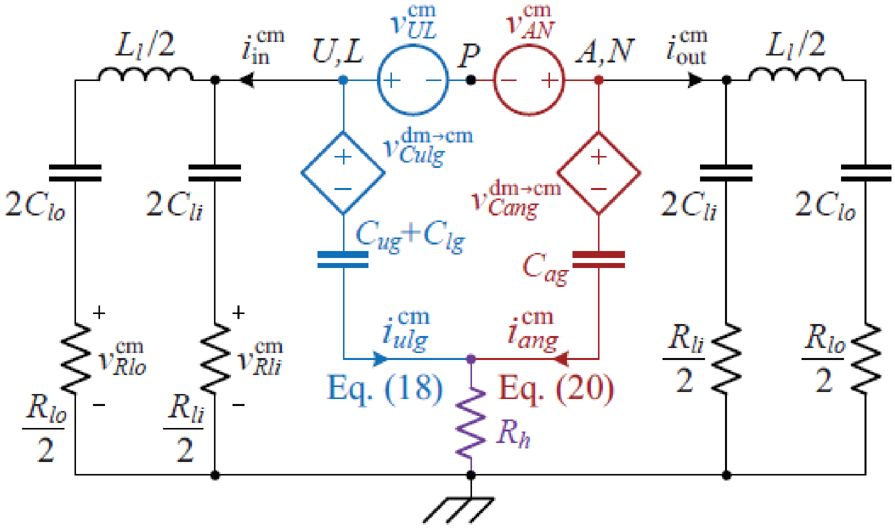


(b) Behavioral model with CM and DM voltage sources

Figure 2.6: Half-bridge converter circuit unterminated behavior model [6]



(a) The parasitic baseplate capacitance of the power switch module (in red) is proved to be the dominating factor of EMI of a WBG-enabled half-bridge converter.



(b) The derived CM equivalent circuit where colored part contains essential information of switching voltages, parasitic elements, and CM/DM cross-coupling due to circuit imbalance.

Figure 2.7: Dominating parasitics driving CM EMI [7]

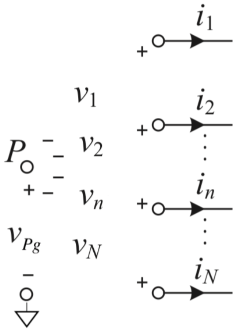


Figure 2.8: A general N-line circuit

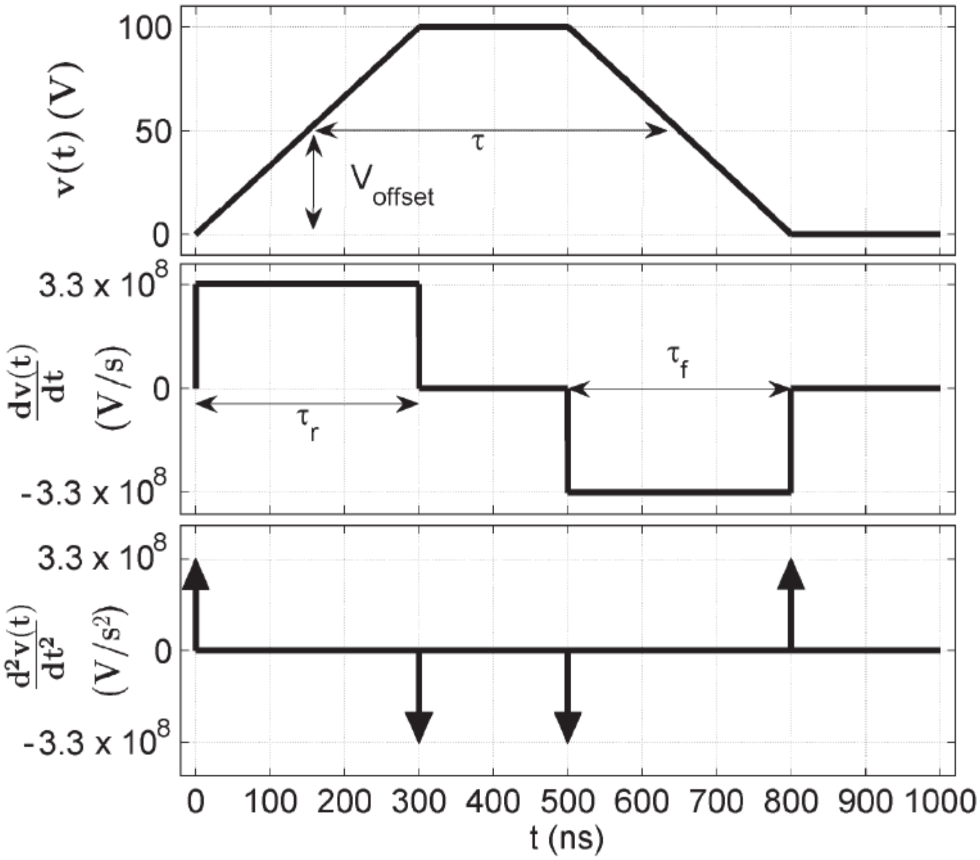


Figure 2.9: Waveform decomposition in time derivatives [8]

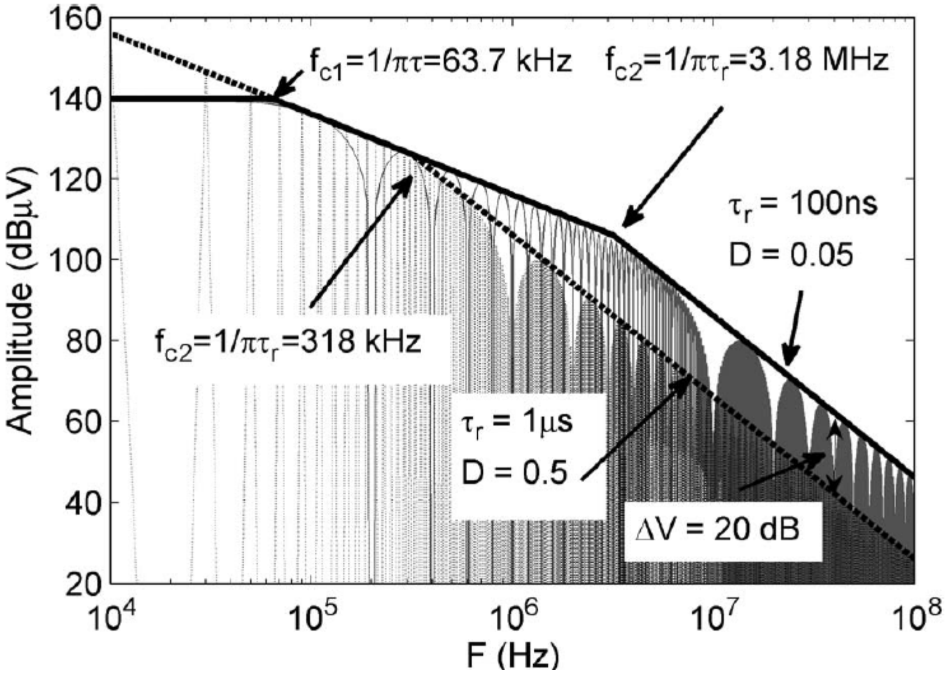


Figure 2.10: Waveform decomposition in frequency-domain [8]

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2.2 Voltage source inverter filter design review

This section reviews the state-of-the-art in methodologies and approaches found in the literature to maximizing the value proposition of Wide Band Gap (WBG) power semiconductors for the motor Variable Frequency Drive (VFD) *from the perspective of Active Front End (AFE) filtering*. The overall goal is to synthesize and organize together the most significant and meaningful published literature covering design processes and constraints for filter interfaces between the ac grid, assuming an AFE (as opposed to Passive Front End) interface to the variable frequency motor drive; this work also includes processes and constraints for dc link capacitor design. The focus of this study is only on the Voltage Source Converter (VSC), consisting of the AFE boost rectifier or Voltage Source Rectifier (VSR), feeding the VFD Back End (VFD-BE) Voltage Source Inverter (VSI).

This review effort attempts to understand the benefit of WBG to both commercial and military (principally shipboard naval) applications. Therefore the salient differences between PQ and EMI standards for these applications and how they influence the filter design approach are highlighted. As the existing literature was studied, the applied standards (PQ and/or EMI) were noted.

For low voltage (< 1 kV) applications, WBG power semiconductors with blocking voltage ratings ranging from 600 V to 1.7 kV are commercially available over a range of current ratings [46–48]. WBG devices in this range have the potential to impact nearly all products that require electrical power and of enabling new product development in the burgeoning energy market [49–56]. To date, the true *value proposition* of WBG power semiconductor technology to variable frequency motor drives has not been decisively determined [56–62]. As a result, it is challenging for VFD Original Equipment Manufacturers (OEMs) to determine whether or not internal research and development resources should be applied to the integration of WBG power semiconductors, such as the Silicon Carbide (SiC) or Gallium Nitride (GaN) Metal Oxide Semiconductor Field Effect Transistor (MOSFET), into future VFD product lines. WBG power semiconductors enable significant increases in switching frequency without loss penalty, which *should* lead to potential reductions in the size, weight, and cost of heat sinks, DC link capacitors, and ac grid/motor interfacing filters [63–70]. Additionally, as experience has been gained in the packaging and layout of WBG power semiconductor multi-chip power modules (MCPMs), another benefit has emerged: A reduction in the margin between the operational DC link voltage range and the device voltage breakdown rating [71]. This benefit has resulted from the critical need for MCPM device manufacturers to control parasitic inductances of MCPM packages without compromising thermal efficiency and lifetime [72, 73]. As a result, MCPM device layout and interconnection improvements have led to better utilization of the device in power electronic energy conversion systems. For example, SiC MOSFET-based MCPMs rated at 1.2 kV are now being applied to dc link voltages as high as 1 kV, whereas Insulated Gate Bipolar Transistor (IGBT) counterparts can only safely be applied with a maximum DC link voltage of 750 V. The key benefit to VFDs is that VFD-driven motors can be driven to higher speeds and can be rated at the same level as the applied ac grid $-$ or can be applied more safely to installations with a widely variant ac grid supply compared to present day IGBT-based VFDs. The increased range of system applications and/or performance improvements, in most cases, implies the incorporation of a boost rectifier Active Front End (AFE) into the VFD implementation. Therefore, it seems that the value proposition of WBG power semiconductors is most readily achievable with AFE-fed VFDs [10, 19, 71, 74].

On the other hand, recent research suggests that the main threat to achieving the WBG power semiconductor value propositions of high power density, higher efficiency, wider range of application and low system integration cost are management of the increased production Electromagnetic Interference (EMI) at the high end of the Radio Frequency (RF) spectral range [75–80] and (high dv/dt) [81–86]. Demonstrations of practical implementations demonstrate the need for an integrative design approach to achieve the full value proposition of WBG power semiconductors in system applications [60, 68–70, 87–

89]. The aim of this work is to help VFD OEMs understand the exact trade-offs that the threat/challenge of electromagnetic compatibility (EMC) presents to the WBG opportunity and to provide guidance on current best practices applied to achieving EMC in WBG power semiconductor based VFDs.

As will be pointed out, the control implementation of the AFE has an influence on the AFE filter design. This aspect of overall WBG-based VFD design will be addressed more rigorously in the second phase of this project. The goal of this document is to synthesize and organize together the most significant and meaningful work in the areas of AFE filter and dc link design in order to derive design processes and constraints on the filter interfaces between the ac grid and AFE and the dc link capacitors. This document will show how an integrative approach to AFE filter design has emerged that addresses both Power Quality (PQ) and EMI concerns.

Filtering requirements between the VFD-BE and motor are driven by considerations in addition to meeting PQ and EMI limits: Maximizing motor insulation and bearing life. These considerations introduce a different set of design constraints and processes. However, the considerations for VFD AFE and BE filter design comprise dual differential-mode and common-mode performance requirements. For the VFD-AFE filter, DM filtering is principally connected to meeting PQ requirements, and CM filtering is driven by the need to limit conducted EMI. For the VFD-BE filter, DM filtering requirements are driven by the need to control voltage stresses applied to the motor insulation system by high $\mathrm{d}v/\mathrm{d}t$ voltage pulses applied to the motor by the VSI. VFD-BE CM filtering requirements are principally driven by the need to limit CM current circulation between the motor and VFD chassis, which behavior contributes to a reduction in motor bearing life.

2.2.1 Overall Approach to VFD-AFE Filter Study

This document takes a unique approach to understanding and synthesizing the body of AFE filter design literature and applying it to the generalized VFD system shown in Fig-

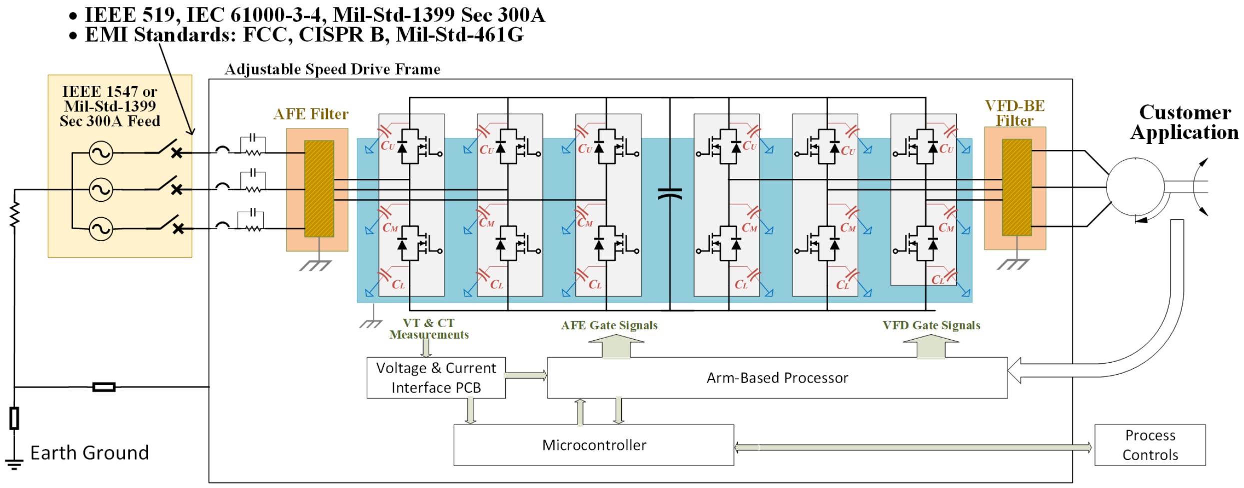


Figure 2.11: Generalized VFD system

ure 2.11. Tracking the evolution of AFE filter design approaches over the years and the influence of WBG power semiconductor integration, it is convenient to sort AFE filter designs into three classes and to document the filter design requirements (*i.e.*, power quality standards, EMI standards), power rating, and power density. Throughout the literature review process, the influence of the frequency spectral ranges on the filter design and optimization process, as broken down in Figure 1.3, is highlighted.

This review section identifies coverage in the existing literature on the competing performance objectives associated with the selection and design of VSR-VSI AFE, and dc links passive components, namely:

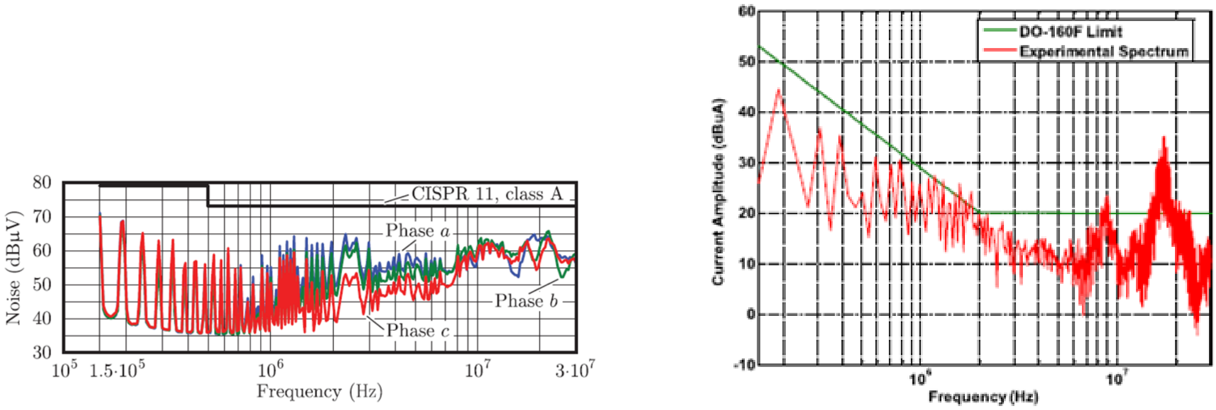
1. Steady-state and dynamic control-ability;
2. Minimization of filter stored energy;
3. Filter resonance;
4. External system parameter variations;
5. Required energy storage;
6. Limiting of conducted EMI.

Three classes of filters are proposed as a means of covering the range of filter types found in the literature. Multi-objective optimization criteria are considered, and state-of-the-art is synthesized in processes for both Power Quality and EMI filter design optimization and optimal sizing and selection of dc link capacitors/capacitance.

2.2.2 Detailed Summary of AFE Filter Design Approaches

This section covers the rigorous review of the literature on AFE filter design approaches. The approaches are organized and discussed according to the above-defined classes. Table 2.5 lists those papers that resulted in designed filter hardware results in the order of year published. There are several important observations. First of all, it is significant to note that, with the exception of just a few papers, the majority of the reported work is for systems having a power rating of less than 10kW. In order to represent a wider range of validated work, the study had to include AFE for a range of applications beyond the VFD and three-level (3L) Neutral Point Clamp (NPC) and T-Type (TT) VSRs had to be included, even though the intent of this study was to keep the focus mainly on the two-level (2L) VSR. The differences between 3L and 2L results can be accounted for principally by considering an effective doubling of the frequency of the fundamental components of noise-producing voltages. For example, the work by Boillat *et al*. [9], and Singh *et al*. [10] represent the most comprehensive approaches to AFE filter design, lining up with the objectives of AFE PQ/EMI filter multi-objective optimization to achieve the highest possible filter power density while keeping filter losses below levels that are thermally manageable. It is interesting to note that if the difference between NPC [9] and 2L [10] are adjusted for by doubling the device switching frequency of the NPC design. Both Boillat and Singh consider nearly equivalently rated systems (400V, 3kW, and 440V, 4kW, respectively), and both come up with nearly equivalent filter power densities for PQ/EMI-compliant systems.

If the switching frequency of Boillat's NPC-based VSR is doubled, then it appears that the systems developed by Bolliat *et al.* and Singh *et al.* represent equivalently matched noise sources, having an equivalent fundamental frequency of 100kHz, that each meets EMI compliance with a resultant filter power density of roughly 20 kW/L. These outcomes may set a baseline for what is achievable for VFD AFE filters rated at < 10 kW operating at the switching frequencies made possible by WBG power semiconductors, such as SiC MOSFETs. It should be noted that the work by Boillat *et al.* builds upon an aggressive heatsink design to achieve 50kHz with IGBTs and that such an approach is not common. Nevertheless, the approach of Boillat *et al.* is worthy of emulation. The work by Singh *et al.* is similarly significant in that it is representative of the approach required to maximize the switching frequency of SiC MOSFETs and thereby achieve the benefit of AFE filter power density. In this scenario, it is the losses and thermal management of the filter that will limit the switching frequency. Comparing these two works, there are a few nuances that require further exploration. First of all, the $\mathrm{d}v/\mathrm{d}t$ of the NPC IGBT-based system is, by its nature, significantly lower than the 2L SiC MOSFET system. This assumption is supported by the EMI test validation results from both papers shown in Figure 2.12. The authors in both works have optimized the EMI filter design to bring the conducted EMI, measured at a LISN according to the respective test set-ups, just below the limit lines. The EMI requirements of [10] and more stringent than those of [9], indicating that the SiC MOSFET-based 2L AFE can achieve a higher power density AFE EMI filter by moving EMI spectral content out to higher frequencies with a simple 2L converter (as opposed to the IGBT based 3L converter, which moves content out to higher switching frequencies through the additional devices and complexity). The results of Figure 2.12 also indicate that the higher frequency spectral content of the SiC MOSFET-based converter will excite resonances in the 10MHz range, making it more difficult to control emissions below the limit line in this spectral range. Thus, the comparison between the work of Bolliat *et al.* and Singh *et al.* demonstrates both the challenge and opportunity that come with the use of WBG power semiconductors to realize power-dense, EMI AFE



(a) (b)

Figure 2.12: (a) Measured LISN voltages from optimal Class 3b EMI filter for TT IGBT-based AFE [9]. (b) Measured LISN voltages from optimal Class 3b EMI filter for 2L SiC MOSFET-based AFE [10]

solutions.

Another important observation is that trends in the literature shown reported work show Class 3 filters resulting in significantly higher power density than Class 2 filters. This result appears to be inadvertent rather than conclusive because research in the area of Class 2 filters, with only a few exceptions, is focused only on meeting PQ requirements. Also, Class 2 filter solutions correspond to lower switching frequency IGBT-based solutions, whereas the literature bears out the assumption that WBG-based solutions will require Class 3 filter solutions. Additionally, it may very well be that the requirement to reduce noise over a wide spectral range forces a discipline within the researchers that, of necessity, forces more tightly packaged and optimally designed solutions. At any rate, this observation bears highlights the need for further study.

As SiC MOSFET integration research surges, two clear trends can be observed. Firstly, the achievement of system-compatible design forces more integrative design approaches, *i.e.* CM and DM emissions, PQ and EMI compliance, self-compatibility, and external system compatibility must be considered simultaneously. Secondly, as has been pointed out, AFE PQ/EMI filter solutions trend exclusively towards the Class 3b filter structures. Considering the fact that filter inductors in these filters must support flux stresses over a wide range of frequencies, from very low to medium frequency, Class 3c filter structures are inevitable. In order to appreciate the evolution towards integrative solutions, consider the classical approach that has been commonly applied to IGBT-based converters in order to bring them into EMI standards compliance, shown in Figure 2.13. Considering the AFE-fed VFD, the classical approach would start with an AFE that has been designed to meet downstream motor controllability and ac grid compatibility through either a Class 1a or Class 2a DM filter. If the system is required to be qualified to an EMI standard that includes conducted EMI limits, such as CISPR 11, then an external Class 3b filter is added to its front-end ac interface. With this approach, the Class 3b EMI filter (which is the standard structure of commercially available EMI filter solutions) seems almost like an afterthought. In fact, it is common for manufacturers of VFDs to provide a product that serves a wide range of applications in domestic and international markets. In such a case, it may be beneficial for the VFD original equipment manufacturer (OEM) to provide EMI filtering as an option and “cost adder” only to solutions that require compliance. This approach makes sense, given that some EMI standards are more stringent than others. At the same time, it should be clear that, for SiC MOSFET-based solutions, such an approach may very well cancel out the power density benefits of WBG power semiconductors because of the redundancy of filters on the AFE grid interface. This consideration may motivate the VFD OEMs to consider WBG power semiconductors only as a means for improving efficiency, which may not be a sufficient motivation to justify the required engineering development costs and the increased costs of the devices themselves. Still, there is a promise that as integrative solutions to WBG-based power electronics become more common that costs will come down, and the WBG-based VFD may then present a more economical and widely applicable “plug-and-play” solution across the entire range of VFD applications.

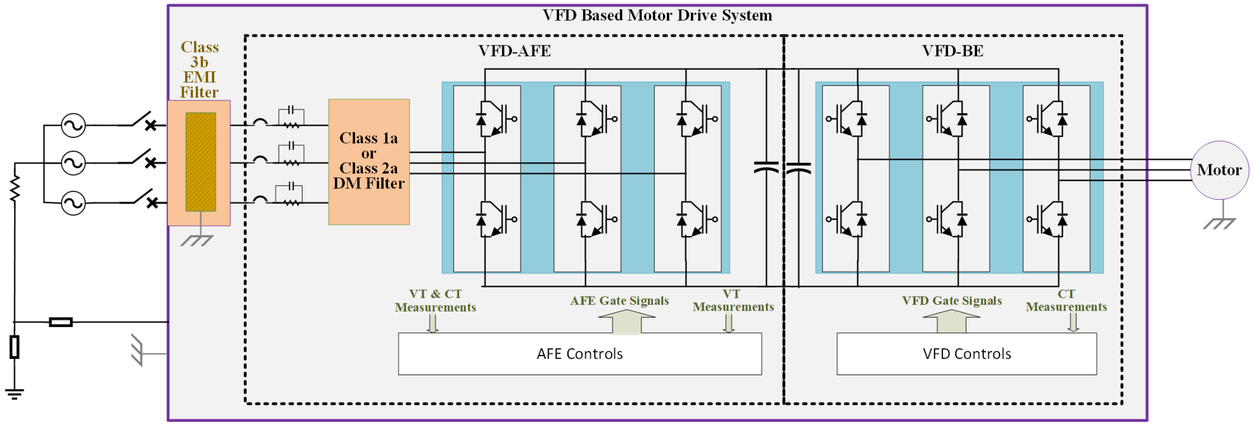


Figure 2.13: Motor Drive system with classical added on Class 3b EMI Filter

Class 1 Filters

The minimal functional circuit for a VSR-based VFD-AFE is shown in Figure 2.14. As has already been mentioned, the VSR requires a sufficiently stiff current, stiff voltage against which VFD-AFE power semiconductors can work in order to synthesize input nearly sinusoidal AC currents from the AC grid into a DC link voltage [15, 90–92]. Similarly, the downstream VSI-based VFD-BE requires a sufficiently stiff voltage against which its power semiconductors can work in order to synthesize DC link voltage into nearly sinusoidal AC currents supplied to the motor. The stiff AC-side currents are ensured through the addition of a sufficiently large boost inductor, $Lboost$, capable of supporting both fundamental components AC currents and switching frequency current (and its harmonics) due to noise voltage created at the power semiconductor terminals by modulated switching of power semiconductors against the stiff DC link voltage. The stiff DC link voltage is ensured through the addition of sufficiently large DC link capacitance to support both the current pulse train from the AFE power semiconductor network modulated switching synthesis of AC-gird side input currents, i_{C_i}, and the current pulses train from BE power semiconductor network modulated switching synthesis of AC-side output currents, i_{C_o}.

The boost inductor may be considered as purely DM inductance (1^{st} order filter) the AC-side AFE filter in Figure 2.14 comprises a Class 1a filter structure that.

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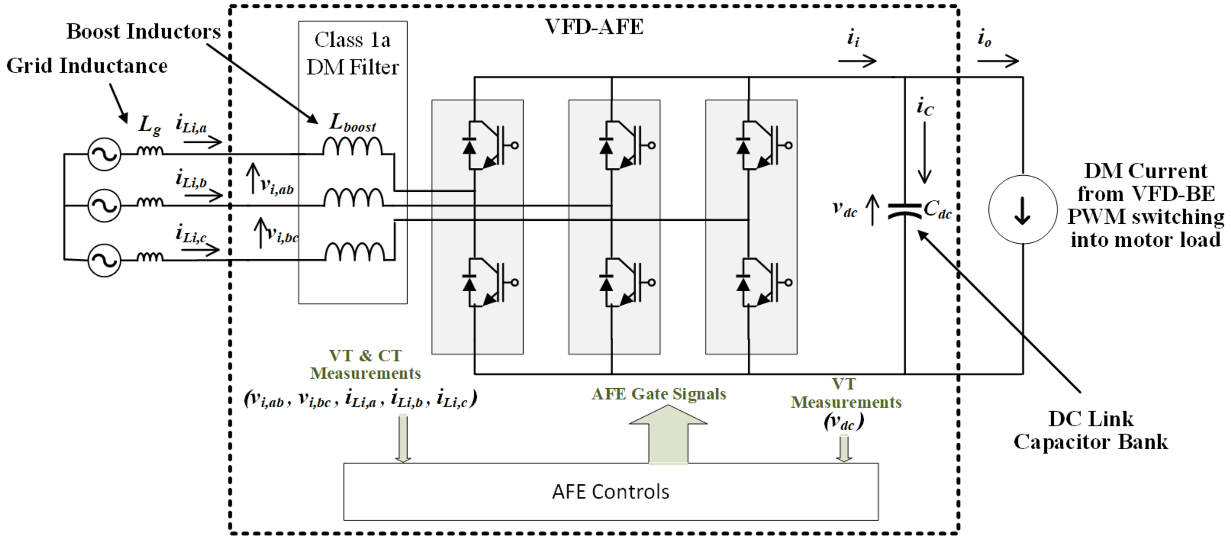

Figure 2.14: Fundamental VSR-based VFD-AFE

$$L_{boost} = L_{fi,1} \tag{2.13}$$

If the intent is to use only the use L_{boost} to meet PQ compliance, the design will result in using an extremely large inductor [93]. On the other hand, in some of the reported research on AFE filters, the filter design process assumes the presence of a boost inductor as part of the functional VSR circuit to which upstream filtering (including $L_{fi,1}$) is added [10, 17]. Clearly, this approach leads to a sub-optimal implementation compared to the more integrative approach suggested by 2.13. It should be noted that the aforementioned work by Singh *et al*. [10] assumes the presence of L_{boost} in the downstream AFE, which implies a lower achieved AFE filter power density in Table 2.5 when compared to the work by Boillat *et al*. [9].

The assurance of sufficiently stiff AC-side currents and DC link voltage corresponds in the most simplistic terms as constraining the peak-to-peak AC currently ripple, $\Delta i_{i,max}$, and DC link voltage ripple, Δv_{dc} to below target constraints, as specified by a set of ratings, operational parameters, and target constraints, shown notionally for a $188k$ VA (225 Hp) VFD, in Table 2.1. The quantities, $\Delta i_{i,max}$ and Δv_{dc} represent peak-to-peak current

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Table 2.1: System Ratings, Operational Parameters, and Target Constraints

Input Ratings		
Input power	188 kVA	S_i
Input line-to-line voltage	480 V	$v_{Li,rms}$
Input line current	226 A	$i_{Li,rms}$
Input frequency	60 Hz	f_i
Output Ratings		
Design or Dependent Variable	***Rating***	***Symbol***
Load power	169 kW	P_o
Output line-to-line voltage	480 V	$v_{Li,rms}$
Output line current	226 A	$i_{Lo,rms}$
Output frequency	60 Hz	f_o
Operational Parameters		
Operational Variable	***Value***	***Symbol***
DC link voltage	784 V	v_{dc}
Switching frequency	50 kHz	f_{sw}
AFE and VFD modulation index	0.79	$m_{a,i}$, $m_{a,o}$
Target Constraints		
Operational Constraint	***Limit***	***Symbol***
Input Power Factor	$\geq$ 0.92	$\cos\varphi_i$
Output Power Factor	$\geq$ 0.9	$\cos\varphi_o$
Efficiency	$>$ 98 %	η
Peak-to-peak DC link voltage ripple	$\leq$ 0.02 p.u.	Δv_{dc}
Peak-to-peak DC boost inductor current ripple	$\leq$ 0.1 p.u.	$\Delta i_{i,max}$

and voltage limits respectively. While this approach may establish a starting point for the selection of L_{boost} and C_{dc} values for component sizing, it in no way assures either optimal design or desired operational, PQ, and EMI performance. Therefore, the approach to determining, at least, the minimum required values for L_{boost} (or $L_{fi,1}$) and C_{dc} according to sets of optimizing objectives, such as those shown in Table 2.2, is a more complex process that requires further study and that can be informed by the state of the art found in the literature.

Minimum DC Link capacitance constraint The sizing of the DC link capacitor is an essential part of the system design and optimization of a WBG semiconductor-enabled

Table 2.2: Optimizing Objectives

Objective	**Symbol**	**Unit**
Power Density	ρ	kW/L
Specific Power	γ	kW/kg
Efficiency	η	%
Specific Cost	σ	kW/$
Lifetime	λ	hour

VFD. The exploration space considered for the sizing of the capacitor includes the semiconductors' switching frequencies (5 kHz to 200 kHz), the converter's control schemes, and the synchronization between the modulations of the front-end rectifier and the back-end inverter. The reference system rating is listed in Table 2.1. During the electrical design, sizing of the DC link capacitor includes the selections of both the capacitor's RMS current and capacitance. Closed-form expressions for the DC link capacitor's RMS current and capacitance are required to incorporate the DC link's physical size, weight, cost, and failure minimization (Table 2.2) into AFE/VFD multi-objective optimizations, which could lead to improvements in meeting system-level optimizing objectives. The closed-form expressions can also be incorporated into VPP and reveal the overall impacts versus drive frame size and drive performance requirements (Table 2.3). Moreover, a knowledge of these expressions will aid in AFE/VFD design decisions. For example, if the main objective of the system design is power density maximization, one approach would be optimizing the Pulse Width Modulation (PWM) control, DC link capacitor's physical size, and DM filter's physical size together through synchronization of the AFE and VFD. However, doing so control synchronization could fail to lead to potential losses in stability and degradation of EMI performance. These problems could be solved by using Model Predictive Control (MPC) [94–97]. The DC link capacitor's size reductions may be insignificant compared to potential EMI filter reduction using Model Predicted Control. Additionally, it is critical to take into consideration the wide range of load change in both

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Table 2.3: Design Choices and Trade-Offs

Objective	**Impact**	**Considerations**
Minimize DC link ripple	Increases DC link stiffness and reduce DM EMI	Increase DC link size/cost
Minimize DC link capacitance	Reduces link size/cost of link	Increase DM EMI
Actively minimize DC link ripple	Reduces link size/cost with less DM EMI impact	Control failure modes

the sizing of C_{dc} and L_{boost} [15].

$$i_{c_i,rms} = 0.65 \cdot i_{Li,rms} \tag{2.14}$$

$$i_{c_o,rms} = 0.65 \cdot i_{Lo,rms} \tag{2.15}$$

$$i_{c,rms} = \sqrt{i^2_{c_i,rms} + i^2_{c_o,rms}} \tag{2.16}$$

$$C_{dc} > \frac{P_{load}}{f_{sw} \cdot v_{dc} \cdot \Delta v_{dc}} \tag{2.17}$$

The DC link capacitor's capacitance requirement is independent of its RMS current. Using this "rule-of-thumb", (2.14) to (2.17), usually leads to over-sizing of the DC link capacitor. As a reference, using this approach will result in a design with $i_{c,rms} = 208$ A and $C_{dc} = 345$ μF for the reference system described in Table 2.1. Conventional implementations with electrolytic capacitors are driven by the RMS current. Electrolytic capacitors have a high capacitance density. This "rule-of-thumb" approach is less effective if higher reliability and lower loss capacitors are selected, such as metalized polypropylene capacitors, which have high RMS current capability but low capacitance density.

Publications [11–14, 98–120] dedicated to the derivation of a closed-form expression for DC link capacitor's RMS current can be sorted into three categories:

1. Calculation of DC link RMS current from the vector difference between the mean

value of input and output currents and RMS AFE/VFD switching currents assuming the instantaneous AFE input or VFD output line current is held fixed over the sampling interval.

2. Frequency domain methods that calculate the dominant DC link capacitor current centered at a specific switching harmonic or group of switching harmonic and sideband harmonics.

3. Piece-wise linear calculations of the time-domain capacitor current expressions derived for each PWM sampling sector from which RMS current is synthesized knowing the switch-state sequences.

The following part of this article will illustrate these three categories with materials from typical publications. A design result using each method is also presented to compare with the "rule-of-thumb" conventional method.

Method 1 This approach originated from [11], where a closed-form expression for the DC link capacitor's RMS current was presented. This expression is used by the same research group in design optimizations. One example with a back-to-back converter design is presented in [98].

In this approach, a closed-form expression for the RMS current feeding into the DC link (AFE side) or as a load on the DC link (VFD side) is first derived assuming Space Vector Modulation (SVM) (Figure 2.15a).

$$i_{Ci,rms} = i_{Li,rms}\sqrt{\frac{2\sqrt{3}}{\pi}m_{a,i}\,\left(\frac{1}{4}+\cos^2\varphi_i\right)} \tag{2.18}$$

where $i_{Li,rms}$ is the rated input line current. Note that, for the Class 1a filter, this is also the rated current in the boost inductor. For the Class 1b and Class 1c filters, this is approximately true because the impact of the line-to-ground capacitance in each phase is neglected.

The closed-form expression for the average DC output load current (VFD side) or DC input source current (AFE side) is derived as follows.

$$i_{i,avg} = \frac{3}{4} i_{Li,pk} \cdot m_{a.i} \cdot \cos\varphi_i \tag{2.19}$$

where

$$i_{Li,pk} = \sqrt{2} \cdot i_{Li,pk} \tag{2.20}$$

The RMS current from each side of the back-to-back converter can be derived from the vector subtraction: $i_{cx,rms} = \sqrt{i^2_{x,rms} - i^2_{x,avg}}$. The resulting closed-form expression for the DC link RMS due to either the AFE or the VFD is as follows

$$i_{Cx,rms} = i_{Lx,rms} \sqrt{2m_{a,x} \left[\frac{\sqrt{3}}{4} + \cos^2\varphi_x \cdot \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} m_{a,x} \right) \right]} \tag{2.21}$$

Applying (2.21) to the AFE side, assuming utilization of SVM, the AFE-side RMS current can be expressed as follows.

$$i_{i,rms} = i_{Li,rms} \sqrt{\frac{2\sqrt{3}}{\pi} m_{a,i} \left(\frac{1}{4} + \cos^2\varphi_i \right)} \tag{2.22}$$

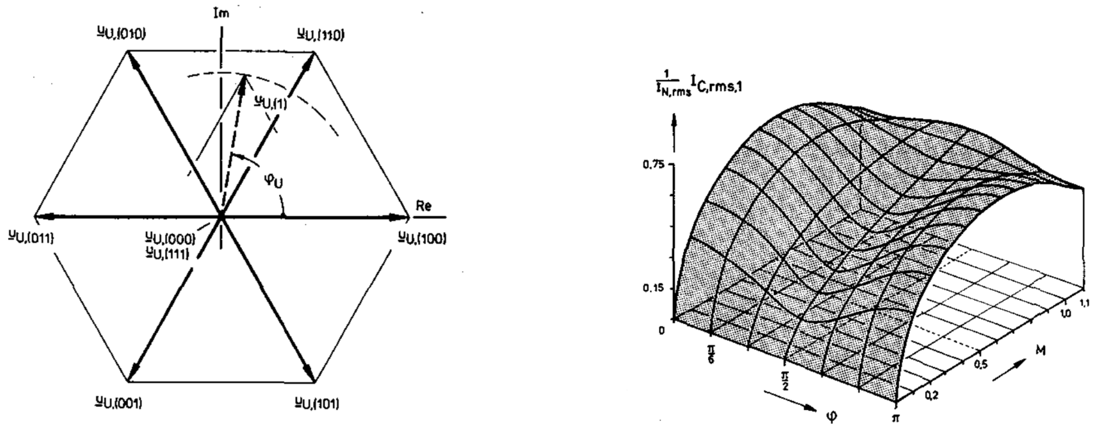
From the VFD-side, $i_{o,avg}$ is the averaged current due to the inverter, filter, and load flowing out of the DC link capacitor, whose expression is as follows.

$$i_{o,avg} = \frac{3}{4} i_{Lo,pk} \cdot m_{a,o} \cdot \cos\varphi_o \tag{2.23}$$

The DC link capacitor's current due to the AFE can be acquired with vector subtraction.

$$i_{c_i,rms} = \sqrt{i^2_{i,rms} - i^2_{o,avg}} \tag{2.24}$$

Repeat the same effort with the VFD side, and the DC link capacitor's current $i_{c_o,rms}$



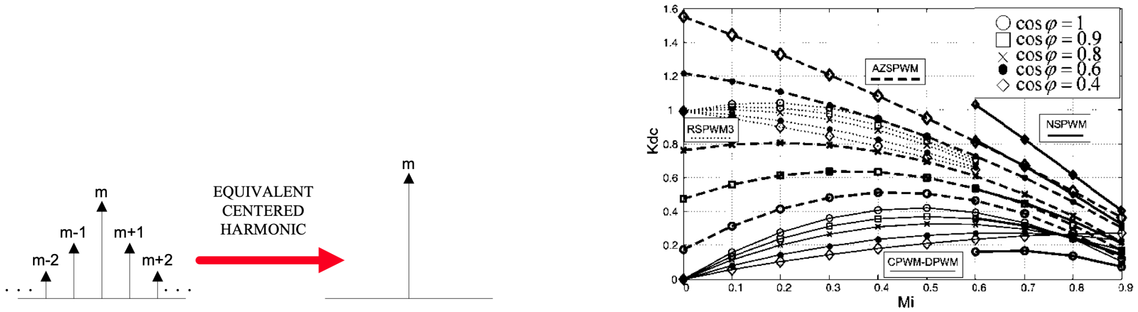
(a) Space vectors of the inverter output voltage assigned to the active inverter switching states and to the non-voltage forming switching states (000) and (111); furthermore shown: inverter output voltage reference value $\underline{u}_{U,(1)}$, which has to be formed in the average over a pulse half period of position φ_U; $\underline{u}_{U,(1)}$ is associated with the fundamentals of the pulse-width modulated inverter output phase voltages $u_{U,i}$, $i = R, S, T$.

(b) Dependency of the inverter-side contribution $I_{C,rms,1}$ to the global DC link capacitor current rms value $I_{C,rms}$ on the inverter modulation index M and on the phase displacement φ of the fundamentals of the inverter output phase voltages $u_{U,i}$ and the associated output phase currents $i_{N,i}$.

Figure 2.15: Figures from [11] describing Method 1

due to the VFD can be acquired. And final RMS current of the DC link capacitor can be derived by vector sum: $i_{c,rms} = \sqrt{i^2_{ci,rms} + i^2_{co,rms}}$. This method will result in $i_{c,rms} = 251$ A for the reference system rating.

Method 2 Method 2 is a frequency-domain-based approach. In [12] and [99], ripple characteristics of the frequency spectrum on AFE and VFD sides of the DC link capacitor are calculated using an equivalent centered harmonic approach (Figure 2.16a). From this analysis, the dominant frequency peak-to-peak current is determined. Note that the RMS current calculation neglects high order harmonics and fundamental frequency (6-pulse) harmonics, so it will likely be lower than the actual RMS current, depending on the DC link capacitance level and its electrostatic inductance (ESL) and electrostatic resistance (ESR).



(a) The equivalent centered harmonic representing the carrier frequency harmonic and its sidebands

(b) RMS ripple current characteristics, $K_{dc} = f(m_{a,x}, \cos\varphi_x)$ for various PWM methods

Figure 2.16: Figures from [12] describing Method 2

$$i_{c,rms} = \sqrt{K_{dc}} \cdot i_{L,rms} \tag{2.25}$$

K_{dc} is the DC link current coefficient defined as the ratio expressed as follows.

$$K_{dc} = \frac{I^2_{h,rms}}{I^2_{1,rms}} \tag{2.26}$$

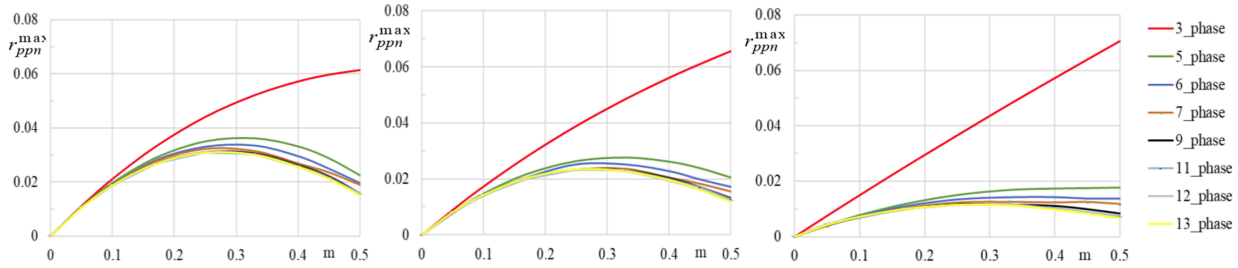
$$i_{c,pk-pk} = 2\sqrt{2} \cdot i_{c,rms} \tag{2.27}$$

The required capacitance is then calculated from the equivalency of the AC component of capacitor voltage to a specified minimum peak-to-peak voltage ripple requirement for both the switching frequency impacts.

$$C_{dc} > \frac{i_{c,pk-pk}}{2\pi f_{sw} \cdot \Delta v_{dc}} \tag{2.28}$$

If the DC link has a significant amount of low-frequency current ripple due to 6-pulse rectification then an alternative approach is used to calculate the DC link capacitance.

$$C_{dc} > \frac{P_o}{240 \cdot \Delta v_{dc} \cdot v_{L,rms} \cdot f_e} \tag{2.29}$$



(a) (b) (c)

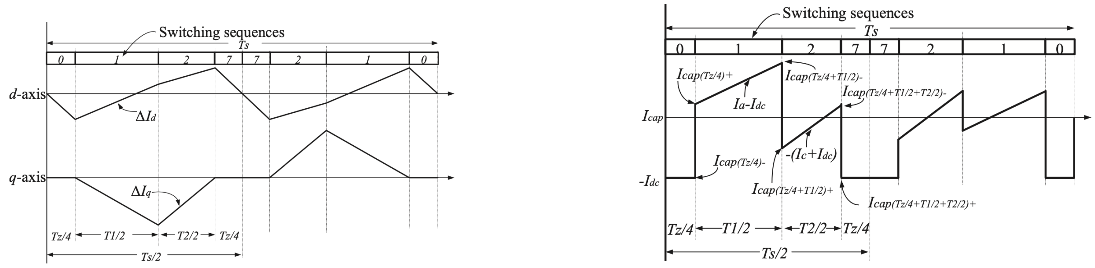
Figure 2.17: Maximum of peak-to-peak voltage ripple amplitude in multiphase VSIs, normalized per total output current, $r_{\text{ppn}}^{\text{max}}$, as a function of modulation index for output phase angles. (a) $\varphi = 20°$. (b) $\varphi = 45°$. (c) $\varphi = 70°$. [13]

This method concludes design results with $i_{c,rms} = 208$ A and $C_{dc} = 167$ µF for the reference system rating in Table 2.1.

$$\Delta v_{dc} = \frac{i_{x,avg}}{f_{sw} C_{dc}} r_{pp} \left(m_{a,x}, \varphi_x \right) \tag{2.30}$$

where $r_{pp} \left(m_{a,x}, \varphi_x \right)$ is obtained according to Figure 2.17. Here, no distinction is made between input or output modulation index, $m_{a,i}$ or $m_{a,o}$ nor between input or output power factor, $cos(\varphi_i)$ or $cos(\varphi_o)$, so it must be assumed that they are equal. Similarly, it is assumed that the switching frequency of the VFD-AFE and VFD-BE are identical.

A modified version of Method 2 is presented in [13] from which a pair of results is almost identical. This paper derives a generalized approach for the calculation of the minimum DC link capacitance requirement for n-phase induction motor DC-fed VFDs. The generalized results Extensive results provide plots of maximum peak-to-peak voltage ripple amplitude normalized to the output current functions of modulation index r_{ppn} and output power factor for 3-13 phase DC-fed VSI-based VFDs. These results are based upon analytical expressions for DC link capacitor peak-to-peak voltage ripple versus capacitance derived from PWM sub-intervals for SVM and SPWM methods. The modified factors can be seen in Figure 2.17 and modifies the voltage ripple with (2.30).



(a) The d-axis and q-axis ripple current components of the line current for the SVM. The modulation index $M = 0.85$ and reference space vector angle $\psi = 23°$.

(b) Capacitor current waveform in a switching cycle.

Figure 2.18: Figures from [14] describing Method 3

Method 3 In [14], the authors apply a simple analytical method to the calculation of DC link capacitor RMS current that applies to SVPWM and Discontinuous PWM (DPWM) methods (Figure 2.18). A time-domain approach is applied where to ripple current in the line current is used to synthesize the DC link current. Time domain methods superimpose the active and zero state vectors onto d- and q- axes from which capacitor current waveshapes are determined through the application of dwell time vectors in each sector and d-q line current ripple components of the line current. The mean-square values are calculated over each sampling interval of the switching sequences from SVPWM and DPWM. An RMS current expression is derived from each approach through vector addition of the mean-square amplitude values of each sampling interval over a $60°$ sector. For each k^{th} sampling interval, the expression as follows applies.

$$i_{c,rms_k} = \sqrt{F_{1k}^2 + F_{2k}^2 + F_{3k}^2 + F_{4k}^2} \tag{2.31}$$

Hence, the rms capacitor current over a $60°$ sector is derived as follows.

$$i_{c,rms} = \frac{3f_0}{f_{sw}} \sum_{k=1}^{\left(\frac{f_{sw}}{3f_0}\right)} i_{c,rms_k} \tag{2.32}$$

This closed-form expression is sufficient to extend over the fundamental line frequency period if SVPWM is applied. Piece-wise linear equations for the DC link capacitor for different Space Vector sequences are presented in this publication [14].

Comparison among three methods and the "rule-of-thumb" approach From the observations above, the RMS current calculation result varies from case to case. Method 1 produces the most conservative result, *i.e.*, higher RMS current was calculated for the reference case versus the "rule-of-thumb" method and Method 2. The results from Method 2 line up very closely with the "rule-of-thumb" reference. Methods 1 and 3 present completely analytical derivations to reach their closed-form expressions. While only a few published variations are purely analytical, most Method 2 examples present empirical data from which the weighting factors are derived to support the harmonic current calculations.

Regarding the closed-form expressions for the minimum DC link capacitance, the papers reviewed mostly aim at deriving the minimum DC link capacitance based on the maintenance of a maximum peak-to-peak voltage ripple. Method 2 yields a straightforward approach to the calculation of minimum DC link capacitance, knowing the dominant centered or equivalent DC link harmonic current. This method results in a much lower DC link capacitance requirement than methods derived from the maintenance of charge balance over the switching interval (a "textbook" approach to DC link capacitance determination). Modifications of method 2 by empirically derived weighing factors provide a margin for conservatism in the minimum DC link capacitance determination [13]. However, these much-less-conservative results from Method 2 are not advised by the authors of this review.

Synchronization of AFE with VFD switching may potentially yield significant reductions in both RMS current calculated from Method 3 based and the amount of DC link capacitor required to support full load swings on the motor side of the VFD [121].

This review proposes a method for DC link capacitance derivation based upon DM components of measured LISN voltages considering an industrial standard and trade-offs with the AFE and VFE DM filtering. The results are expected to provide a more sound approach to DC link capacitor optimization against DC link voltage ripple compared to the frequency-domain methods (Method 2) and potentially less conservative results than what would be yielded from Method 1 and Method 3. Dynamic stabilization requirements imposed upon the minimum DC link capacitance determination have yet to be considered but are essential for the next stage of research.

Boost Inductance Constraint A rudimentary approach to the determination of the minimum allowable boost inductance may start simply by sizing the inductance in order to comply with the maximum current ripple requirement, such as a per unit $\Delta i_{i,max}$, which can be used, along with rated RMS input current and operational DC link voltage to find a minimum value for L_{boost} using the following relationship

$$L_{boost} = \frac{v_{dc}}{4 \cdot \Delta i_{i,max} \cdot i_{Li,rms} \cdot f_{sw}} \tag{2.33}$$

This approach may lead to over-design if the value $\Delta i_{i,max}$ is selected arbitrarily. The value should at least have some basis, such as a maximum value at which switching ripple in the boost inductor affects power semiconductor junction temperature significantly. Even this approach is arbitrary and is really ineffective without a more analytical or accurate method for correlating the peak-to-peak ripple of the boost inductor current to power semiconductor device loss. For optimal designs, the impact of this ripple (and its frequency) on both the inductor sustainable hot spot temperature and the power semiconductor sustainable junction temperature must be considered.

Impact of AFE Controls on DC link Capacitance and Boost Inductances Work by Shi *et al*. [15] has explored the relationship between the required boost inductance and DC link capacitance values as influenced by the AFE controls. The most common AFE control

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approach is the cascaded PI controller shown in Figure 2.19 with an average model of the basic VSR-based VFD-AFE circuit of Figure 2.14. The approach taken by Shi *et al.* is to size the boost inductor so that harmonic performance levels are met and then to size the DC link capacitance taking into account controller considerations. With this approach, a per unit boost inductance, x_{Lmin}, is found according to such that a THD is constrained to a maximum level. This per-unit boost inductance can then be scaled to any power rating. The per unit boost inductance levels as a function of frequency index are shown in Figure 2.20, for three different THD levels. The frequency index is the ratio of the switching frequency to a base frequency, f which, in this case, would be the grid-side fundamental electrical frequency f_i, or

$$f = f_i \tag{2.34}$$

The boost inductance may be found in Figure 2.20 by

$$L_{boost,min} = x_{Lmin} \cdot L_b \tag{2.35}$$

where L_b is the base inductance for the system and is found using the system ratings (see Table 2.1 from the following equation

$$L_b = \frac{v_{Li,rms}}{\sqrt{3} \cdot 2\pi \cdot f_i \cdot i_{Li,rms}} \tag{2.36}$$

In order to find the minimum DC link capacitance for the minimum boost inductance Shi *et al.* propose performing a small signal stability analysis on the system over the range of heavy loads and light loads that the VFD system must support. The range of loads is quantified in terms of the equivalent resistance downstream of the AFE DC link as shown in Figure 2.19. The extreme points to be analyzed are

$$R_{o_{min}} = \frac{v_{dc}}{i_{o_{max},avg}} \tag{2.37}$$

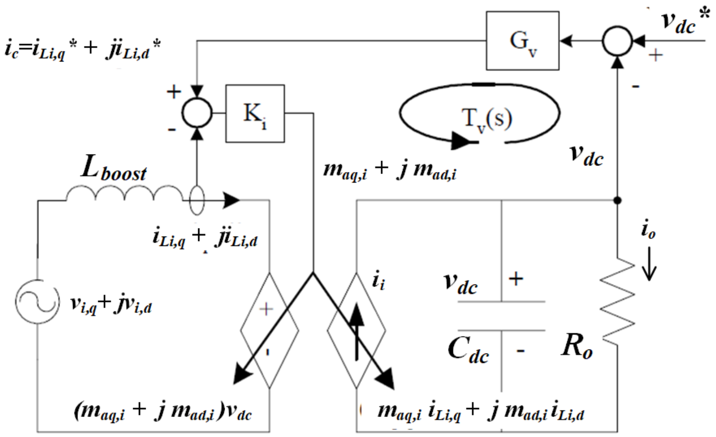

Figure 2.19: AFE Cascaded PI controller [15]

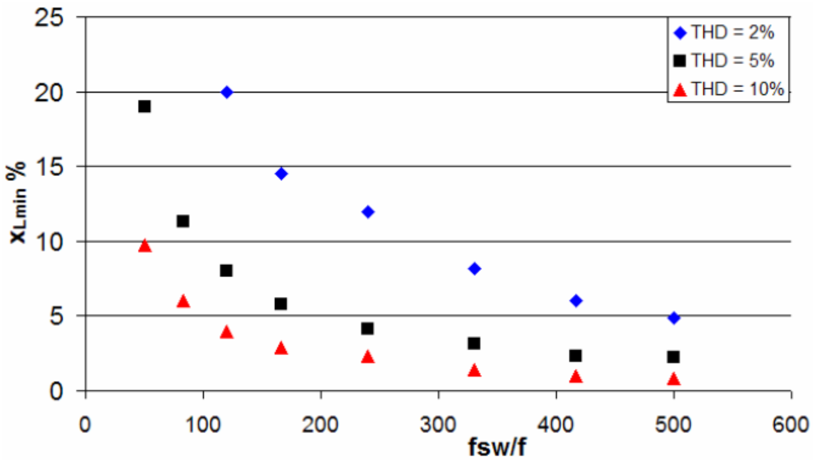

Figure 2.20: Minimun per unit boost inductance (x_{Lmin}) as a function of the frequency index ($\frac{f_{sw}}{f}$) for three different THD specifications [15]

$$R_{o_{max}} = \frac{v_{dc}}{i_{o_{min},avg}} \tag{2.38}$$

where $i_{o_{max},avg}$ and $i_{o_{max},avg}$ are the average current looking into the VFD-BE from the DC link perspective for the maximum and minimum load power scenarios defined by 2.23.

To perform this analysis, the transfer function for the complete system of Figure 2.19 is derived and a Bode plot phase gain analysis is performed, as shown in Figure 2.21. The transfer function is

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$$G_i = K_{pv} \cdot G_o \cdot \frac{(1 + \frac{\omega_{iz}}{s})}{(1 + \frac{s}{\omega_p})} \cdot \frac{(1 - \frac{s}{\omega_{zr}})}{(1 + \frac{s}{\omega_{pL}}) \cdot (1 + \frac{s}{\omega_{pI}})} \tag{2.39}$$

The process for selecting minimum C_{dc} is

1. Place the zero of the voltage PI regulator, ω_{iz}, at (or below) the first pole ω_{pL} of the current PI regulator from light load conditions ($R_o = R_{o_{max}}$)
2. Place a high-frequency roll off of the voltage PI regulator, ω_p, at (or greater than) the right-hand pole-zero location of the current PI regulator, ω_{zr}, found from light load conditions ($R_o = R_{o_{max}}$)
3. Place the gain crossover frequency at the middle of the roll-off window between the first pole ω_{pL} and the right-hand-plane zero ω_{zr}

These criteria yield the following outer voltage PI regulator gains

$$\begin{gathered} \omega_{iz} = \frac{2}{C_{dc} \cdot R_{o_{min}}} \\ \omega_p = \frac{m^2_{aq,i_{high}} \cdot R_{max}}{L_{boost}} \\ K_{pv} = \frac{2\sqrt{10}}{m_{aq,i_{high}} \cdot R_{o_{min}}} \end{gathered} \tag{2.40}$$

The paper by Shi *et al.* outlines the process for finding the inner current loop gains.

This entire approach has some limitations. First of all, the selection of L_{boost} is based upon THD. Meeting a THD limit of a given PQ standard does not guarantee that the IHD limits will be met at all frequencies defined by the standard. If a conservative approach is taken, say, limiting THD below the standard limit, then this may very well result in an over-designed boost inductance. Another limitation of this approach comes in dynamic response. Observing the crossover frequency point in Figure 2.21, it is at 16 Hz. If the greatest benefit of WBG power semiconductor integration into the VFD is to reduce the required AFE filter size by increasing the switching frequency, thereby reducing the value of first-stage DM inductance of the front-end filter (through an integrative filter design with $L_{fi,1} = L_{boost}$), this implies a need for the faster response of the DC link voltage to compensate for the reduced stiffness of the ac-side input currents. This observation is consistent with the fact that the cascaded PI controller is inherently sluggish and, as a result, the full performance benefits to be gained by the fast speed of response of the power semiconductors will be limited by a constraint of the minimum L_{boost} and minimum C_{dc} required to stabilize the controller. One way to address this limitation is to move away from the cascade PI controller to a form of control that eliminates the inner loop. One way to accomplish this is through MPC methods [94–97].

In conclusion, enabling lower limits on L_{boost} (or $L_{fi,1}$) and C_{dc}, the multi-objective optimization of any one of the filter classes (Class 1, 2 or 3) starts with a determination of these lower limits taking into account the switching frequency, PWM method, DC link controls, and grid synchronization. The process for determining the lower limit values of $L_{fi,1}$ and C_{dc} is shown in Figure 2.22,

Class 1a Filter Design Generally, Class 1a filtering is an ineffective approach to meeting both PQ and EMI requirements. There are some VFD OEMs who take this approach to make a VFD system PQ compliant, as shown in Figure 2.23 or Figure 2.24. A PQ-compliant system must also limit the inrush current at start-up and relies upon grid synchronization. VFD OEM vendors who take the approach of Class 1a filtering only usually end up with such a large combination of L_{boost} and/or $L_{fi,1}$ inductance that the inductor(s) limit the inrush at start-up and unique methods for grid synchronization can be implemented without the cost of input voltage (*i.e.* $v_{i,ab}$ and $v_{i,bc}$) sensing. Such an approach may lead to a lower-cost solution but at the expense of high volume (or low power density). If the Class 1a filtering approach is selected, then the process for determining

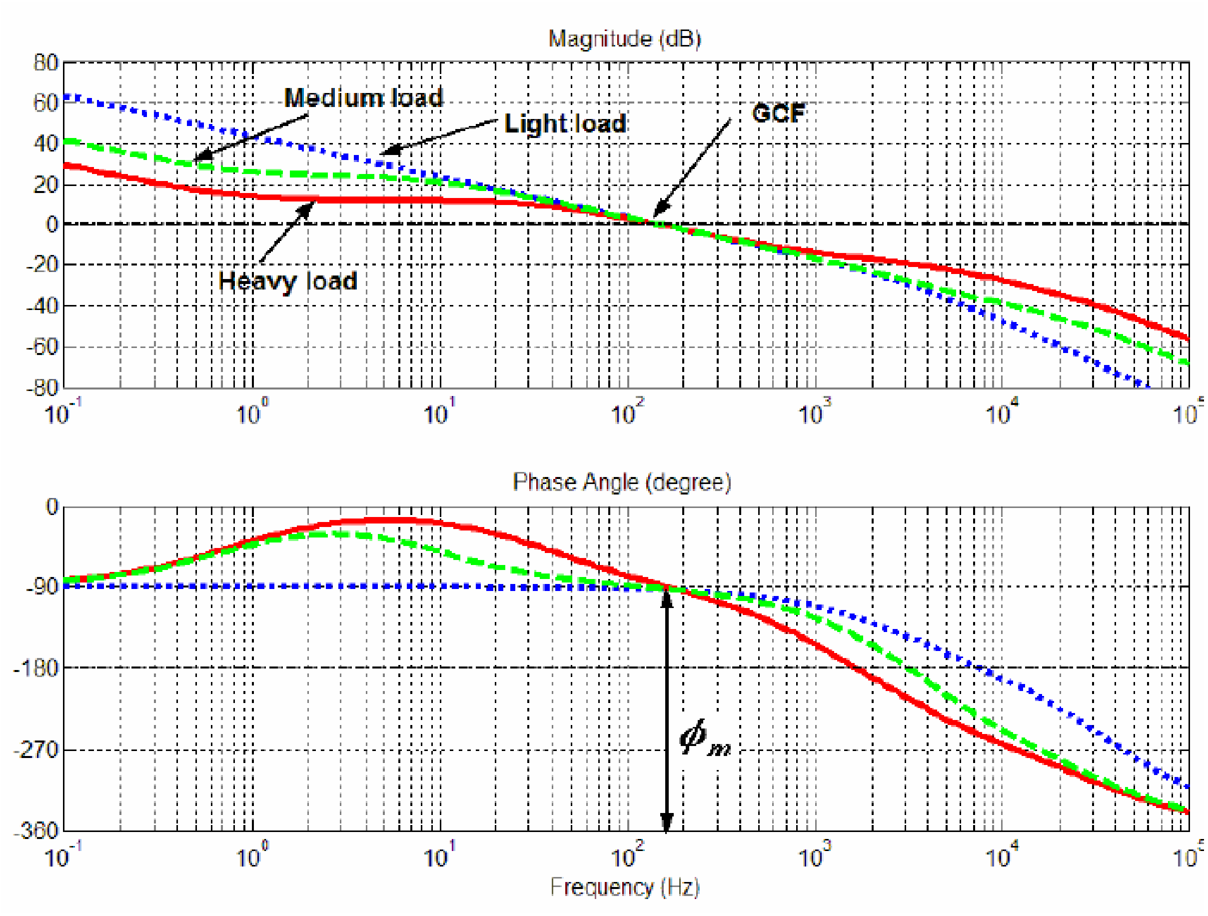

Figure 2.21: Bode plots for phase gain margin stability analysis of the system of Figure 2.19 [15]

minimum C_{dc} and minimum L_{boost} (or minimum $L_{fi,i}$ for the integrative solution of Figure 2.24) establishes the minimum constraint for these component values and a starting point for determining the amount of additional DM inductance needed to bring the input current IHD and THD (measured at the point of common coupling) below prescribed limits.

The increased switching frequency made possible by WBG power semiconductors may enable viable EMI-compliant Class 1a solutions however, as the harmonic spectrum is moved into the HF to MF range CM emissions will dominate, in which case a Class 1b filter is a better solution.

Class 1b Filter Design The reason for the choice if Class 1b, where EMI compliance is important. Referring to Figure 2.34a and 2.34b, the Class 1b filter provides -40 dB/decade of CM noise attention, while the Class 1a filter only provides -20 dB/decade, because of the inclusion of line-to-ground capacitors, C_{ei} along with common mode inductance according to (2.67).

Class 1c Filter Design The reason for a Class 1a, Class 2c or Class 3c filter is the same, and will be addressed in conjunction with the discussion of Class 3 filters.

Class 2 Filters

The largest number of publications on AFE filtering fall under the category of Class 2 filtering. Historically, the Class 2 filter was introduced as the means to PQ compliance for VSR-based AFEs for a wide range of applications, not limited to VFDs. The literature in this area has surged with the advent of a utility grid-connected renewable energy system. The bulk of the literature focuses on the Class 2a filter but there is some notable work that has been reported regarding the Class 2b filter.

Class 2a Filter Design The DM Class 2a filter is the most common filter type found in the literature [16, 74, 92, 93, 122–132]. It is the simple LCL configuration with damping resistance in the capacitive branch as shown in Figure 2.25a, which has removed the EMI filter components from the simplified LN equivalent circuit representation of Figure 2.40. The components in Figure 2.25a correspond to those in Figure 2.40 with

$$C'_{fi} = 3 \cdot C_{fi} \tag{2.41}$$

and

$$R'_{fi} = \frac{R_{di}}{3} \tag{2.42}$$

One of the earliest mentions of this type of filter, with the AFE, combines second-order LCL filtering with active damping in the inner loop controls as described by Blasko *et al.* [122]. Blasko *et al.* implement the fully controlled AFE with a cascaded PI (2.19) and utilize active damping in combination with the cascaded PI in order electronically mimic the behavior of R_{di}, enabling a simple LCL filter without the losses associated with the damping resistor. The main objective for the Class 2a filter is to achieve switching frequency and switching harmonic attenuation at -40dB/decade. However, this 2^{nd} order response is not easily achieved in AFE application due to several considerations enumerated as follows:

1. The AFE and its filter connect to a grid installation having an unknown grid inductance, L_g, as shown in Figure 2.24
2. Resonance will occur between grid inductance, L_g, converter-side inductance of L_{fi} and C_{fi}
3. Since the power semiconductor voltage breakdown limits the margin between the fundamental peak voltage active rectifier ac-side voltages and the dc link voltage, $L_{fi,1}$ must have sufficient inductance to enable voltage control across $L_{fi,1}$
4. $L_{fi,1}$ inductance should be kept low enough to ensure that under nominally rated conditions and step-on transients of the VFD motor, the associated AFE converter-side voltage drop is not reflected in the VFD-BE performance
5. Since the principal PQ objective of the AFE is to achieve nearly unity input power factor, the value of C'_{f1} should be limited to keep leading power factor reactive current on the grid-side to a minimum

Of these considerations, (1.) and (2.) dictate the need for a grid-side inductor, $L_{fi,2}$ of sufficient inductance to ensure that the L_g associated with any VFD installation does not

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cause ELF to VLF resonant frequency content in the input spectrum to exceed PQ IHD limits. The resonant frequency is given by the following expression.

$$f_o = \frac{1}{2\pi}\sqrt{\frac{L_{fi,1} + L_{fi,2} + L_g}{L_{fi,1} \cdot (L_{fi,2+L_g}) \cdot C_{fi}}} \tag{2.43}$$

Assuming the appropriate choice of L_{fi} consideration (2.) dictates the need for sufficient and optimal resonant damping resistance of R'_{di} while simultaneously keeping the losses associated with R_{di} low enough to meet minimum efficiency objectives of the VFD system (considering all loss components). If the values of $L_{fi,1}$, $L_{fi,2}$ and C'_{fi} result in a resonant frequency that is within the controllable range of the AFE controller, then active damping may be utilized to eliminate the losses associated with R'_{di}. Resonant currents between Consideration $L_{fi,1}$, $L_{fi,2}$ and C'_{di} will certainly be excited by the range of harmonic voltages that are applied from the converter-side through $L_{fi,1}$. At the same time, transient disturbances on the grid-side at the point of common coupling or transients from the motor side of the VFD will excite resonances through $L_{fi,2}$ or a combination of $L_{fi,1}$ and $L_{fi,2}$. Active damping is possible if the sampling frequency, f_s, and resultant closed-loop bandwidth frequency, f_b of the digital controller relate to the switching frequency f_{sw} and resonant frequency f_o as follows [131]

$$f_b < f_o < f_{sw} < f_s \tag{2.44}$$

where the bandwidth relates approximately to the sampling frequency as follows

$$f_b \approx \frac{f_s}{6\pi} \tag{2.45}$$

Defining the ratio of switching frequency to resonant frequency as $k = {}^{f_{sw}}/_{f_o}$, [125, 126] and [132] provide guidance according to Table 2.4.

According to Table 2.4, k is dependent upon f_s as it relates to the switching frequency f_{sw}. Single update PWM samples the inverter-side current feedback utilized for active

Table 2.4: Comparison of value $'k'$ under various design requirements

Minimum k based on single update PWM	2
Mean value of k in double update PWM	3.07
Mean value of k in single update PWM	4.34
Capacitor active damping (maximum damping) [128,133]	3.12
Lead-lag network (maximum damping) [134]	3.2-3.4
Critical resonance frequency single update PWM	6
Critical resonance frequency double update PWM	3

damping at a rate of $f_s = f_{sw}$. This is a minimal approach, given sensitivities to noise in the current sensors and the need to carefully synchronize sampling with gating of the AFE power semiconductors, the realization of the desired performance is problematic. Double update PWM is the most widely applied approach in power converters requiring current feedback control and samples the inverter-side current feedback at $f_s = 2 \cdot f_{sw}$. Performance can be improved by over-sampling currents at rates that are at factors of two times the double update PWM and, even more so, if sampling and average techniques are applied. The active damping can be improved for lower k if it is possible to directly sense current in the capacitor branches [128,133]. However, this approach is not recommended because of the necessary introduction of parasitic inductance in the capacitor branches, as will be explained in the discussion on Class 1b filters. The same effect can be accomplished without penalty in PQ/EMI performance by sensing both inverter- and grid-side currents in each phase and using the difference between them to synthesize the capacitor branch currents. The use of a lead-lag network to achieve active damping tuning will result in the best active resonance damping performance given the trade-off of current feedback noise against maximizing the gain of resonance attenuation [134].

Because of the computational hardware requirements and associated cost and control complexity of active damping, passive damping is more commonly applied to the Class 2 AFE filter. As the switching frequency can be increased to reduce the size of AFE passive filter components, the effect is to increase f_o of 2.43 to a level where digital sampled feed-

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back controls with rates that are achievable in the most cost-effective control hardware implementations prohibit active damping. In fact, if the full benefit of WBG power semiconductors in reducing AFE filter size is to be achieved, it will be necessary to revisit the common paradigm of the ubiquitous Digital Signal Processor (DSP)-based implementation of a digital closed-loop controller for the grid-interfacing converter. Alternatively, a movement towards FPGA-based closed-loop controls that enable the high f_b closed-loop controls, approach performance of analog feedback controls, may be necessary. In this case, the cost of the control hardware should be carefully considered. A practical tradeoff of the reasonable cost of controls versus minimization AFE filter size may very well result in the compromise that utilizes passive damping. If passive damping is applied, the following relationship for R'_{di} results in the maximum damping:

$$R'_{di} = \frac{1}{3 \cdot \omega_o \cdot C_{fi}} \tag{2.46}$$

where $\omega_o = 2\pi f_o$

It is important to note that, considering (2.43) and (2.46), the actual value for R_{di} that critically damps out resonance is dependent upon the grid inductance L_g. This consideration is a principal driver for the selection of $L_{fi,2}$ that is acknowledged in all of the literature and that has led to the general rule of thumb of selection of the $L_{fi,2}$, as a percentage according to the installation feed impedance [74,127,135]. The standard approach of selecting $L_{fi,2}$ between 3% and 6% and has the effect of making $L_{fi,2}$ in the same order as the feed inductance L_g. Unfortunately, this approach does not eliminate the sensitivity to L_g and, in order to account for the connection of the VFD into a weak grid, it is almost always necessary to combine passive damping together with active damping with, in many cases, unpredictable results [133]. If, on the other hand, critical or over-damping is ensured, then second-order response can be assured, and the remaining parameters, $L_{fi,1}$ and C_{fi}, can be considered as design space variables with constraints in order to satisfy the PQ IHD requirement of

$$I_h \leq I_{h,limit,dB}(f_h)\,\forall h \tag{2.47}$$

according to a given standard. A consideration of the standard limits of 2.47 in a required attenuation as a function of harmonic frequency, $A^*(f_h)$ can be found. Processes for determination of the attenuation function for the Class 2a filter are well-described in [93, 131] and [16]. This approach is more effectively applied when a known or assumed value for L_g is included in the ratio between inductances on the grid and converter sides of C_{fi},

$$k_L = \frac{L_g + L_{fi,2}}{L_{fi,1}} \tag{2.48}$$

where k_L iis more commonly referred to as r in the literature.

A rigorous approach, proposed by Cittanti *et al.* [16] is to optimize k_L so that the filter attenuation for a given total amount of inductance,

$$L_{tot} = L_{fi,1} + L_{fi,2} + L_g \tag{2.49}$$

is maximized. The asymptotic expression for filter admittance, which corresponds to the inverse of $A(s)$ (where $s = j\omega$), is derived for both the undamped and damped cases as

$$Y_f(s) \overset{s \to \infty}{=} \begin{cases} \frac{1}{s^3 C_{fi} L_{tot}^2} \cdot \frac{(1+k_L)^2}{k_L} & \text{undamped } (R_{di} = 0) \\ \frac{R_{di}}{s^2 L_{tot}^2} \cdot \frac{(1+k_L)^2}{k_L} & \text{undamped } (R_{di} \neq 0) \end{cases} \tag{2.50}$$

It was shown in Cittanti *et al.* [16] that maximum filter attenuation is obtained for $k_L = 1$, as shown in Figure 2.26. This result suggests that $k_L = 1$ will minimize the product between the filter capacitance, C_{fi} and the total filter inductance (including grid inductance), L_{tot}. It is suggested in Cittanti *et al.* that this condition, which minimizes the required capacitance for a given total inductance, and vice-versa, is a necessary condition for overall LCL filter size minimization. Additional studies on the relationship between

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k_L and the attainment of LCL filter optimization objectives also suggest that, for the Class 2a filter, $k_L = 1$ is a beneficial choice [93, 124, 132]. It should be noted, however, that the paradigm for the Class 2a filter is the assurance of PQ compliance only with the general application to IGBT-based AFEs and the relative reduction in sensitivity of the L_{tot} to variations in L_g when $k_L > 1$ [123]. However, it is pointed out in Cittanti *et al.* that reliance upon these criteria alone and subsequent use of fixed damping resistance per (2.46) (without the use of active damping to accommodate scenarios where L_{tot} is sensitive to L_g) limits the filter design space and leads to sub-optimal results. Furthermore, if the introduction of WBG power semiconductors is utilized to minimize both CM and DM filter size against both PQ and EMI requirements, maintenance of a fixed R_{di} as L_{tot} is reduced overall with increasing f_{sw} may significantly sub-optimize the results of the filter design process. Hence, active damping should always be considered within the design space [133].

The focus of the literature on Class 2a filtering is on either the determination of the $L_{fi,1}$, $L_{fi,2}$ and C'_{di} through closed form expressions or simplified processes [130, 131] or through optimal or constrained selection processes of $L_{fi,1}$, $L_{fi,2}$ and C'_{fi} to minimize filter size, [16], losses, [126], cost [93, 123] or against multiple objectives [74, 92, 132, 133]. The inevitable result of the determination of $A^* f_h$ that meets the criteria of (2.47) while assuring the condition(s) described by (2.50) is a broad choice of $L_{fi,1}$ and C'_{fi} that result in PQ standard compliance. This point is further driven home by Nagel, and De Doncker [136], regardless of filter order. The point is that there are many combinations of $L_{fi,1}$ and C'_{fi} when it is considered that a large number of design exploration variables exist for any given implementation of $L_{fi,1}$ and C'_{fi}, thousands of combinations of design space variables associated with the physical realization of $L_{fi,1}$ and C_{fi} (including an infinite resolution on the range of the $L_{fi,1}$ and C'_{fi} values themselves) will satisfy the minimum attenuation needed to comply with a given PQ standard, it follows that, as a minimum, on or more objectives, such is an as minimal cost, size or losses, is necessary to the meaningful realization of the LCL filter, it is clear that the design process for the LCL filter that will truly demonstrate the conclusive value of, say, a given choice of power semiconductors (*i.e.* WBG) or for a given power electronic circuit topology [92], requires multi-disciplinary, multi-objective evolutionary optimization.

Additionally, one consideration that is noticeably absent in the literature is the impact of the VFD power rating, with only a few exceptions [16,123], is the impact of VFD power rating on the optimal selection LCL values for that power level. As an example, the power density of the AFE filter for lower power drives (*i.e.* $< 40kW$) goes up as the L_{tot} increases and C_{fi} reduces. For high power drives (*i.e.* $> 40kW$) power density goes up as L_{tot} decreases and C_{fi} increases. It follows that there will necessarily be constraints of the maximum and minimum $L_{fi,1}$ and C_{fi}. Even when this consideration is addressed in the literature, the detailed design choices associated with, say, $L_{fi,1}$ are not covered in sufficient detail to yield scaling laws. At best, the literature on Class 1a and 2a filters, synthesized as a whole, provides sets of constraints on the $L_{fi,1}$ and C'_{fi} and relationships from which $L_{fi,2}$ and R_{di} can be determined. Cittanti *et al.* [16] provides probably the best synthesis of these takeaways from the literature. One thing that Cittanti *et al.* attempt to do is to account for the passive or active damping in the optimal selection criteria and the impact of power rating through a consideration of inductor and capacitor energy densities that are $\alpha\ LI^2$ and $\alpha\ CV^2$ in the design and constraint equations. Combining (2.46) and (2.50, into the calculation of $A^*(f_h)$ needed to comply the IHD design constraint of (2.47) through the following expression

$$A(f_h) = \frac{1}{|Y_{f,s\to\infty}(j2\pi f_h)|} = \frac{\pi^2 f_h^2 L_{tot}^2}{R_{di}}\ f_h \gg f_o \tag{2.51}$$

The required harmonic attenuation in the dB scale can be expressed as

$$A^*(f_h) = V_{h,dB}(f_h) - I_{h,limit,dB}(f_h) + \text{margin}_{dB} \tag{2.52}$$

where the harmonic frequency, f_h, which requires the largest filtering effort to stay below $I_{h,limit,dB}(f_h)$ is $f_h = f_d$, where f_d is the design frequency. If the filter incorporates passive damping (as indicated by Figure 2.25a), then filter attenuation increases with a 40 dB/decade rate, and the design frequency value corresponding to the worst-case filter design condition is

$$f_d = f_h \Longleftrightarrow max[A^*(f_h) - 40\ log_{10}(f_h)] \tag{2.53}$$

The following is a synopsis of the design constraints for the Class 2a AFE filter:

- **Minimum resonant frequency:** $f_o \geq f_{o_{min}}$ constrains $C'_{fi_{max}}$ to

$$C'_{fi} \leq \frac{1}{\pi^2 f_{o,min}^2 L_{tot}} \tag{2.54}$$

- **Maximum resonant frequency:** $f_o \leq f_{o_{max}}$ constrains $C'_{fi_{min}}$ to

$$C'_{fi} \geq \frac{1}{\pi^2 f_{o,min}^2 L_{tot}} \tag{2.55}$$

- **Maximum no-load reactive power:** $Q_i le Q_{i_{max}}$ when $P_i = 0$ constrains $C'_{fi_{max}}$ to

$$C'_{fi} \leq \frac{Q_{i_{max}}}{3\pi f_i \sqrt{2}\ v_{Li,rms_{min}}} \tag{2.56}$$

  where $v_{Li,rms_{min}}$ is the minimum continuous grid-side line-to-line voltage allowable by the installation interface standard.

- **Minimum converter-side inductance:** $L_{fi,1_{min}}$ is constrained by the process described in Figure 2.22 and

$$L_{fi,1} \geq 2\frac{\Delta\psi_{fi,1}}{\Delta i_{i,max}\sqrt{2}\ i_{Li,rms}} \tag{2.57}$$

where $\Delta\psi_{fi,1}$ is the maximum allowable peak-to-peak flux in $L_{fi,1}$ according to inductor loss and heat extraction constraints

- **Maximum total inductance:** $L_{tot_{max}}$ is constrained by

$$L_{tot} \leq \frac{\sqrt{\frac{v_{dc_{min}}^2}{3}} - \sqrt{2}\, v_{Li,rms_{max}}}{2\pi f_i \sqrt{2}\, i_{Li,rms}} \tag{2.58}$$

  where $v_{Li,rms_{max}}$ is the maximum continuous grid-side line-to-line voltage allowable by the installation interface standard, assuming converter PWM allows for a maximum modulation index of $m_{a,i_{max}} = 1.15$.

- **Minimum power factor:** $\cos\varphi \geq \cos\varphi_{min}$ when $P_i = P_{i_{min}}$ constrains $C_{fi_{max}}$ to

$$C'_{fi} \leq L_{tot} \frac{I_{min^2}}{\sqrt{2}\, v_{Li,rms_{min}}^2} + \frac{P_{i_{min}}}{3\pi f_i \sqrt{2}\, v_{Li,rms_{min}}^2} \cdot \frac{\sqrt{1 - \cos\varphi_{min}^2}}{\cos\varphi_{min}} \tag{2.59}$$

Class 2b Filter Design The DM Class 2b filter is the LCCL filter configuration found in the literature [124, 135, 137] and shown in Figure 2.25b. This approach is generally taken when both PQ and EMI requirements must be met, although this point is not brought out clearly in the literature. As the requirement for controlling I_h below limits as the frequency goes into the MF spectral range, the resonance associated with ESL of C'_{fi} and its interconnecting inductance is excited, leading to conducted EMI outages. The criticality of managing the C'_{fi} branch parasitic interconnection inductance prohibits the connection of R_{di} in series with $C_{fi'}$, as is the case with the Class 2a LCL filter (Figure 2.25a). These resonances can be avoided by connecting C_{fi} directly across the terminals and carefully managing the parasitic connection inductance. Low ESL capacitors are also required. The Class 2a filter results from the need to control LF resonances between $L_{fi,1}$, $L_{fi,2}$ and C_{fi} through the addition of a parallel series R'_{di}/C'_{di} branch. It should be noted that the same requirement to control the excitation of resonances in the MF range drives the physical realization of the Class 2a filter using delta-connected C_{di} capacitor branches as shown in Figure 2.37. Comparing Figure 2.37 with Figure 2.25b,

$$C'_{di} = 3 \cdot C_{di} \tag{2.60}$$

According to [135, 137] the optimal value for C_{di} is

$$C_{di} = a_C \cdot C_{fi} \tag{2.61}$$

where the optimal value for a_C is a trade-off between the effective damping and power loss in the shunt passive R_{di}/C_{di} branch. A general rule of thumb that is commonly applied is to set

According to [135, 137] the optimal value for C_{di} is

$$C_{di} \geq 3C_{fi} \tag{2.62}$$

The damping resistor R_{di} is

$$R_{di} = 3R'_{di} \tag{2.63}$$

where R_{di} comes from (2.46).

Class 2c Filter Design The Class 2c filter is not covered in the literature but is often the inadvertent result of the addition of the Class 2a to the AFE with boost inductor (Figure 2.23) in an attempt to meet PQ and EMI requirements simultaneously. Here, the intent of the sub-class 'c' filter is revealed. The boost inductor may absorb the LF stresses associated with f_sw and its lower order harmonics, while parasitic elements of the boost inductor dominate for spectral content in the MF range. Class 2c offers the opportunity to shape the frequency-dependent attenuation characteristics of the combined converter-side inductance.

Class 3 Filters

The effort to tackle both the EMI challenge and PQ within an integrated filtering structure tends to result in oversized DM inductors and capacitors. With the popularity growth of WBG utilization, more designs on deligated EMI filters have been published. Since only high-frequency DM and CM noises are considered, filter box volumes are allowed to be smaller due to the inductance and capacitance selections. Moreover, due to the nature of the EMI spectral envelope, multiple LC stages can be implemented to achieve volumetric optimization. In the previous subclass 'c' examples, the un-suppressed EMI components in the higher frequency range can be attenuated by adding smaller inductances in series with existing $L_{fi,1}$ and $L_{ei,1}$. But this only compensates for the attenuation drop due to the parasitics of inductors without providing significantly more attenuation. In scenarios where high-frequency resonances occur due to converter parasitics, a higher-order filter would be necessary to avoid filter over-design.

As demonstrated in [10, 17, 138], a multi-stage DM EMI filter can be realized by using n_f LC filter stages with the same inductance and capacitor values. The boost inductors are selected before and not considered in this filter design method. The required filter attenuation over a target frequency range defined by the target EMC standard is acquired from signal processing with a simulated converter voltage waveform. The signal processing emulates EMI measurement results of an un-filtered converter connected to an EMI receiver via the required LISNs and power source. When necessary, the quasi-peak (QP) detector and an EMI level margin can be included in the simulation to accommodate the standard requirement and tolerances. The method provided in [17] also further simplifies the simulation process by first summing all the high-frequency EMI spectral

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contents and placing it on the switching frequency as one component (Figure 2.27). The EMI predictions on the design frequency are, in turn, calculated based on this noise sum and the overall spectral EMI envelope (Figure 2.27c). This simplified method can serve as a guideline for the EMI filter design of the XPC project. However, more details such as high-frequency filter parasitics, CM noise filtering, and other standard demanded restrictions need to be considered.

Class 3a Filter Design The Class 3a filter (Figure 2.42) is not found in the literature, but it is an approach that could be taken to bring the VFD into PQ compliance with a higher order filter while managing the resonances of each stage in a high order filter with tuned passive damping branches.

Class 3b Filter Design The Class 3b filter is the most commonly found AFE filter design where DM and CM attenuation is required in order to meet PQ and EMI limits simultaneously as WBG power semiconductors provide the opportunity to reduce filter volume through the increase in f_{sw} into the high end of the LF range (*i.e.* from 40kHz to 200kHz). The result is that spectral content associated with the EMI standard will drive the optimization of the AFE filter design. Furthermore, filter design will require multi-objective evolutionary methods in order to discover the switching frequency at further increases in f_sw, resulting in a larger overall filter volume or the inability to extract the heat from the converter-side inductor due to high-frequency losses.

Example 1 A symmetric two-stage DM filter design for a 3-phase boost PFC converter is illustrated in [10]. Similarly, with [17], the boost inductors are not considered a part of the filter. The design constraints considered for this filter are EMI conducted emission standard (aviation industrial, DO-160, 150 kHz to 30 MHz), power factor limits, and lower frequency harmonic control. Because this design only focuses on DM, filter performance is only evaluated for frequencies up to 5 MHz. The two-stage filter is also optimized for minimal cost, and the cost function is chosen as the average stored energy in the EMI filter defined in (2.2.2).

$$E_{DM} = k_l \left(L_1 + L_2\right) I_{ph}^2 + k_c \left(C_1 + C_2\right) V_{ph}^2 \tag{2.64}$$

The inductor damping resistors and boost inductors are selected before the EMI filter design. Starting with a set of all acceptable filter LC's, the optimization comb through these options via the three constraints sequentially. The EMI conducted emission attenuation is sufficed first, the power factor limits second, and the sub-switching-frequency damping last. The EMI attenuation requirement is acquired by a single-line DM circuit simulation where the PWM converter is simulated as a stiff voltage source (Figure 2.29a). This work achieved the filter realization following the guideline in [17] applying to a three-phase six-switch rectifier, but it lacks a CM filtering component and not passing the EMI conducted emission requirement in higher frequencies above 8 MHz (Figure 2.29b).

The same research team presented a similar filter focusing on CM EMI for 3-phase boost PFC converter [18]. As shown in Figure 2.30a, the filter has a $LCLCLC$ structure if including the boost inductors. The design uses only one set of DM capacitors C_X to reduce the size and weight of the filter. The number of filter stages is determined by the minimum attenuation requirement to guide volume minimization.

Example 2 Instead of a symmetric two-stage design, a two-step design for the two individual stages of an EMI filter is presented in [9, 19]. This proposed two-stage EMI filter utilizes a $LCLCL$ structure for a 10 kW three-phase, T-type three-level, boost-type PWM rectifier system, and it is optimized for minimal filter box volume. The main constraints for this design are EMI conducted emission requirement (industrial, 150 kHz to 30 MHz) and touch current limit requirement. Since having multiple line-to-ground capacitor stages would potentially violate the touch current limit, the first CM stage capacitor is connected to the mid-point of the DC linkage instead of the system ground. This property also relaxes the capacitance selection options for optimization and is found to provide a more stable DC link voltage.

The first filter stage mainly serves as boost inductance and EMI attenuation, and the filter is optimized with a procedure listed as follows:

1. initiate $L_{cm,1,tot} = 100 \times 10^{i/16}$ in µH, where $i = 5, 6, \ldots, 36$;
2. compute $L_{dm,1,tot}$ with given phase current ripple at no load condition;
3. compute $C_{dm,1}$ and $C_{cm,1}$ for the given voltage ripples;
4. design of CM inductor as $L_{cm,1} = L_{cm,1,tot} - L_{dm,1,tot}/3$;
5. design of DM inductor as $L_{dm,1} = L_{dm,1,tot} - L_{\sigma,1}$, where L_{σ} is the leakage inductance of the CM inductor.

The optimization uses the ratio between $L_{cm,1}$ and $L_{dm,1}$ to evaluate design options. The second filter stage uses a LCL structure to provide higher-order filtering for high-frequency EMI. The utilization of the third set of inductances enabled further volumetric reduction of the filter. The RC damping elements are used in both stages to eliminate the parasitic resonances within the designed filter.

Class 3c Filter Design No specific literature has been found promoting the use of subclass ‘c’ filters. However, subclass ’c’ filter designs are a practical technique that is applied in VFD applications PQ and EMI compliance must be met where a higher power density is required (such as naval shipboard requirements [139, 140]. The Class 3c filter design would involve the connection of inductors in series used to compensate for the non-linear, frequency-dependent characteristics of the converter-side inductor design. As has already been indicated, staging inductor in series on the converter side of the AFE filter may result in a smaller total filter volume when compared to subclass ’b.’ An indication of a future trend toward the Class 3c filter can be found in the application of Class 1c filters that exploit SiC or Gallium Nitride (GaN) MOSFETs to achieve extremely power-dense EMI-compliant dc-fed VFDs, and switch-mode power supplies [141, 142].

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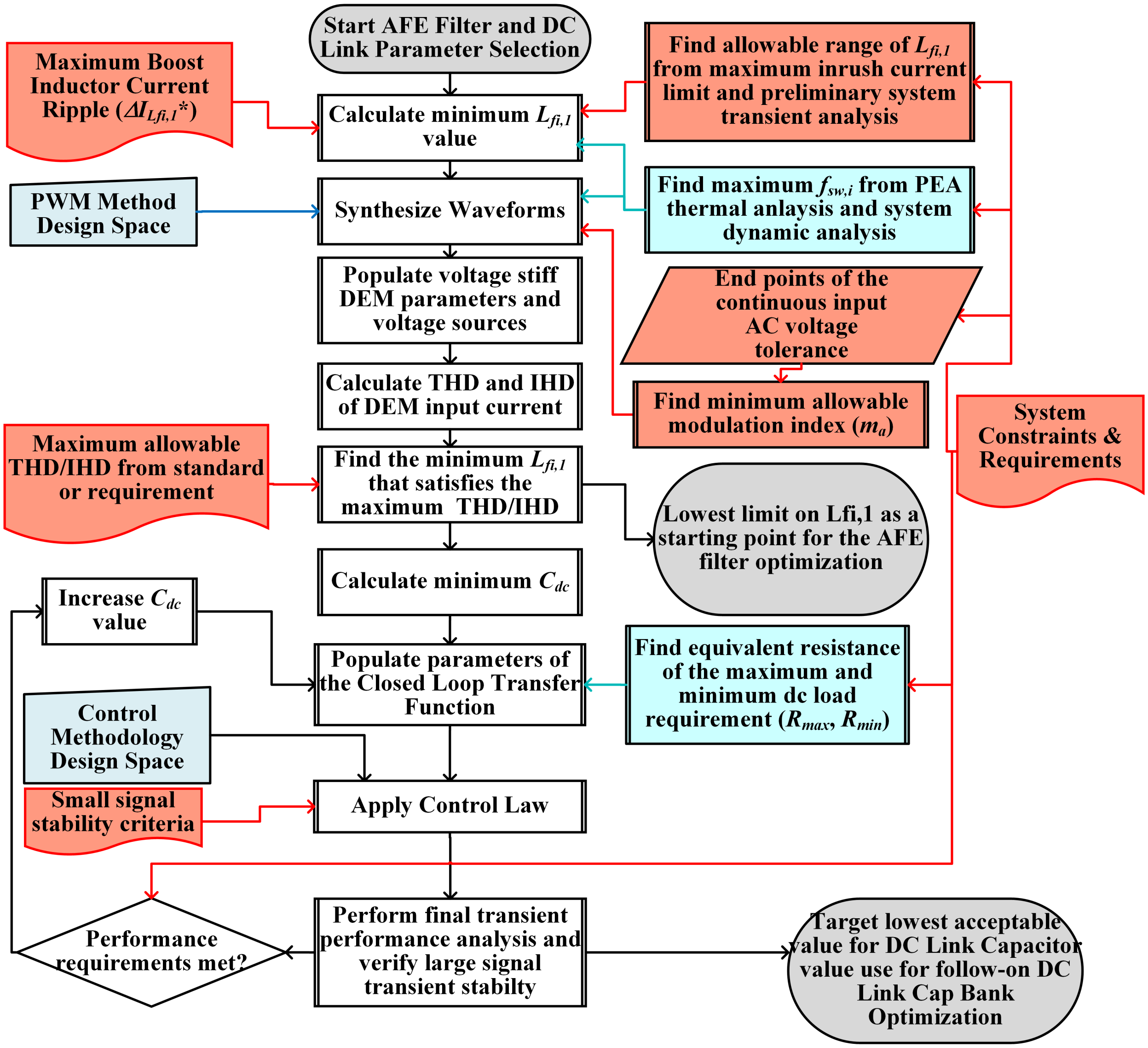


Figure 2.22: Process for determination of minimum $L_{fi,1}$ and C_{dc}

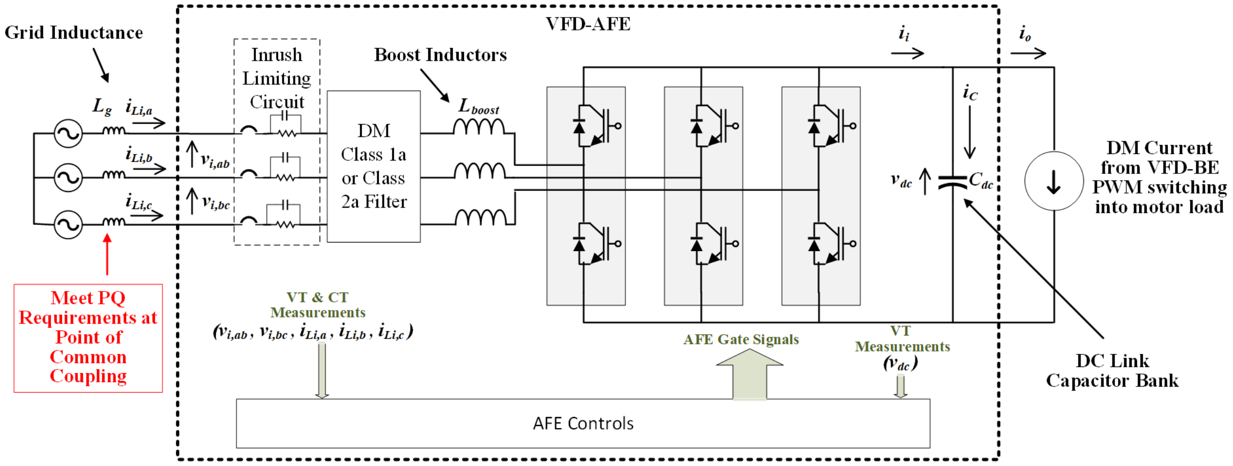


Figure 2.23: VFD-AFE with boost inductor and Class 1a or Class 2a filter

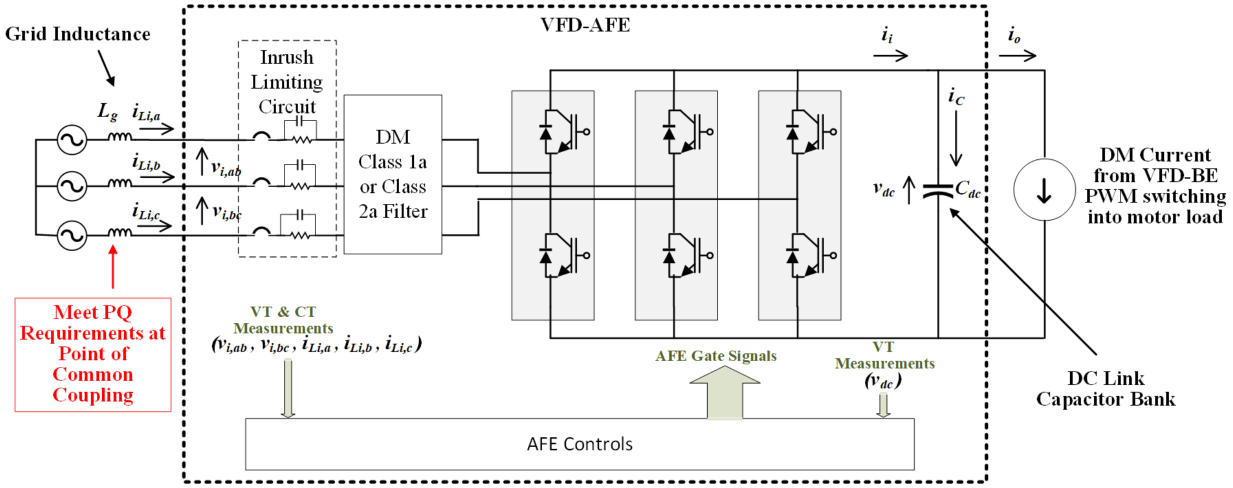
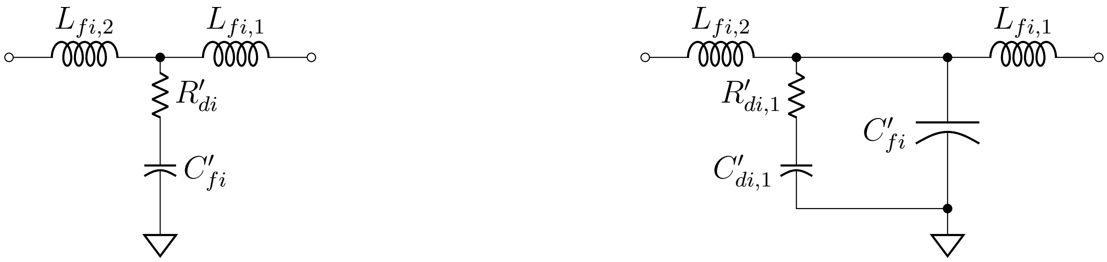


Figure 2.24: Integrative solution to VFD-AFE filtering with Class 1a or Class 2a filter



(a) Class 2a

(b) Class 2b

Figure 2.25: LN equivalent circuit representations of Class 2a (LCL) and Class 2b (LCCL) filters found in the literature

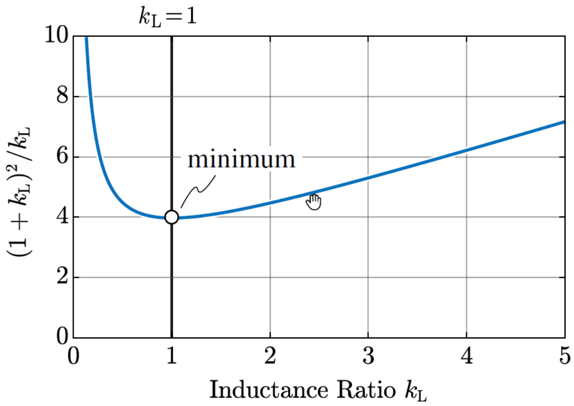
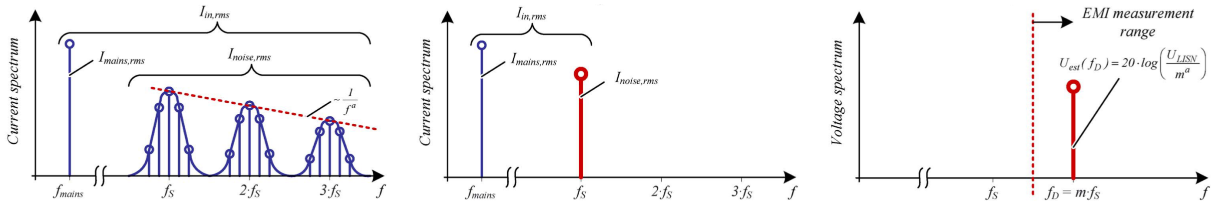


Figure 2.26: Asymptotic filter admitance trend of the proportionality factor, $\frac{(1+k_L)^2}{k_L}$ as a function of the inductance ratio k_L. [16]



(a) (b) (c)

Figure 2.27: Main idea of the noise estimation by (b) summing up all high-frequency current components in (a) to only one component at the switching frequency f_S and (c) calculating the estimated noise voltage at the design frequency f_D. [17]

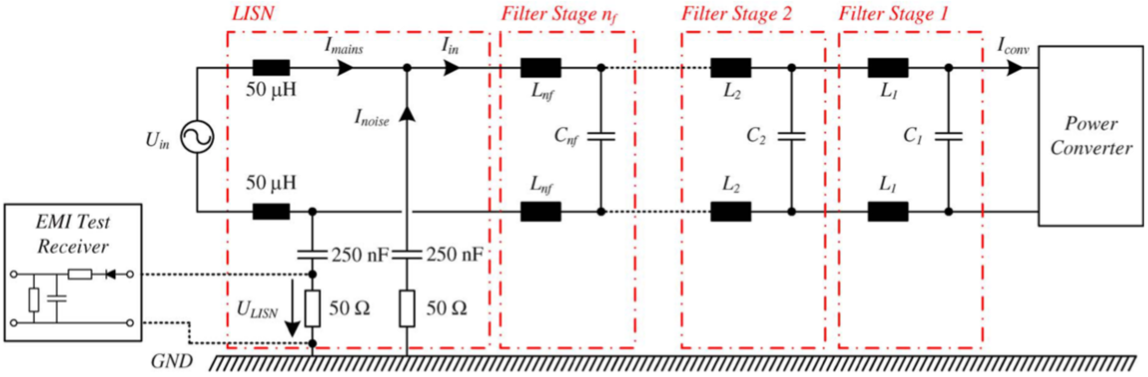
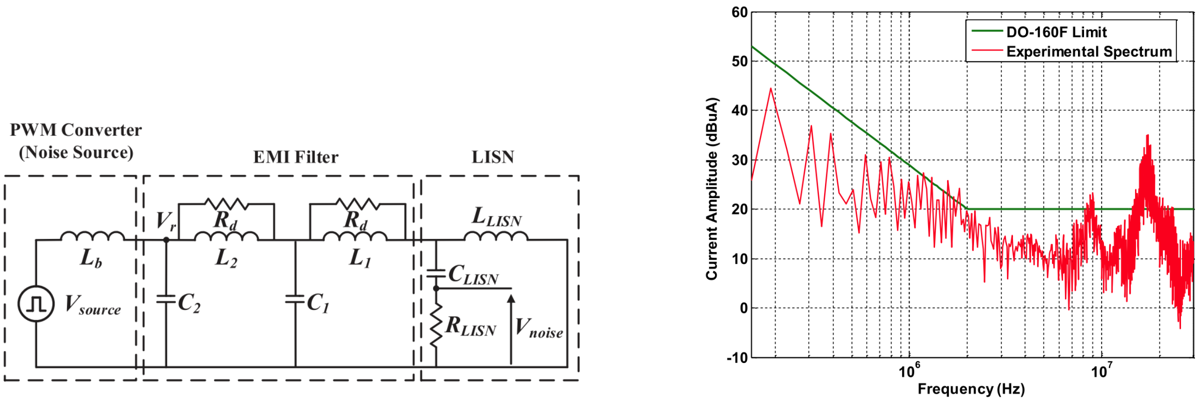
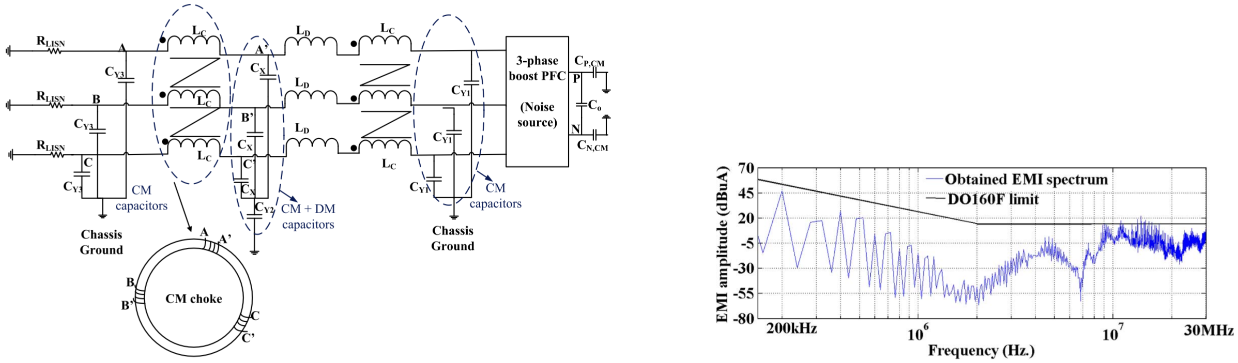


Figure 2.28: Topology of a DM input filter with nf filter stages and the simplified LISN together with the EMI test receiver. [17]



(a) (b)

Figure 2.29: Single-line DM model from [10] and the EMI conducted emission spectrum of the designed filter.



(a) (b)

Figure 2.30: Cascaded two-staged EMI filter for three-phase boost PFC [18], and the EMI conducted emission spectrum of the designed filter.

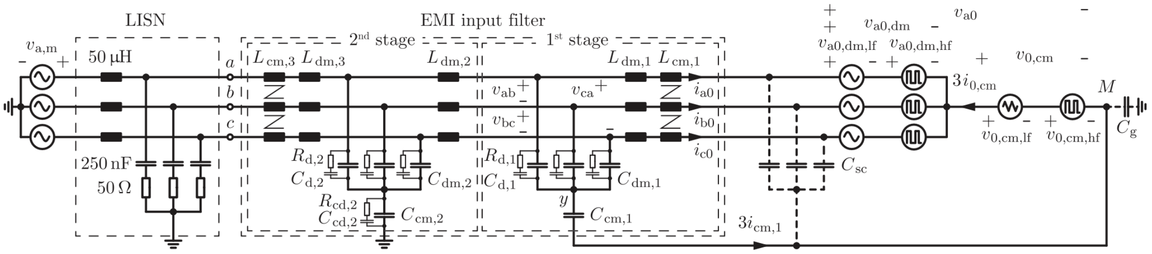


Figure 2.31: Equivalent circuit of the three-phase rectifier system and proposed two-stage EMI filter structure. [19]

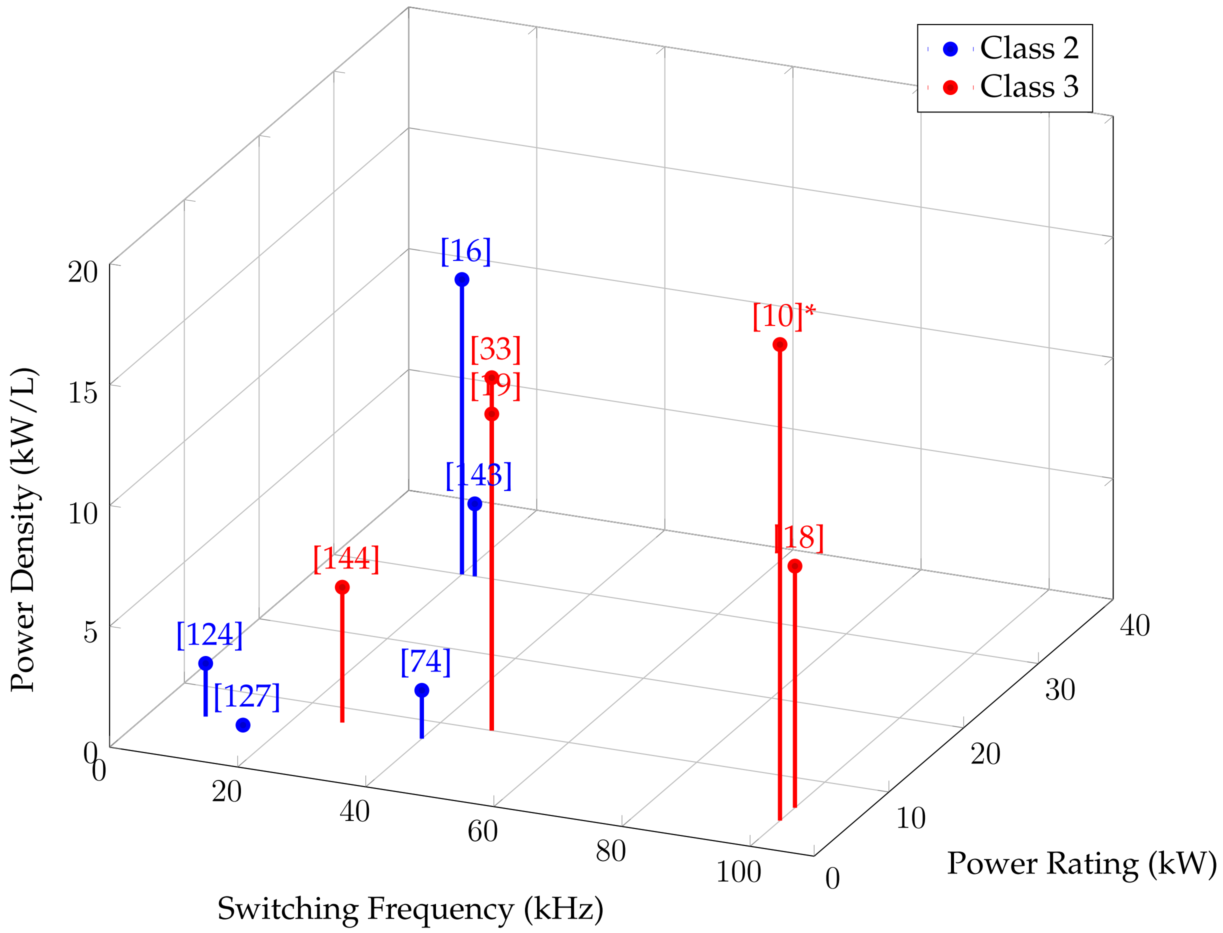


Figure 2.32: Existing Study Power Density vs. Power Rating (* [10] is DM filter only.)

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Table 2.5: Publication reporting hardware realizations of AFE filters

Publication Title	**Authors**	**Yr**	**Std.**	**Fltr**	**Dev. Type**	**Cir. Topo.**	f_{sw} **(kHz)**	**Pwr (kW)**	**Fltr** ρ **(kW/L)**	**Ref.**
Optimal design of LCL harmonic filters for three-phase PFC rectifiers	Muhlethaler, Kolar, Ecklebe	2013	Reduced THD	2b	IGBT	2L	8	6	2.2	[124]
LCL Filter Design and Performance Analysis for Grid Interconnected Systems	Reznik, Simoes, Al-Durra, Muyeen	2014	IEEE 519, IEEE 1547	2a	IGBT	2L	15	5	0.2	[127]
EMI Filter Volume Minimization of a Three-Phase, Three-Level T-Type PWM Converter System	Boillat, Krismer, Kolar	2017	CISPR 11, Class A	3b	SiC MOSFET	3L TT	48	10	13.1	[19]
Volume Optimization of a 30kW Boost PFC Converter Focusing on the CM/DM EMI Filter Design	Wyss, Biela	2017	EN 61000-3, CISPR 11 Class A	2b	IGBT	2L	22	30	3	[143]
A Comprehensive Design and Optimization of the DM EMI Filter in a Boost PFC Converter	Singh, Malik, Khaligh	2018	DO 160F	3b	SiC MOSFET	2L	100	4	19.7	[10]
Filter Design for AFE Rectifier using SiC MOSFET	Sun, Wei	2019	IEEE 519	2a	SiC MOSFET	2L	40	7.5	2	[74]
99.3% Efficient Three-Phase Buck-Type All-SiC SWISS Rectifier for DC Distribution Systems	Schrittwieser, Leibl, Haider, Thony, Kolar, Soeiro	2019	EMI	3b	SiC MOSFET	Swiss Rectifier	27	8	5.6	[144]
Design Space Optimization of a Three-Phase LCL Filter for Electric Vehicle Ultra-Fast Battery Charging	Cittanti, Mandrile, Gregorio, Bojoi	2021	IEEE 519	2a	IGBT	2L TT	20	30	12.2	[16]

2.3 Nomenclature Harmonization

2.3.1 Filter Element Naming and Numbering

Prior to a detailed discussion of the filter topology classes, a consistent nomenclature system needs to be introduced for the filter to be used to name inductive (L), capacitive (C), and resistive (R) components, coupling coefficients, leakage, symmetry/asymmetry factors, input (AFE) versus output (BE) filter, etc. The most complex aspects of the filter topology are associated with the inductors, as described below. Filter component subscripts starting with f are applied to those filter components whose principal design function is DM filtering. Filter component subscripts starting with e are applied to those components whose principal design function is CM filtering. Filter component subscripts starting with d are for resonance damping components. Subsequent subscripts i and o refer to input or output filters, respectively. The numbered subscripts, 1, 2, *etc.*, apply to the placement of the filter component(s) with respect to the noise source (switching power electronic circuit) and grid source or motor load. For any filter structure, input, or output, numbering (i.e. $L_{xx,1}$) starts at the noise source and increments in increasing numbers working out towards the grid source or motor load.

Figure 2.33 shows the three types of three-phase inductors that are considered in this study: three-phase CM inductor, DM common-core three-phase inductor, and DM separate core three-phase inductor assembly. The differences between these three inductor types and important parameters that represent aspects of various hardware implementations of the inductors are understood through matrix representations of the inductor's electrical behavior.

In each case, the inductor voltage equation is described by

$$\mathbf{v}_{L_{x,n}} = \mathbf{L}_{x,n} \cdot \frac{\mathrm{d}}{\mathrm{d}t}\mathbf{i}_{abc_{x,n}} \tag{2.65}$$

where x is either i or o, and $n = 1, 2, 3$ (such that 1 is closest to the power semiconductors).

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In cases where only a single filter stage is used, the n is left out.

For the CM inductor (Figure 2.33a), the inductance matrix is

$$\mathbf{L}_{x,n} = L_{ex,n}[\mathbf{k}_{Ax,n} + k_{ex,n} \cdot (\mathbf{J_3} - \mathbf{I_3})] = L_{ex,n} \begin{bmatrix} k_{Aax,n} & k_{ex,n} & k_{ex,n} \\ k_{ex,n} & k_{Abx,n} & k_{ex,n} \\ k_{ex,n} & k_{ex,n} & k_{Acx,n} \end{bmatrix} \tag{2.66}$$

where $L_{ex,n}$ is the average self-inductance of the CM inductor. The CM inductor is characterized by its CM and DM inductance. The CM inductance is mutual inductance defined by

$$L_{Mx,n} = L_e \cdot k_{ex,n} \tag{2.67}$$

where $k_{ex,n}$ is the mutual coupling factor.

The DM inductance is the difference between the average self-inductance and mutual inductance and corresponds to the leakage inductance of the three-phase common core winding. In the most common three-leg core geometries it is difficult to control the symmetry of the leakage inductance in all three phases. For this reason, the general CM inductor structure of Figure 2.33a includes an asymmetry factor which is represented by the diagonal matrix

$$\mathbf{k}_{Ax,n} = \begin{bmatrix} k_{Aax,n} & 0 & 0 \\ 0 & k_{Abx,n} & 0 \\ 0 & 0 & k_{Acx,n} \end{bmatrix} \tag{2.68}$$

The DM inductance of a given phase is the leakage inductance of that phase, or

$$L_{lx,n_a} = L_e(k_{Aax,n} - k_{ex,n}) \tag{2.69}$$

$$L_{lx,n_b} = L_{e_{lbx,n}} = L_e(k_{Abx,n} - k_{ex,n}) \tag{2.70}$$

$$L_{lx,n_c} = L_{e_{lcx,n}} = L_e(k_{Acx,n} - k_{ex,n}) \tag{2.71}$$

If the only design objective of the CM inductor is to limit CM current then it is important to eliminate winding leakage asymmetry such that

$$k_{Aax,n} = k_{Abx,n} = k_{Acx,n} \simeq 1 \tag{2.72}$$

Some researchers have attempted to incorporate both DM and CM inductance into a single common core structure [9, 142, 145], in which case, meeting the criteria on 2.72 is critical. However, in most cases, the aim is to minimize the leakage found from (2.69)-(2.71) in order to avoid the coupling of DM flux into the core. If it symmetry is assumed then a single leakage inductance term can represent the DM component in each phase as $L_{lx,n}$.

This following section needs revision according to new findings that are published in APEC 2023 paper.

For the common core DM three-phase inductor (Figure 2.33b, the inductance matrix is

$$\mathbf{L}_{fx,n} = L_{fx,n}\left(\mathbf{I}_3 + \mathbf{k}_{lx,n}\right)\mathbf{L}_{x,n} = L_{fx,n}\begin{bmatrix} 1 & k_{abx,n} & k_{cax,n} \\ k_{abx,n} & 1 & k_{bcx,n} \\ k_{cax,n} & k_{bcx,n} & 1 \end{bmatrix} \tag{2.73}$$

where mutual coupling due to asymmetrical leakage paths is accounted for by the asymmetrical coupling matrix

$$\mathbf{k}_{lx,n} = \begin{bmatrix} 0 & k_{abx,n} & k_{cax,n} \\ k_{abx,n} & 0 & k_{bcx,n} \\ k_{cax,n} & k_{bcx,n} & 0 \end{bmatrix} \tag{2.74}$$

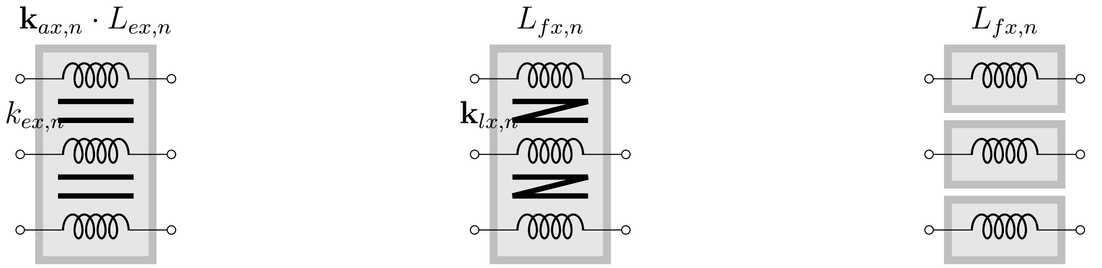
For the separate core DM three-phase inductor (Figure 2.33c, the inductance matrix is

$$\mathbf{L}_{fx,n} = \begin{bmatrix} L_{fx,n} & 0 & 0 \\ 0 & L_{fx,n} & 0 \\ 0 & 0 & L_{fx,n} \end{bmatrix} \tag{2.75}$$

Considering only the fundamental component of phase currents, a minimum volume-designed common-core three-phase DM inductor will have a lower boxed volume than three separate DM inductors. However, if the common core DM inductor is connected directly to the power electronics, where both CM and DM stresses are the highest, the coupling factors of 2.74 will cause flux from CM noise to limit the flux supported by the core. If the coupling is tight, as will be the case for a minimum volume design, and asymmetry in the coupling factors, as will be the case with the typical three-leg EI or EE gapped core, then the inductor may saturate due to CM effects. As a result, common core, EI, or EE-gapped core DM inductors tend to be overdesigned. The mode conversion from CM to DM noise into the inductor is minimized when

$$k_{abx,n} = k_{Abx,n} = k_{Acx,n} \simeq 0 \tag{2.76}$$

In this case, the DM common core three-phase DM inductor is essentially the same as the three separate core DM inductors. Alternatives core structures to the commonly applied EI or EE common core three-phase inductors that meet the criteria of 2.76 have been investigated [146–148].



(a) CM inductor

(b) DM common core three-phase inductor

(c) DM separate core three-phase inductor assembly

Figure 2.33: Inductor structures: Gray-shades stand for inductor core (common/separate). Black shapes stand for winding direction. k_e: coupling coefficient. k_a: asymmetry. k_l: leakage coupling. i: input. o: output.

2.3.2 AFE Filter Topology Classification

Three classes of filter topologies are designated as Class 1, Class 2, and Class 3. The literature review of AFE filters can be organized according to these classes and variations in filter structure, or sub-classes, within each filter class (*i.e.*, Class 1a, Class 1b, *etc.*). The class number principally corresponds to the number of stages and order of the DM filter (ignoring the poles and zeros introduced by passive damping). CM filter stages generally follow the same structure, but in some sub-classes, the CM filter order is higher than the DM filter.

For each filter class, the sub-class 'c' (*i.e.*, Class 1c, Class 2c, and Class 3b) incorporates all of the elements of the preceding subclass but deals with the wide spectral range of EMI noise by staging different inductors in series to form the total DM and CM inductance closest to the noise source (*i.e.*, the power electronic side connection). These inductors will compensate for the attenuation drop in higher frequency caused by the non-linear frequency dependence of the inductors in the part of the circuit that absorbs the highest stress produced by the switching of the power semiconductors, or, more succinctly, the power electronic-side DM inductor(s). This method allows the designer to shape the high-frequency attenuation of the filter to pass both PQ and EMI standards without introducing a higher-order filter. It should be noted that, in practice, both PQ and EMI standards cannot be easily met with anything but subclass ‘c’ filters. However, this point is not acknowledged in much of the literature, and it is for this reason that the lower ‘a’ and ‘b’ sub-classes must be considered. Also, if the VFD is only required to meet a PQ limit, then the low ‘a’ or ‘b’ sub-classes may be sufficient.

Within each filter topology class, a range of inductor realizations can be considered, falling under the three inductor type classifications shown in Figure 2.33. Combining inductor types and the range of variations on each type with the filter classes results in a very wide design space for filter implementations both on the AFE- and VFD- sides of the drive system. The literature on the filter design aspects of drive system implementations covers the broad range of filter implementations, which can be generalized as set forth in this document. The contributions of the filter literature will be organized according to these classifications and types.

Class 1

Class 1 filter topology contains only a single stage of DM inductors with no DM equivalent capacitive filter elements (Figure 2.34 through 2.36). A minimum level of DM inductance and the DC link capacitance is required for the AFE to function properly, as influenced by the control method. The DM inductance must provide a sufficiently stiff current, and the DC link capacitance must provide a sufficiently stiff voltage against which AFE power semiconductors work to synthesize input AC currents from the grid into a DC voltage.

The CM part of Class 1 provides attenuation to CM EMI noise in MF and HF frequency ranges. The most common structure of the CM filter is the second order LC filter, where line-to-ground (LG) (typically feed-through capacitors) form the interface between the AFE electrical connection and the grid. It is important to note that PQ and/or EMI standards generally limit the allowable capacitance to ground per line. If the LG capacitance is too high, it will result in excessive high-frequency current flowing into the chassis ground structure.

As with all of the filter topology classes presented, it is possible for the Class 1 filter to meet both PQ and EMI standards, but at a significant size penalty because DM emissions will only roll off at -20dB per decade while CM emissions (for Classes 1b and 1c) roll off at -40dB per decade. Without extreme measures taken in the core material selection and design of both CM and DM inductors, only Class 1c is likely to meet the EMI standard over the full spectral range.

Class 1a The Class 1a filter is comprised of either a single DM inductor in series with a CM inductor (Figure 2.34a) or, more effectively, a single power electronic interfacing and grid interfacing DM inductor, $L_{fi,1}$ and $L_{fi,2}$ respectively on either side of a CM inductor, L_{ei}, as shown in Figure's 2.34b and 2.34c. The DM inductors may be either three separate single-core inductors or a single three-phase common-core inductor. If two stages of DM inductors are included, then the grid-side DM inductor, $L_{fi,2}$ will be a three-phase common core inductor. In this case, there is no benefit to the grid-side DM inductor having its cores separated out because $l_{fi,1}$ and L_{ei} absorb the majority of the CM stress.

Class 1b The Class 1b filter is distinctive from the Class 1a by the addition of a 2$^{\text{nd}}$ order CM LC filter as shown in Figure 2.35. Typically, if the AFE filter is not required to meet a PQ standard but only an EMI standard, then the 2$^{\text{nd}}$ order CM filter is the best practice to achieve a reasonable size and weight of the filter.

Class 1c The Class 1c filter is shown in Figure 2.36. This class of filter differs from the Class 1b filter in one respect, the addition of series CM and DM inductors, each designed to provide a linear inductance versus frequency characteristic over a specific spectral range. This approach may be applied to shape the frequency characteristics of the required insertion loss needed to bring CM and DM conducted emissions below the limit over the full spectral range of the EMI standard.

Table 2.6: Filter Topology Category

Class	**DM**	**CM**
1a	L	L
1b	L	LC
1c	$L \cdots L$	$L \cdots LC$
2a	LCL	LC
2b	LCC^dL	LC
2c	$L \cdots LCC^dL$	$L \cdots LC$
3a	$LC \cdots LC \cdots LCL$	$LC \cdots LC \cdots LCL$
3b	$LCC^d \cdots LCC^d \cdots LCC^dL$	$LC \cdots LC \cdots LCL$
3c	$L \cdots LCC^d \cdots LCC^d \cdots LCC^dL$	$L \cdots LC \cdots LC \cdots LCL$

C^d: Damper branch

One important point to be made is that the LG capacitors of the CM filter present a DM capacitance in the differential equivalent model (DEM) of the system or equivalent single-phase line-to-neutral (LN) representation of the circuit. As a result, it is appropriate to include $L_{fi,2}$ on the grid side of the filter in order to ensure consistent PQ and EMI behavior, regardless of the grid inductance of the installation. It is acknowledged that a DM LC resonance may occur between L_{fi_2} and C_{ei}, however common practice is to rely upon the electrostatic resistance (ESR) of the LG capacitors to dampen out the high-frequency resonance between these two components. Generally, this is a good practice because the LG capacitors can have a high ESR without diminishing the CM attenuation of the filter, and the associated resonant frequency will tend towards such a high frequency that the increased resistance of L_{fi_2} due to skin effect will add to the ESR damping capability of the LG capacitors.

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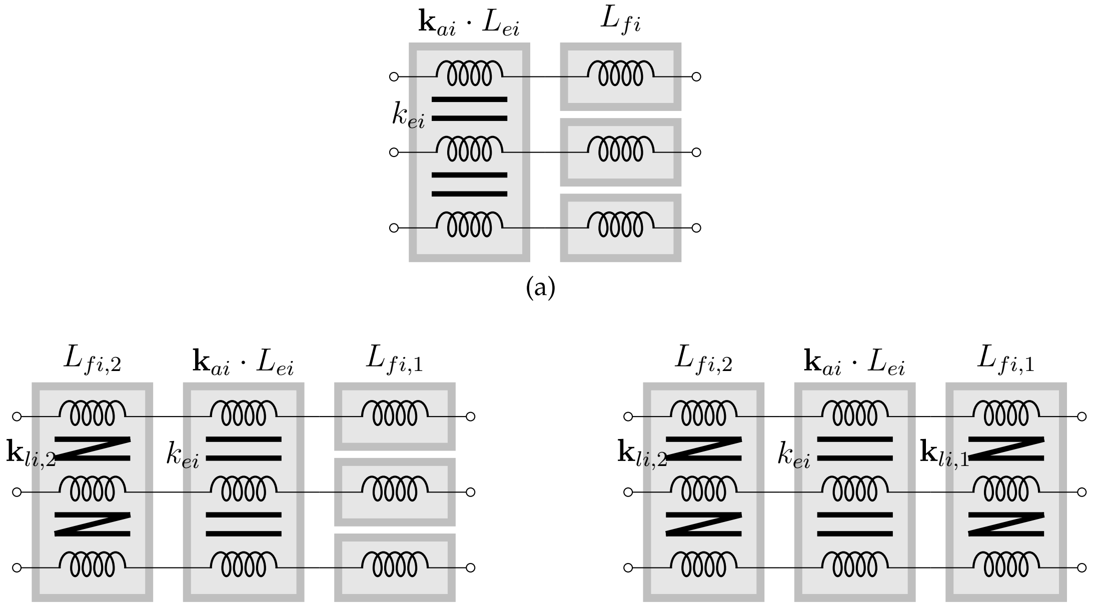


(a)

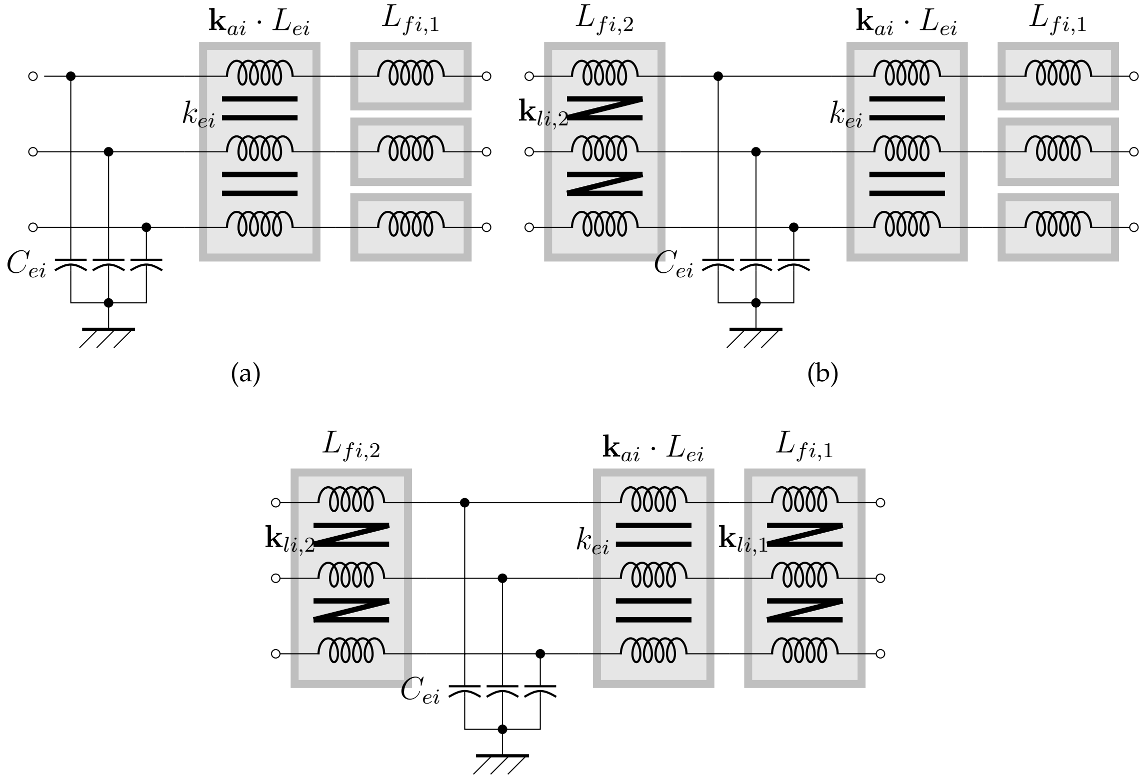
(b) (c)

Figure 2.34: Class 1a

Class 2

The Class 2 filter topology (Figure 2.37 through 2.39) provides 2^{nd} order attenuation of DM noise produced by the AFE with grid-side inductance de-coupling and represents the most common PQ filter found in the literature: the LCL with 2^{nd}-order resonance damping [16, 92, 93, 122–124, 126, 127, 129, 130, 132, 133, 135, 149, 150]. Class 2 filters are most effectively applied to the attenuation of noise in the Very Low Frequency (VLF) to Low Frequency (LF) ranges of the International Telecommunication Union (ITU) defined radio spectrum (3-300kHz). In the literature, Class 2 filtering is generally confined to DM filtering to meet PQ limits. However, the concept can be extended to meet both DM and CM filtering of EMI. For this reason, the general representations of Class 2 filters in Figure 2.37 through 2.39 incorporate both CM and DM filtering.

Class 2a The Class 2a filter topology of Figure 2.37 is best understood by considering the single phase LN equivalent and CEM circuits shown in Figure 2.40. In these figures, the grid connection is on the left and the noise source (PEC connection) is on the right.



(a)

(b)

(c)

Figure 2.35: Class 1b: DM: L, CM: CL

If the filter includes both CM and DM inductors, then the inductance on the PEC-side of Figure 2.40b is

$$L'_{Mi} = \frac{L_{fi,1}}{3} + L_{Mi} + \frac{L_{lx,n}}{3} \tag{2.77}$$

If the Class 2a filter does not include CM filtering (which is what is reflected in most of the research) then C_{ei} is eliminated from the filter equivalent circuits of Figure 2.40 and L'_{Mi} in Figure 2.40b becomes

$$L'_{Mi} = \frac{L_{fi,1}}{3} \tag{2.78}$$

This configuration is the most common LCL filter found in the literature. Because both $L_{fi,1}$ and $L_{fi,2}$ both introduce LC resonant modes with C_{fi}, the Class 2a filter includes a

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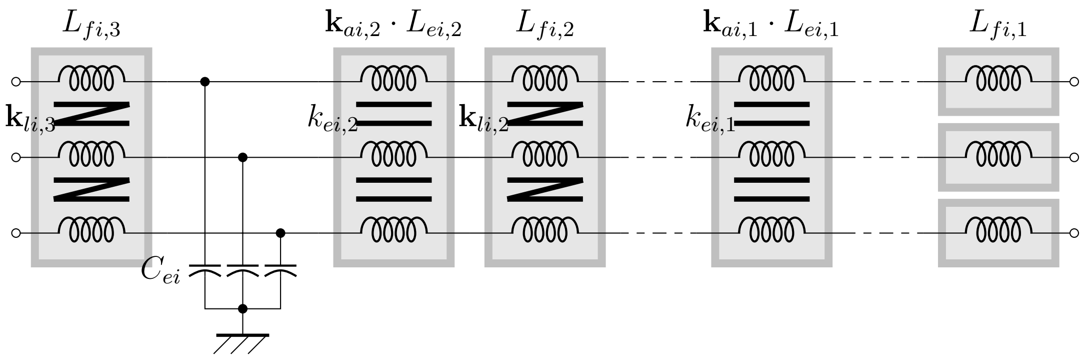
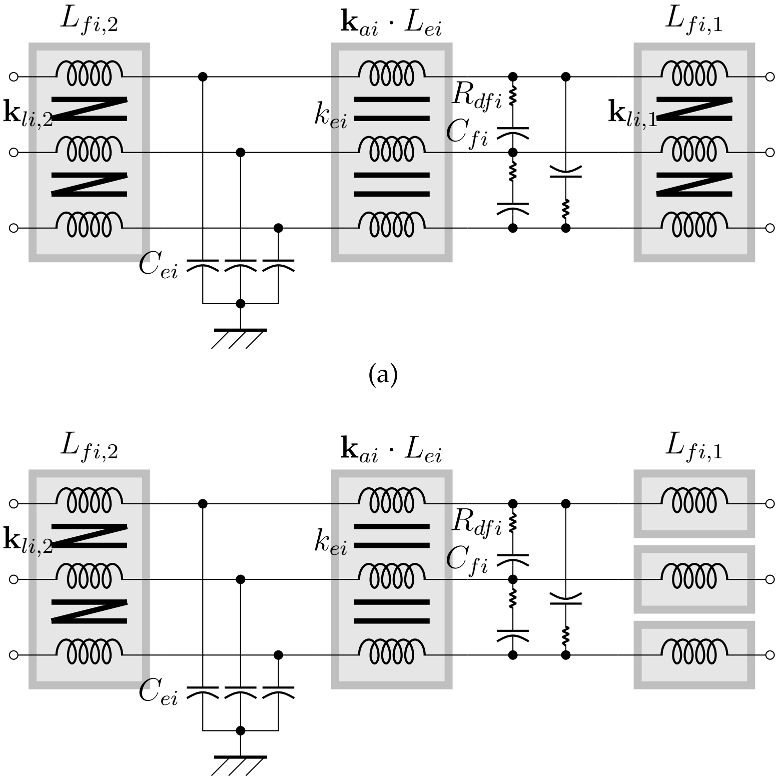


Figure 2.36: Class 1c: DM: LL, CM: CLL

damping resistor R_{di} to dampen out resonance mode(s).

Active filtering In a motor drive system, it is possible to utilize active filtering to attenuate the low-frequency nuances and passive filtering to mitigate high-frequency EMI [151–155]. Such hybrid filter will allow smaller passive filter LC value, *i.e.*, higher corner frequency since the low-frequency noise is already suppressed with active damping. The location of the active filter is different among designs. [151, 152] have the active filter installed between the converter and motor to attenuate the low-frequency CM noise, while designs such as [153] install the filters in series between the grid-tie and the converter. The design from [154] installed the active filter between two stages of CM capacitors to dampen the un-suppressed CM noises circulating in the induced CM path.

Class 2b This subclass is typically introduced when PQ and EMI requirements must be met simultaneously. The series RC network introduces parasitic inductance that can cause increases in DM conducted EMI at higher frequencies. It is a common practice to introduce a line-to-line capacitive filter network with well-controlled bus interconnection inductance to achieve good high-frequency conducted EMI behavior. The RC damping circuit is still required so a paralleled RC damping network must be added. This filter configuration is typically referred to as $LCCL$ in the literature.

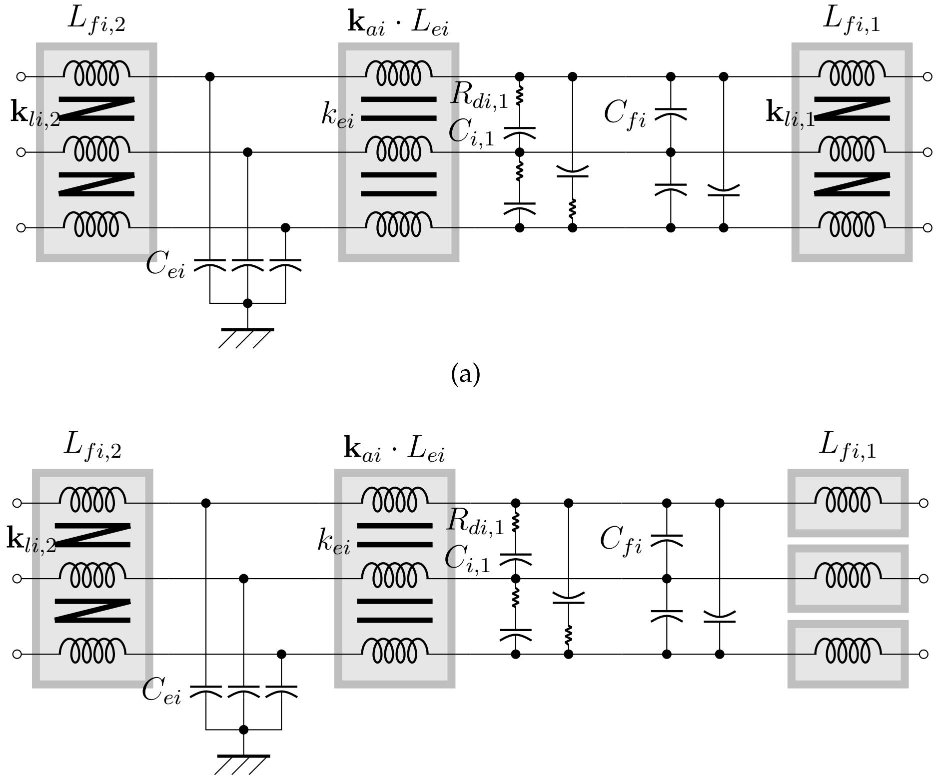


(a)

(b)

Figure 2.37: Class 2a: DM: LCL, CM:LC

Class 2c The addition of inductors in series on the PEC-side of the filter to shape the filter response may be applied to the Class 2 filter, but it is more effectively applied to Class 3.



(a)

(b)

Figure 2.38: Class 2b: DM: LCC^dL, CM: LC

Class 3

Class 3 filter topology handles power quality standard addressed harmonics in ULF separately from EMI standard addressed noises in MF and HF frequency ranges. This class of filters is becoming more common in the literature as, with the advent of WBG power semiconductors, the dominant DM noise associated with switching frequency harmonics moves into the MF to HF frequency ranges. Even with the more conventional designs with IGBT-based AFE, this class of filter has been utilized in order to comply with both PQ and EMI standards.

The DM part of the class 3 filter consists of multi-stages of LC to form a 3$^{\text{rd}}$- or higher-order filter (Figure 2.42). In the scenario where the Class 2 filter would not mitigate the high-frequency nuances, more stages of DM LC can be added to increase the high-frequency attenuation of the filter.

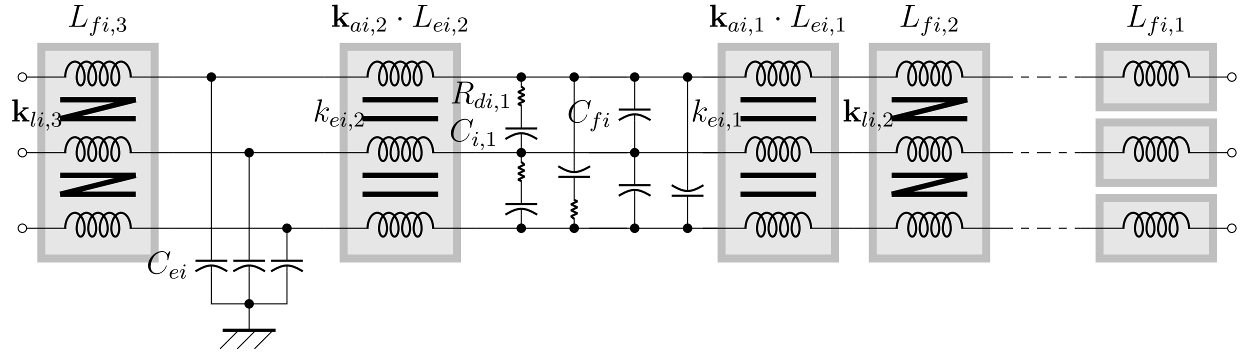
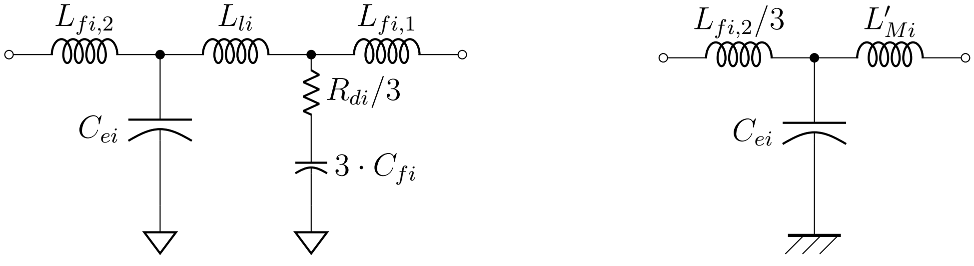


Figure 2.39: Class 2c: DM: LC^dCLL, CM: $LCLL$



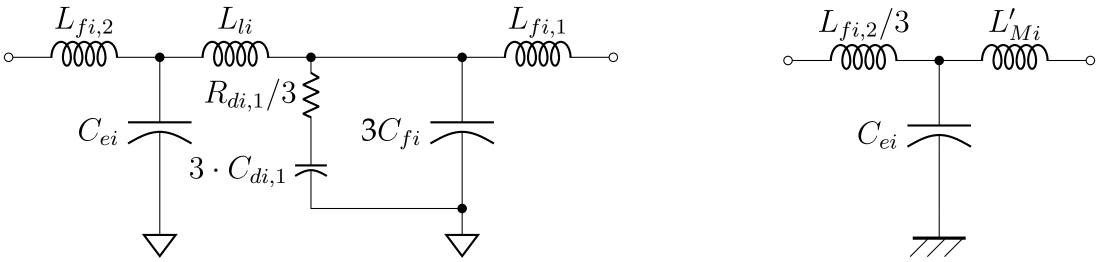
(a) DM Equivalent Circuit

(b) CM Equivalent Circuit

Figure 2.40: Class 2a DM CM circuits if $k_{abi,2} = k_{bci,2} = k_{cai,2} = 0$; $k_{abi,1} = k_{bci,1} = k_{cai,1} = 0$; $k_{aai} = k_{abi} = k_{aci} = 0$

The CM part of the filter also utilizes the higher-order structure to increase the EMI noise in the HF range. Since more stages of LC would increase the circuit ties to the ground or chassis, increasing the ground currently, the additional CM stages would violate the ground current limit and other grounding requirements. To avoid such a scenario, one or more CM stages can have their capacitors connected to the mid-point of the DC-linkage, and the final stage, the chassis. By assuming that the midpoint of the DC-linkage is connected to the ground by a parasitic capacitance, a significant amount of CM current will be circulating between these CM filter stages and the midpoint.

Class 3a Similarly with Class 2a, this subclass uses generic RLC to shape the corner frequencies of the 3^{rd}- or higher-order filter. However, the numeric LC combinations will generate multiple parasitic resonances within the multi-stage filter.



(a) DM Equivalent Circuit (b) CM Equivalent Circuit

Figure 2.41: Class 2b DM CM circuits if $k_{abi,2} = k_{bci,2} = k_{cai,2} = 0$; $k_{abi,1} = k_{bci,1} = k_{cai,1} = 0$; $k_{aai} = k_{abi} = k_{aci} = 0$

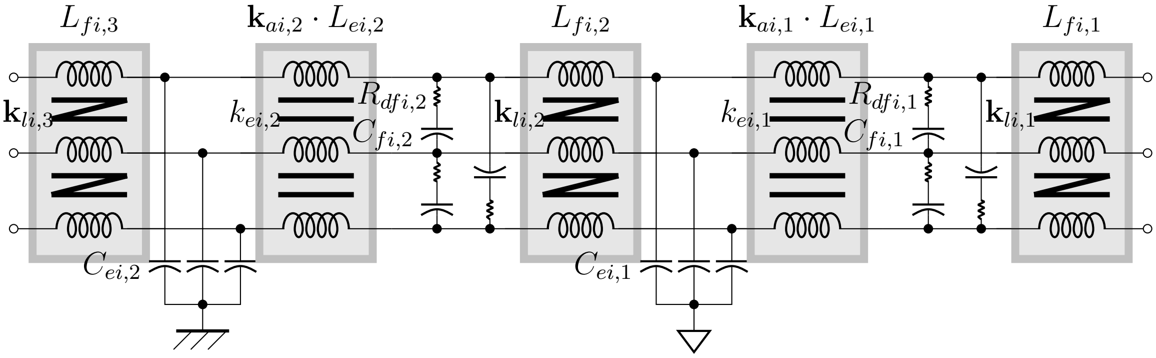


Figure 2.42: Class 3a

Class 3b Similarly with Class 2b, Class 3b adds RC dampers to suppress the parasitic resonances from the existing LC stages in the DM part of the filter.

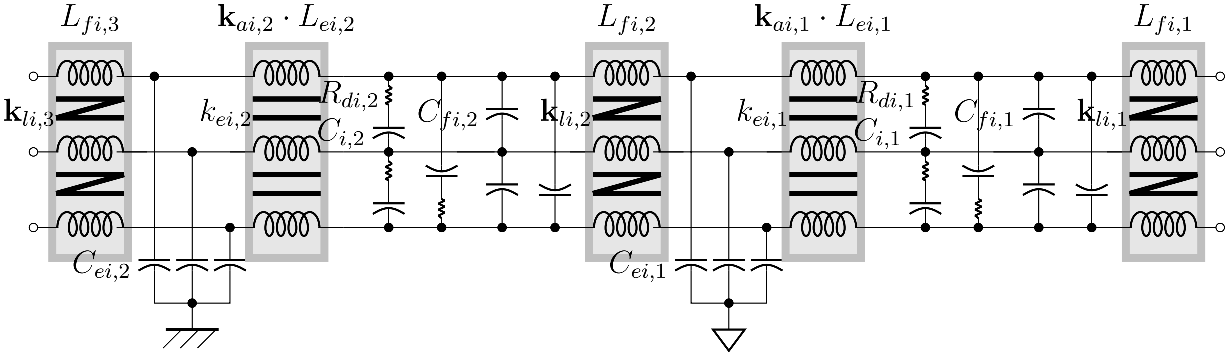


Figure 2.43: Class 3b

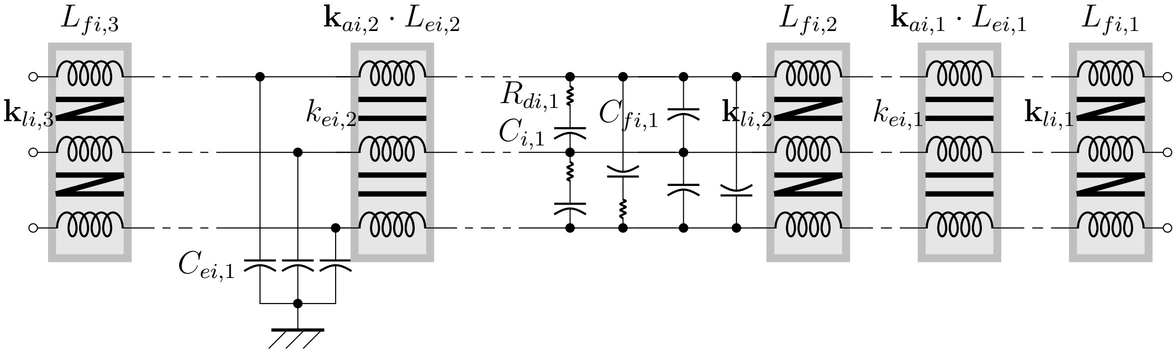
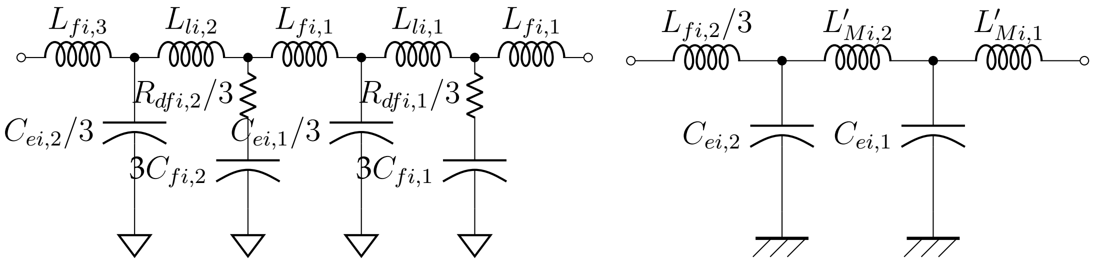


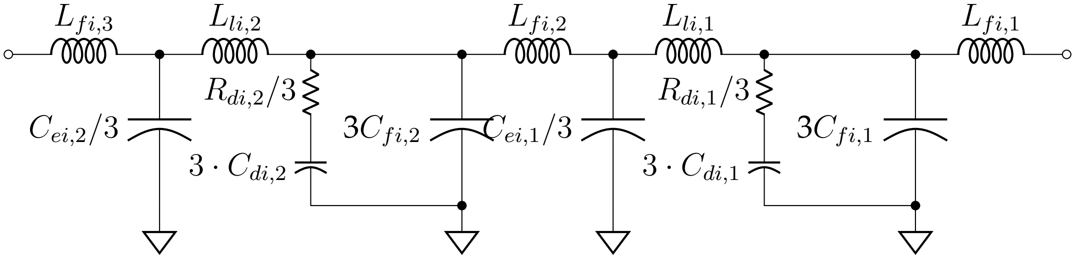
Figure 2.44: Class 3c



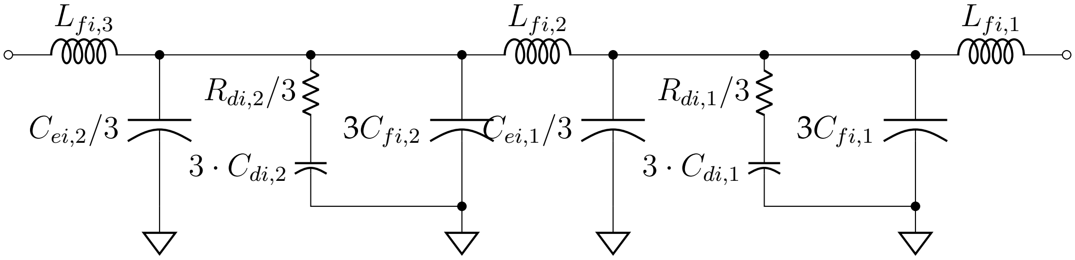
(a) DM Equivalent Circuit

(b) CM Equivalent Circuit

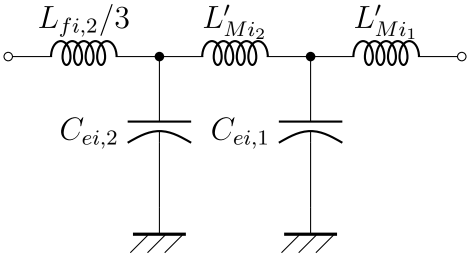
Figure 2.45: Class 3a DM CM if $k_{abi,2} = k_{bci,2} = k_{cai,2} = 0$; $k_{abi,1} = k_{bci,1} = k_{cai,1} = 0$; $k_{aai} = k_{abi} = k_{aci} = 0$



(a) DM Equivalent Circuit

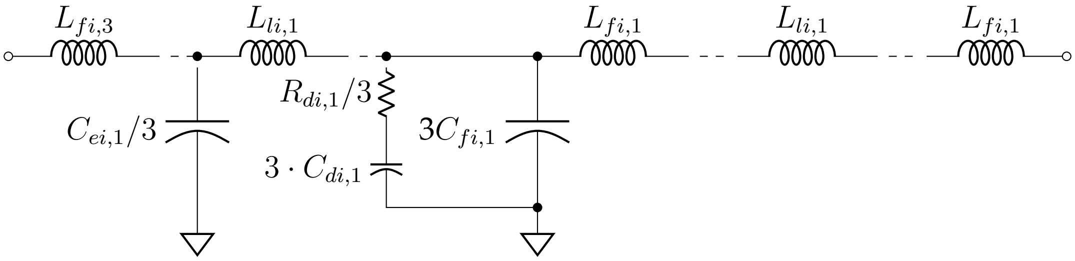


(b) DM Equivalent Circuit 2

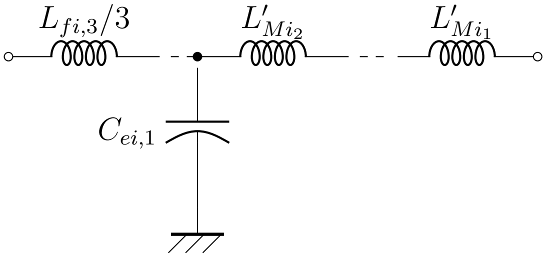


(c) CM Equivalent Circuit

Figure 2.46: Class 3b DM CM circuits if $k_{abi,2} = k_{bci,2} = k_{cai,2} = 0$; $k_{abi,1} = k_{bci,1} = k_{cai,1} = 0$; $k_{aai} = k_{abi} = k_{aci} = 0$



(a) DM Equivalent Circuit



(b) CM Equivalent Circuit

Figure 2.47: Class 3c DM CM circuits if $k_{abi,2} = k_{bci,2} = k_{cai,2} = 0$; $k_{abi,1} = k_{bci,1} = k_{cai,1} = 0$; $k_{aai} = k_{abi} = k_{aci} = 0$

2.4 Industrial and Military Standards

2.4.1 Power quality standards

Before the utilization of WBG semiconductors, power quality standards drove most of the AFE filtering designs as the spectral content of the non-WBG converter rarely enters the EMI control frequency ranges with significant amplitude. The commercial industry and military treat power quality control differently. These differences can be seen in their required measurement methods, measurement requirements, quantity definitions, and proposed limits.

Industry Standards: IEEE 519-2014, IEC/EN 61000-3-2

The IEEE 519-2014 [24] and IEC 61000-3-2 [23] are applied to industrial products in different jurisdictions, but the content and required power quality measurement methods, measurement requirement, and proposed limits on power quality nuances are harmonized across these standards. For AFE filter designs, the focus within such PQ standards is usually on harmonic controls. IEEE and IEC power quality standards address harmonic limits that represent shared responsibility for harmonic control between system owners or operators and users [24, 156]. The amount of harmonic voltage distortion supplied to other users is a function of the aggregate effects of the harmonic current producing loads of all users and the impedance characteristics of the supply system. Harmonic voltage distortion limits are provided to reduce the potential negative effects on the user and system. The IEEE 519 requires total harmonic distortion (THD) for both voltage and current as defined in (2.79) and (2.80). Up to the 50^{th} harmonic of the fundamental, either 50 Hz or 60 Hz, needs to be measured, which lies at either 2.5 kHz or 3 kHz. As mentioned before, the frequencies between the high-end frequency for harmonic control (3 kHz) to the low-end frequency for conducted emission EMI control (150 kHz) are unregulated.

$$\mathrm{THD}_V = \frac{1}{V_1}\sqrt{\sum_{n=2}^{N} V_n^2} \quad (N \leq 50) \tag{2.79}$$

$$\mathrm{THD}_I = \frac{1}{I_1}\sqrt{\sum_{n=2}^{N} I_n^2} \quad (N \leq 50) \tag{2.80}$$

The Individual Harmonic Distortion (IHD) is defined and set with limits by the ratio of individual current harmonics (up to 50^{th}) to rated load current [156]. Such industrial standards also recommend limiting current ripple above the 35^{th} harmonic to address safety considerations for particular equipment.

The measurement methods and requirements are practically identical across these mainstream industrial standards. Measurement instrumentation is ubiquitous commercially.

Military Standard: MIL-STD 1399 Section 300b

The MIL-STD 1399 Section 300b defines the standard interface requirements for and the constraints on the design of shipboard user equipment that will utilize shipboard alternating current (AC) electric power [22]. In addition to the 60 Hz system, the MIL-STD 1399 Section 300b sets requirements for a 400 Hz AC system. As shown in (2.81), the military PQ standard defines the THD differently from the industrial standards. [25]

$$\mathrm{THD}_V = \sqrt{\sum_{n=2}^{N} \left(\frac{V_n}{V_1}\right)^2} \tag{2.81}$$

For current IHD requirements, MIL-STD 1399 covers frequencies up to 20 kHz. But both the harmonic limit and the testing instrument requirement from 2.5 kHz to 20 kHz are much more relaxed compared with what is required under 2.5 kHz. Moreover, the MIL-STD has PQ and EMI overlapping frequency-wise, the limit lines are similar, but the testing requirements are different.

2.4.2 EMC Standards: Conducted Emission

EMC standards across the world treat EMI-conducted emissions separately from radiated emissions. The frequencies covered by EMI radiated emission usually starts around 30 MHz and ends in the gigahertz range [156]. This frequency range is beyond the 100^{th} harmonic of the switching frequency as high as 300 kHz. EMI radiated emission is not considered in this project. But with the reduction of the physical size of the converter systems, conducting structures are becoming more efficient radiators or megahertz range RF radiations, which will cause new inter- and intra-system compatibility issues. The authors of this study believe that radiated emission research is worth attention in future phases of the XPC project.

With the utilization of WBG semiconductors, the high edge rates and high switching frequencies have driven the spectral nuances into the frequencies covered by EMI conducted emission requirement. Publications on high power density drive designs have been shifting their focus to meet EMI standards instead of power quality harmonic controls.

The methodology's core of the EMI conducted emission test is to acquire an in-line voltage spectrum between the power source and the equipment under test (EUT) during its rated operation condition. A limit of the in-line voltage spectrum across a certain frequency range is required so that the common-coupling point, *i.e.*, the power source that is shared among other equipment, is not polluted with an excessive amount of EMI. This in-line voltage acquisition was historically made without any device implementation between the EUT and the power source, but since the early 80s [157], artificial networks were developed to mimic better the influence of the interactions between the EUT and the electrical system where the EUT would operate in. Eventually, standards across different military services and industrial societies would adopt their own designed artificial networks, namely the Line Impedance Stabilization Networks. The LISN structures have differences that are often ignored by researchers since their frequency responses are sim-

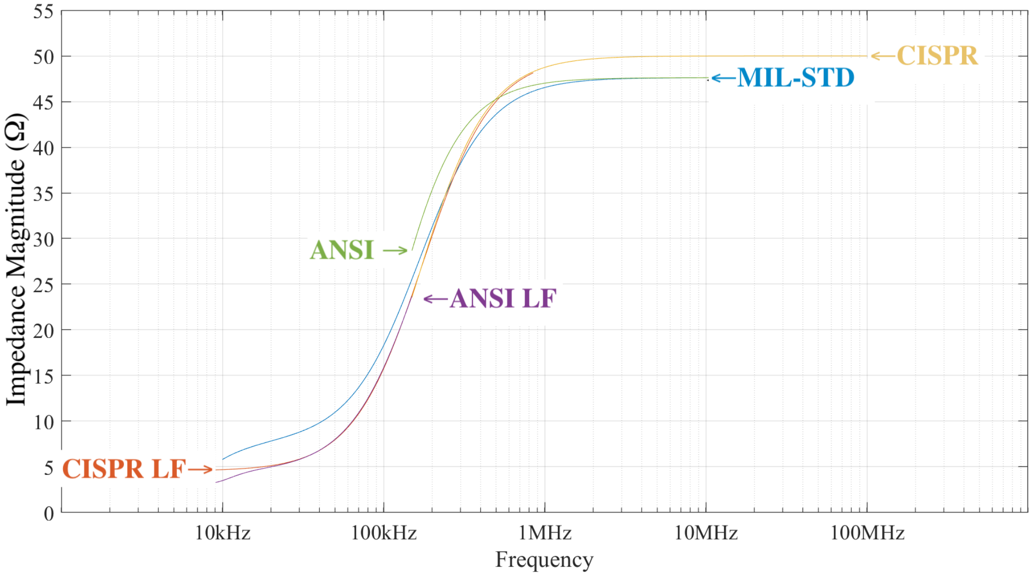


Figure 2.48: LISN frequency responses among different standards

ilar (Figure 2.48).

Since the EMI-conducted emission standards are imposed only to govern inter-system compatibility, self-compatibility and EMI immunity are not defined or required in these parts of the corresponding EMC standards.

Industrial Standards: CISPR 11, EN 55011, FCC Part 15

The Comité International Spécial des Perturbations Radioélectriques (CISPR) published CISPR 11 [21] with the baseline EMI conducted emission test requirement and limit for industrial equipment described in the generic EMC standard IEC 61000-6-4 [158]. EN 55011 [27] is the European adoption of the same standard. Similarly, for other equipment classes, the CISPR standard number can be seen in the last two digits of EN 550xx. The FCC Part 15 [26] is the United States regulation for unintentional RF emitters and has a very similar requirement in EMI-conducted emission.

The industrial standards require a set of LISN and a spectrum analyzer to acquire the conducted emission measurement. The LISN circuit and requirements are different

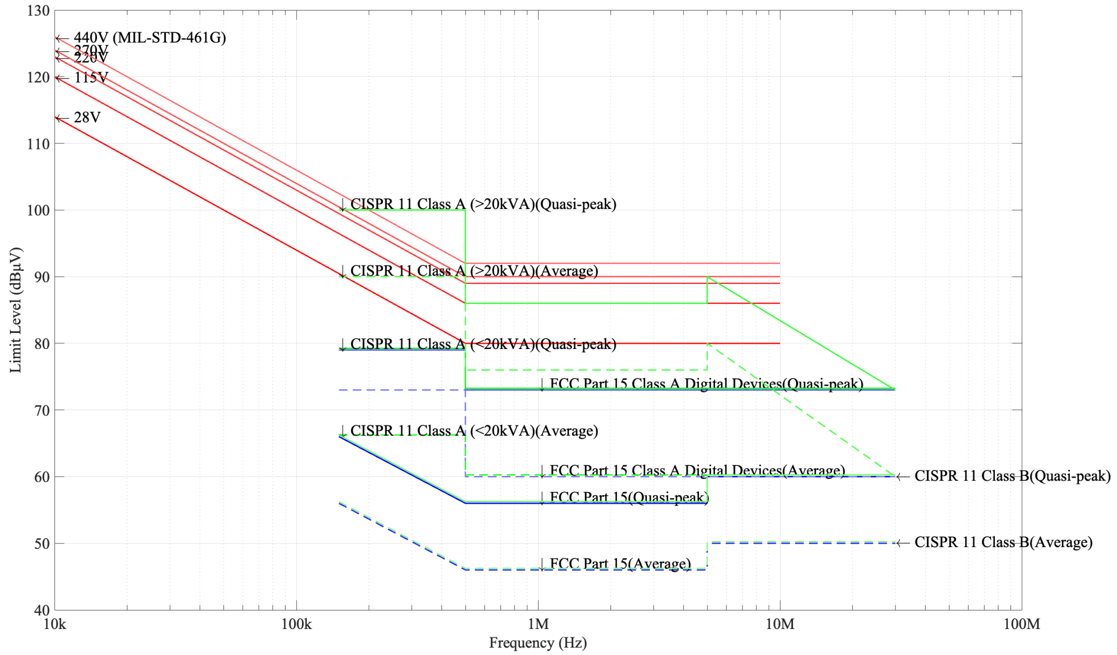


Figure 2.49: EMI Standards comparison

among the categories of EUT, but the difference among standards are minimum. The industrial standards usually cover the 150 kHz to 30 MHz frequency range.

One testing requirement from the industrial standards that is distinct from the military standard, such as MIL-STD, is the detector requirement. The industrial standards, due to the historical evolution of the EMC standards, require a quasi-peak detector and an average for the conducted emission test, while the MIL-STD requires peak detection. Generally speaking, spectral contents' levels are highest with peak detection, lower with quasi-peak, and lowest with average detection. These detectors are all commonly equipped with commercially available EMI receivers and spectrum analyzers.

Military Standard: MIL-STD 461G

MIL-STD 461G [25] is the EMI emission and susceptibility standard for United States military equipment. It covers EMI requirements, including conducted emissions (CE), radiated emissions (RE), conducted susceptibility (CS), and radiated susceptibility (RS). VFD drive designs usually only focus on the CE101 and CE102 when military applications are considered.

Low-Frequency EMI conducted emission: CE101 Instead of a voltage spectrum limit that is commonly required by EMI-conducted emission standards, CE101 sets a power lead current spectral limit that covers the frequency range from 30 Hz to 10 kHz[1] for DC, 60 Hz AC, 400 Hz AC equipment. This compensates for the unregulated frequency range of industrial standards. The emission limit is very similar to the MIL-STD 1399 power quality standard requirement. The measurement method, however, requires the usage of LISNs, which is not required by the PQ standard.

High-Frequency EMI conducted emission: CE102 The high frequency conducted emission requirement of MIL-STD 461G is very similar to what is regulated by industrial standards. CE102 controls the voltage spectral content by its peak measurement value. To protect the spectrum analyzer from excessive EMI levels that are not well mitigated, the measurement is acquired via a 20 dB 50 Ω RF attenuator that is absent from the industrial measurement. Together with CE101, CE102's required frequency range from 10 kHz to 10 MHz fills the unregulated frequency as in industrial standards. MIL-STD 461G handles a frequency higher than 10 MHz with other tests that differs from industrial standards.

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[1] For AC applications, this requirement is applicable starting at the second harmonic of the EUT power frequency.

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Chapter 3

Voltage Source Converter Common-mode Model Development

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3.1 Overview

In this chapter, the common-mode modeling method, the modeling process, and the resulting common-mode equivalent models for essential voltage source converter sections are documented in detail. The essential circuit sections are selected so that the CEM of common voltage source converters and surrounding circuits (*e.g.*, filters, LISNs, load) can be put together exclusively using these modulized sections. The circuit sections included in this study are:

- Generic half-bridge (two switches), Section 3.3
- Generic full-bridge (three-phase, six switches), Section 3.6
- Generic capacitor pair, Section 3.7
- Generic inductor pair, Section 3.4
- Generic three capacitors group, Section 3.3
- Generic three-phase inductor, Section 3.6

3.2 Modeling Methodology

The CEM and DEM baseline concept's mathematical definition is explained in [37]. Generally speaking, any N-line circuit with a common coupling point can be expressed with line currents (i_1, i_2, ... i_N) and line voltages to a designated reference point "P" (v_1, v_2, ... v_n) on individual lines (Fig. 3.1). "P" node is a mathematically arbitrary potential point.

Common-mode voltage and current are defined as:

$$v_{\mathrm{CM}} \triangleq \frac{1}{N}\sum_{n=1}^{N} v_n \tag{3.1}$$

$$i_{\text{CM}} \triangleq \sum_{n=1}^{N} i_n \tag{3.2}$$

Differential-mode voltages are defined as voltage drops between lines $v_{mn} = v_m - v_n$ and differential-mode currents are $i_{mn} = \frac{1}{2}(i_m - i_n)$ as if line *n* is the "return path" of line *m*. With $N - 1$ differential-mode elements and one common-mode element, these definitions can be arranged into an $N \times N$ linear transformation so that the common-mode and differential-mode derivation can be systematically shown as follows.

$$\underbrace{\begin{bmatrix} v_{12} \\ v_{23} \\ \vdots \\ v_{(N-1)N} \\ v_{\text{CM}} \end{bmatrix}}_{\mathbf{v}_{\text{DCM}}} = \underbrace{\begin{bmatrix} 1 & -1 & 0 & \dots & 0 \\ 0 & 1 & -1 & \dots & 0 \\ \vdots & & \ddots & & \vdots \\ 0 & \dots & 0 & 1 & -1 \\ \frac{1}{N} & \frac{1}{N} & \frac{1}{N} & \dots & \frac{1}{N} \end{bmatrix}}_{\mathbf{T}_v} \underbrace{\begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_{N-1} \\ v_N \end{bmatrix}}_{\mathbf{v}_n} \tag{3.3}$$

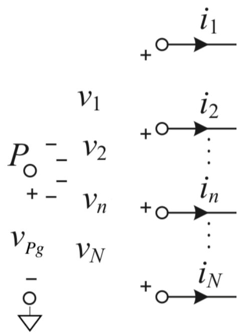

Figure 3.1: A generic N-line circuit

$$\underbrace{\begin{bmatrix} i_{12} \\ i_{23} \\ \vdots \\ i_{(N-1)N} \\ i_{\text{CM}} \end{bmatrix}}_{\mathbf{i}_{\text{DCM}}} = \underbrace{\begin{bmatrix} 1/2 & -1/2 & 0 & \dots & 0 \\ 0 & 1/2 & -1/2 & \dots & 0 \\ \vdots & & \ddots & & \vdots \\ 0 & \dots & 0 & 1/2 & -1/2 \\ 1 & 1 & 1 & \dots & 1 \end{bmatrix}}_{\mathbf{T}_i} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_{N-1} \\ i_N \end{bmatrix}}_{\mathbf{i}_n} \tag{3.4}$$

Left multiplying the inverse matrix of $\mathbf{T}_v$ and $\mathbf{T}_i$, (3.3) and (3.4) become the derivations of mixed-mode voltages and currents from common-mode and differential-mode voltages and currents.

$$\mathbf{v}_n = \mathbf{T}_v^{-1}\mathbf{v}_{\text{DCM}} \tag{3.5}$$

$$\mathbf{i}_n = \mathbf{T}_i^{-1}\mathbf{i}_{\text{DCM}} \tag{3.6}$$

By transforming the mixed-mode voltages and currents, the KVL and KCL expression change, and new equivalent circuits can be drawn from the new expression. The end goal is a mathematical expression that can be interpreted as an equivalent circuit such as the generic example in Figure 3.2, *e.g.* a DEM or a CEM. The generic form of the mathematical expression is:

$$v_x = R_{eq}i_x + L_{eq}\frac{\mathrm{d}i_x}{\mathrm{d}t} + \int C_{eq}i_x\mathrm{d}t + v_{eq} \tag{3.7}$$

where v_{eq} is usually a sum of cross-mode coupling terms. When derived, the section of the circuit can be attached to other sections of the equivalent circuit with the same group of nodes as selected at the ends of the CEM.

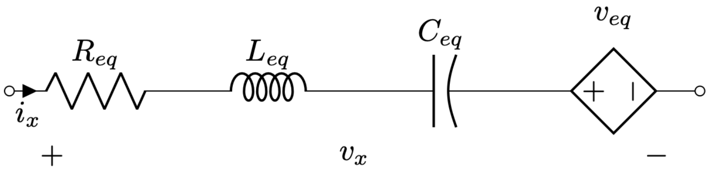

Figure 3.2: A generic equivalent circuit

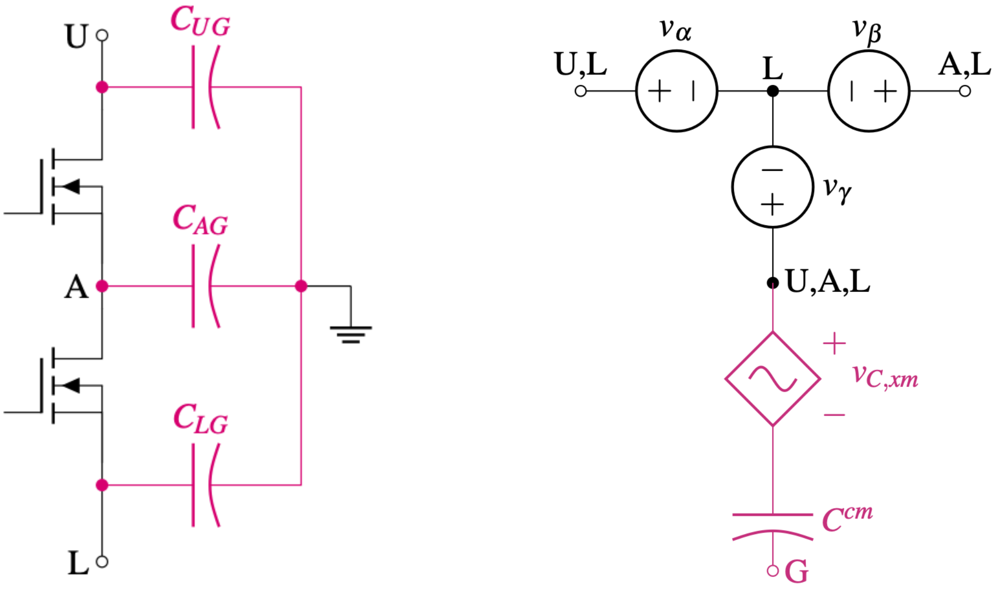

Figure 3.3: Generic half-bridge with three (parasitic) capacitors group (left) and the corresponding CEM (right)

3.3 Generic half-bridge and generic three-capacitor group

In [7], the CEM of a half-bridge and a three capacitor group (Figure 2.7). However, the example shown in Figure 2.7 split the three capacitors into two groups. A more generic three capacitors group CEM can be derived.

As shown in 3.3, the mixed-mode half-bridge circuit is split into two parts, the power switches, and the parasitic capacitor group. The common-mode voltages among the switches can be expressed as follows using similar progress illustrated above.

$$v_\alpha = \frac{1}{2}\left(v_{UL} + v_{LL}\right) = \frac{v_{UL}}{2} \tag{3.8}$$

$$v_\beta = \frac{1}{2}(v_{AL} + v_{LL}) = \frac{v_{AL}}{2} \tag{3.9}$$

$$v_\gamma = \frac{1}{3}(v_{UL} + v_{AL} + v_{LL}) = \frac{1}{3}(v_{UL} + v_{AL}) \tag{3.10}$$

The capacitors group can be expressed in mixed-mode as follows.

$$\begin{bmatrix} V_{UG} \\ V_{AG} \\ V_{LG} \end{bmatrix} = \frac{1}{j\omega} \begin{bmatrix} C_{UG} & 0 & 0 \\ 0 & C_{AG} & 0 \\ 0 & 0 & C_{LG} \end{bmatrix} \begin{bmatrix} I_{UG} \\ I_{AG} \\ I_{LG} \end{bmatrix} \tag{3.11}$$

Similarly, the transformation matrixes can be utilized to extract the common-mode component. The common-mode expressions of the capacitors group (illustrated in `magenta` in Figure 3.3) are listed as follows.

$$v_{C,xm} = -\frac{1}{3}\left(\frac{C_{UG} + C_{AG} - 2C_{LG}}{C_{UG} + C_{AG} + C_{LG}}\right) v_{AL} + \frac{1}{3}\left(\frac{-2C_{UG} + C_{AG} + C_{LG}}{C_{UG} + C_{AG} + C_{LG}}\right) v_{UA} \tag{3.12}$$

$$C^{cm} = C_{UG} + C_{AG} + C_{LG} \tag{3.13}$$

3.4 Generic inductor pair

The generic inductor pair CEM expression can be derived with the following procedure. Name the self-inductance of the two windings L_1 and L_2; the mutual inductance between the windings M. The voltages across each winding can be expressed as follows.

$$\begin{bmatrix} V_{L_1} \\ V_{L_2} \end{bmatrix} = j\omega \begin{bmatrix} L_1 & M \\ M & L_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{3.14}$$

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Transform this equation with the transformation matrixes. The mixed-mode expression is split into a common-mode and a differential-mode expression.

$$\begin{bmatrix} V_L^{dm} \\ V_L^{cm} \end{bmatrix} = j\omega \begin{bmatrix} L_1 + L_2 - 2M & \dfrac{L_1 - L_2}{2} \\ \dfrac{L_1 - L_2}{2} & \dfrac{L_1 + L_2 + 2M}{4} \end{bmatrix} \begin{bmatrix} I^{dm} \\ I^{cm} \end{bmatrix} \tag{3.15}$$

Common-core symmetrical case: In a scenario where inductor designs where the windings are symmetrical and wrapped on an un-gapped core, which means $M = L_1 = L_2 = L_e$. This type of inductor is widely used as a "common-mode choke." Equation (3.15) becomes simplified.

$$\begin{bmatrix} V_L^{dm} \\ V_L^{cm} \end{bmatrix} = j\omega \begin{bmatrix} 0 & 0 \\ 0 & L_e \end{bmatrix} \begin{bmatrix} I^{dm} \\ I^{cm} \end{bmatrix} \tag{3.16}$$

The CEM expression of the common-mode inductor is equal to the inductance of the individual winding.

Symmetrical separate pair: In a scenario where two identical inductors without mutual influence are used, mutual inductance M becomes zero and $L_1 = L_2 = L$. Equation (3.15) becomes the equation as follows.

$$\begin{bmatrix} V_L^{dm} \\ V_L^{cm} \end{bmatrix} = j\omega \begin{bmatrix} 2L & 0 \\ 0 & \dfrac{L}{2} \end{bmatrix} \begin{bmatrix} I^{dm} \\ I^{cm} \end{bmatrix} \tag{3.17}$$

It is clear that the inductor pair provides twice the inductance in differential-mode and half in common-mode.

3.5 Generic 4-pole bridge with discrete SiC

The following material has been published at the Fourth IEEE International Conference on DC Microgrids (IEEE ICDCM 2021) [159].

A 4-pole bridge mixed-mode model in Fig. 3.4 can be split into three groups as shown

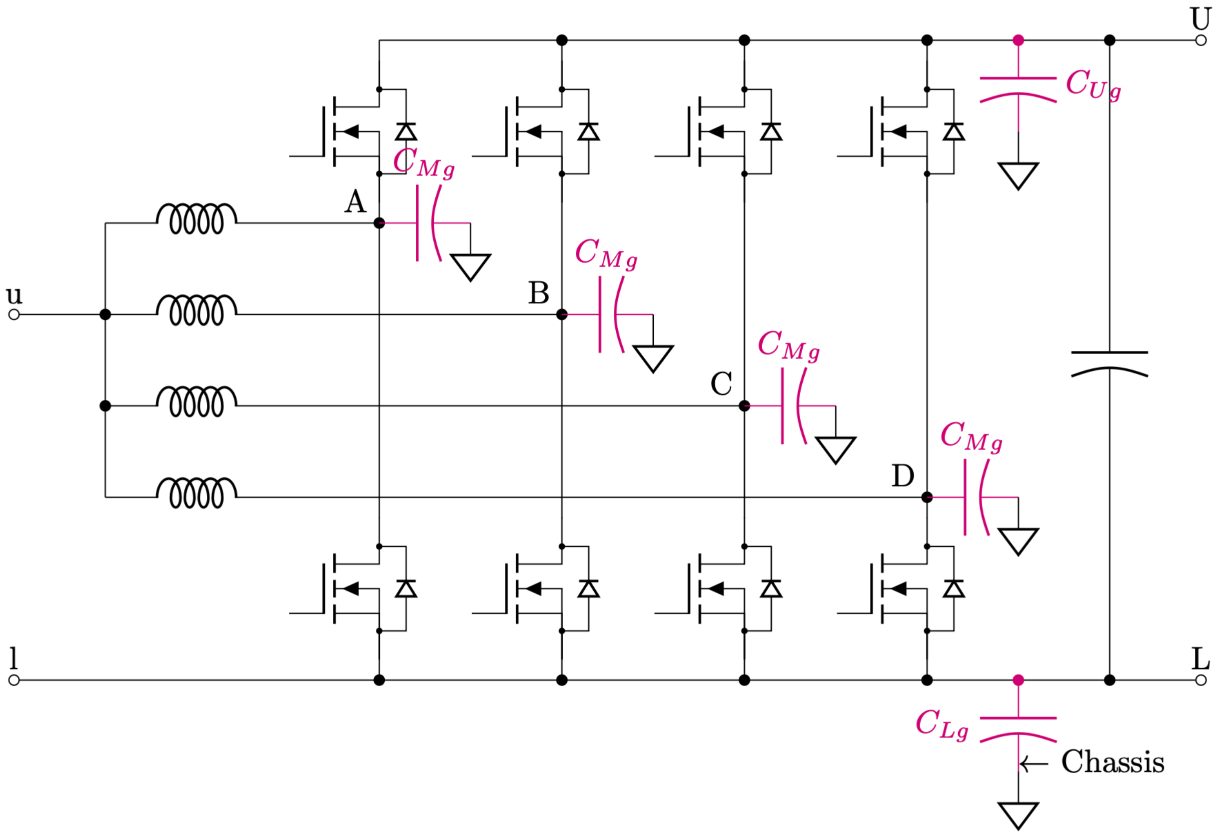

Figure 3.4: Four-pole converter mixed-mode circuit model (The magenta-colored capacitors are the lumped element models for the mutual coupling between the MOSFETs and the converter's chassis. Nodes u and l connect to the low voltage side. U and L connect to the high voltage side.)

in Fig. 3.5. All the MOSFETs are represented with the corresponding voltages between defined circuit points. "P" node is a mathematically arbitrary potential point.

The left group has no direct coupling with the chassis and will not take part in the CEM. The other two parts can be mathematically represented by (3.18) and (3.19). (From this point forward, the time domain current and voltage values are represented in lower case letters i and v; the frequency domain in upper case letters I and V.)

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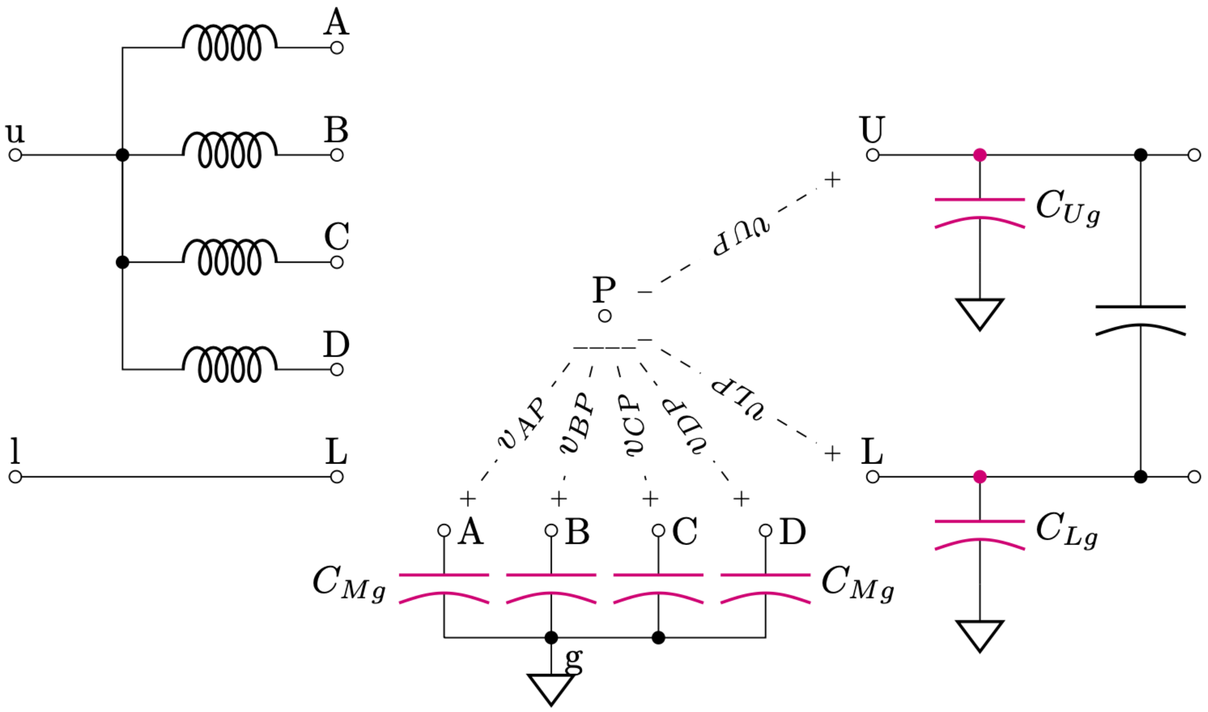

Figure 3.5: Four-pole converter circuit analysis

$$\mathbf{V}_{Pg} + \begin{bmatrix} V_{AP} \\ V_{BP} \\ V_{CP} \\ V_{DP} \end{bmatrix} = \begin{bmatrix} V_{C_{Ag}} \\ V_{C_{Bg}} \\ V_{C_{Cg}} \\ V_{C_{Dg}} \end{bmatrix} \tag{3.18}$$

$$\mathbf{V}_{Pg} + \begin{bmatrix} V_{UP} \\ V_{LP} \end{bmatrix} = \begin{bmatrix} V_{C_{Ug}} \\ V_{C_{Lg}} \end{bmatrix} \tag{3.19}$$

The right side of (3.19) is the voltages across the capacitors C_{Ug} and C_{Lg}, which also satisfy the following.

$$\begin{bmatrix} I_{Ug} \\ I_{Lg} \end{bmatrix} = \frac{1}{j\omega} \begin{bmatrix} C_{Ug} & 0 \\ 0 & C_{Lg} \end{bmatrix} \begin{bmatrix} V_{Ug} \\ V_{Lg} \end{bmatrix} \tag{3.20}$$

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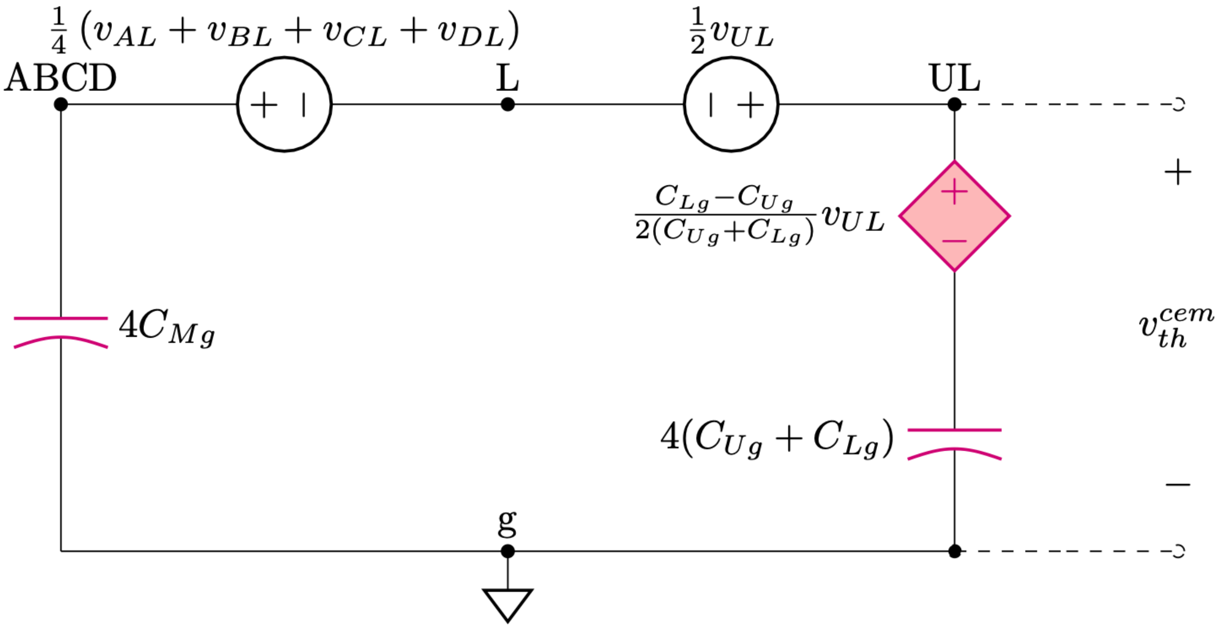

Figure 3.6: Four-pole converter common-mode equivalent circuit

Left multiplying $\mathbf{T}_{i,2}$ to both sides and substituting the voltage with (3.5) results in the following.

$$\begin{bmatrix} I_{DM}^{UL} \\ I_{CM}^{UL} \end{bmatrix} = \frac{1}{j\omega}\mathbf{T}_{i,2}\begin{bmatrix} C_{Ug} & 0 \\ 0 & C_{Lg} \end{bmatrix}\mathbf{T}_{v,2}^{-1}\begin{bmatrix} V_{UL} \\ \frac{1}{2}\left(V_{C_{Ug}}+V_{C_{Lg}}\right) \end{bmatrix} \tag{3.21}$$

The voltages can be solved.

$$\frac{V_{C_{Ug}}+V_{C_{Lg}}}{2} = \frac{I_{CM}^{UL}}{j\omega\left(C_{Ug}+C_{Lg}\right)} + \frac{C_{Lg}-C_{Ug}}{2\left(C_{Lg}+C_{Ug}\right)}V_{UL} \tag{3.22}$$

Left multiplying both sides of (3.19) by $\mathbf{T}_{v,2}$.

$$V_{Pg}+V_{CM}^{UL} = \frac{1}{2}\left(V_{C_{Ug}}+V_{C_{Lg}}\right) \tag{3.23}$$

Substituting (3.23) with (3.22), the common-mode component of the right section of Fig. 3.6 results in the following.

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$$V_{Pg} + V_{CM}^{UL} = \frac{I_{CM}^{UL}}{j\omega\left(C_{Ug} + C_{Lg}\right)} + \frac{C_{Lg} - C_{Ug}}{2\left(C_{Lg} + C_{Ug}\right)} V_{UL} \tag{3.24}$$

Since capacitors in (3.18) have identical capacitor values, the common-mode component is not difficult to extract.

$$V_{Pg} + V_{CM}^{ABCD} = I_{CM} \frac{1}{j\omega(4C_{Mg})} \tag{3.25}$$

The $\frac{I}{j\omega C}$ parts of (3.24) and (3.25) can be modeled as capacitors with corresponding values. Setting "P" at existing circuit node "L", *i.e.*, defining $v_{Pg} = v_{Lg}$, the CM currents can be expressed with measurable voltages.

$$V_{CM}^{ABCD} = \frac{1}{4}\left(V_{AL} + V_{BL} + V_{CL} + V_{DL}\right) \tag{3.26}$$

$$V_{CM}^{UL} = \frac{1}{2} V_{UL} \tag{3.27}$$

The common-mode component (Fig. 3.6) is now extracted from the mixed-mode circuit (Fig. 3.5) of the four-pole converter such that all voltage values are measurable on the hardware. This derived CEM presents an accurate model of the converter's common-mode noise source.

3.6 Generic three-phase full bridge and generic three-phase inductor

The following section covers material accepted to publish and present in the Thirty-eighth Annual IEEE Applied Power Electronics Conference (APEC 2023). [160] It covers the derivation of a generic three-phase full bridge and a generic three-phase inductor in *a realistic applicational scenario*, where a three-phase VSI is utilized as a VFD operating with a $\mathrm{d}v/\mathrm{d}t$ filter.

Similarly with the half-bridge case, the dominating parasitic identified in the full-bridge VSI assembly is the capacitances between the drain of the upper MOSFET and the module chassis C_{UG}, mid-point of the module and the module chassis C_{AG}, and source of the lower MOSFET and the module chassis C_{LG}, as shown in Fig. 3.3. By grouping the three C_{UG} and C_{LG} from three paralleled switching modules, the parasitics can be expressed in the mixed-mode circuit as the pink shaded area in Fig. 4.8.

CEM derivation of this unfiltered inverter assembly is similar to what was described in [159] with a DC-DC voltage source converter. The resulting CEM model can be seen in Fig. 3.8 between the CEM node "U,L" and "A,B,C". Details of the inverter CEM are listed in Table 3.2, where all the voltages in the expressions are measurable from the hardware. It is worth noticing that the two sets of capacitances $3C_{UG}$ and $3C_{LG}$ on the DC-side, this capacitance asymmetry will result in a cross-mode coupling expressed as follows.

$$v_{Cxm} = \frac{C_{LG} - C_{UG}}{2\left(C_{LG} + C_{UG}\right)} v_{UL} \tag{3.28}$$

This cross-mode coupling is non-trivial to the CM behavior of the system. An example of this cross-mode coupling effect can be seen in hardware analysis (Fig. 4.12 and 4.13).

3.6.1 Three-phase inductor

The common-core inductor sometimes has an inherent semi-symmetric structure (*e.g.*, EE-core, IE-core). Utilizing the magnetic equivalent circuit (MEC) (Fig. 3.7), the inductance expression can be found. For clarity of expression, this study simplifies the MEC to focus on the two main inductances of the EE-core inductor: the inductance due to the common-core structure mutual coupling L_M and each winding's independent inductance L_{ind}. L_M is generally driven by core reluctance and gap reluctance. Since inductor optimization is not within the scope of this study, the reluctance of the different core sections and air gaps are expressed as the sum of the three branches. Assuming the inductor operates

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Table 3.1: $\mathbf{L}_M$ matrix detail

Matrix Term	Expression
L_{aa}, L_{cc}	$\dfrac{N^2}{\mathcal{R}_e + \frac{\mathcal{R}_c \mathcal{R}_e}{\mathcal{R}_c + \mathcal{R}_e}}$
L_{ab}, L_{cb}	$-\dfrac{1}{2} \dfrac{N^2}{\mathcal{R}_c + \frac{\mathcal{R}_e}{2}}$
L_{ac}, L_{ca}	$-\dfrac{\mathcal{R}_c}{\mathcal{R}_c + \mathcal{R}_e} \dfrac{N^2}{\mathcal{R}_e + \frac{\mathcal{R}_e \mathcal{R}_c}{\mathcal{R}_e + \mathcal{R}_c}}$
L_{ba}, L_{bc}	$-\dfrac{\mathcal{R}_e}{\mathcal{R}_c + \mathcal{R}_e} \dfrac{N^2}{\mathcal{R}_e + \frac{\mathcal{R}_c \mathcal{R}_e}{\mathcal{R}_c + \mathcal{R}_e}}$
L_{bb}	$\dfrac{N^2}{\mathcal{R}_c + \frac{\mathcal{R}_e}{2}}$

without core saturation, in Fig. 3.7, the total reluctance on two ends is noted with $\mathcal{R}_e$, the center total reluctance, $\mathcal{R}_c$. L_{ind} is mostly affected by self-leakage reluctance $\mathcal{R}_{sle}$ and $\mathcal{R}_{sle}$. Assuming equal winding turns per phase, the inductance matrix of $\mathbf{L}_M$ can be expressed as follows (details in Table 3.1).

$$\mathbf{L}_M = j\omega \begin{bmatrix} L_{aa} & L_{ab} & L_{ac} \\ L_{ba} & L_{bb} & L_{bc} \\ L_{ca} & L_{cb} & L_{cc} \end{bmatrix} \tag{3.29}$$

By naming k_1 the asymmetry factor between the end-windings and center winding due to the core geometry ($\mathcal{R}_e = k_1 \mathcal{R}_c$), and k_2 the asymmetry factor between the end-windings and center winding in self-leakage inductance ($\mathcal{R}_{sle} = k_2 \mathcal{R}_{slc}$), the inductance matrix can be further simplified, and a more manageable MM KVL expression of the inductor is shown as follows.

$$\begin{bmatrix} V_{L,a} \\ V_{L,b} \\ V_{L,c} \end{bmatrix} = \left(L_M \begin{bmatrix} \frac{(1+k_1)}{2} & -\frac{1}{2} & -\frac{k_1}{2} \\ -\frac{1}{2} & 1 & -\frac{1}{2} \\ -\frac{k_1}{2} & -\frac{1}{2} & \frac{(1+k_1)}{2} \end{bmatrix} + \mathbf{L}_{ind} \right) j\omega \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{3.30}$$

where the $V_{L,x}$ are the voltages across the windings, and the independent inductance

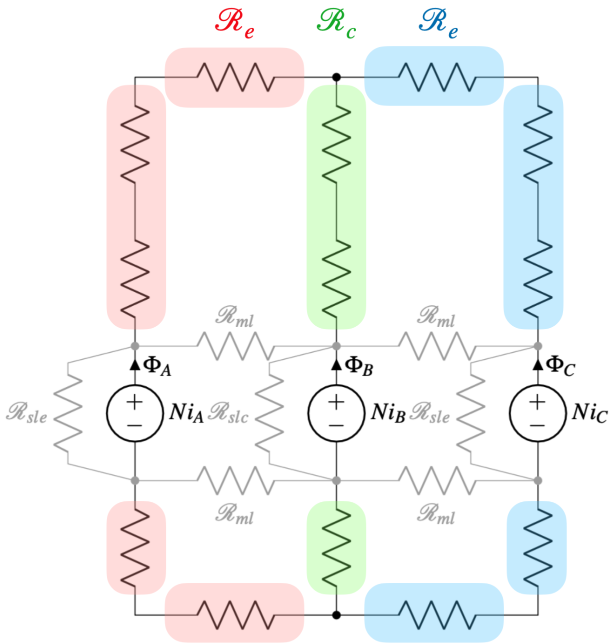

Figure 3.7: Magnetic equivalent circuit

matrix $\mathbf{L}_{ind}$ can be written as follows.

$$\mathbf{L}_{ind} = L_{ind} \begin{bmatrix} k_2 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & k_2 \end{bmatrix} \tag{3.31}$$

Applying the transformation matrixes $\mathbf{T}_v$ and $\mathbf{T}_i^{-1}$ to (3.30), the CM voltage expression of the EE-core inductor can be written as follows.

$$V_L^{cm} = j\omega L_{ind}^{cm} I_L^{cm} + V_{Lxm} \tag{3.32}$$

where $L_{ind}^{cm} = \frac{k_2}{k_2+2} L_{ind}$ and $V_{Lxm} = \frac{k_2(k_2-1)}{3(k_2+2)} \left(V_L^{ab} - V_L^{bc}\right)$. Here the differential voltage across the inductor follows the definition: $V_L^{mn} = V_{L,m} - V_{L,n}$ and . Note that L_M of the EE-core inductor does not contribute to the CM voltage of the inductor. If the $\mathrm{d}v/\mathrm{d}t$ inductor uses a separate-core structure, L_{ind} is the inductance of each inductor winding, and L_M in (3.30) becomes zero.

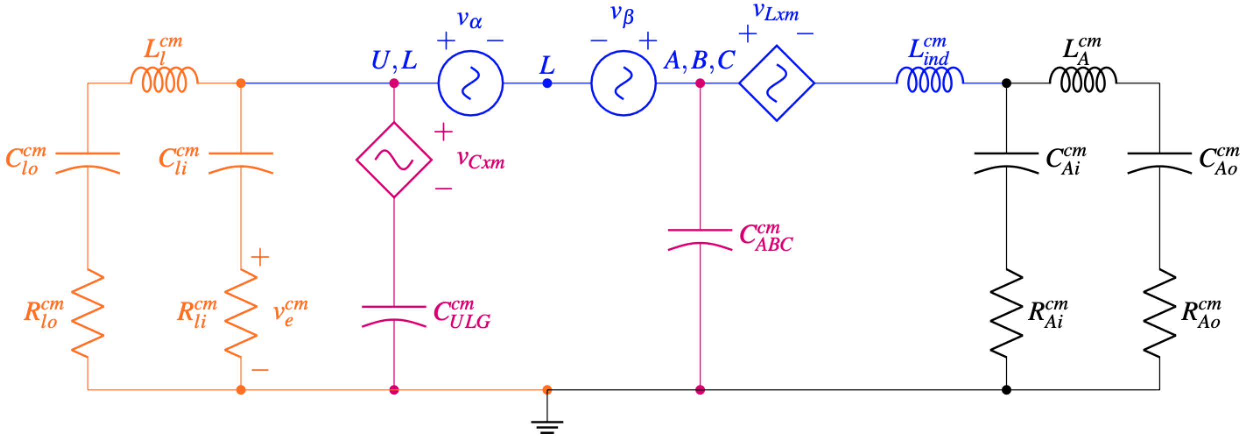

Figure 3.8: CEM

The resulting CEM of the inductor is presented in Fig. 3.8 after node "A,B,C" in blue. The system CEM has diamond-shaped voltage sources v_{Cxm} and v_{Lxm} representing the DM to CM cross-mode coupling expressed in (3.28) and (3.32). The other sources are formed with source-drain voltages across MOSFETs and DC-link voltage. These voltages are utilized later with measured in-situ waveforms to avoid inaccuracy in MOSFET behavior models. Table 3.2 contains all the detailed expressions of elements in Fig. 3.8.

3.7 Generic capacitor pair

The capacitor pair CEM derivation can be seen in Section 3.5 and 3.6. The key expression is (3.28).

3.8 Simulation validation

To validate the mathematical derivations of CEMs, computer simulations are utilized to compare the voltages and currents between the mixed-mode models and their corresponding CEMs. The mixed-mode models (such as those in Fig. 4.8) and their cor-

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Table 3.2: CEM detail expressions

CEM element	Expression
Inverter assembly	
C_{ULG}^{cm}	$3\left(C_{LG}+C_{UG}\right)$
C_{ABC}^{cm}	$3C_{AG}$
v_{Cxm}	(3.28)
v_{α}	$\frac{1}{2}v_{UL}$
v_{β}	$\frac{1}{3}\left(v_{AL}+v_{BL}+v_{CL}\right)$
Inductor	
v_{Lxm}	$V_{Lxm}=\dfrac{k_2(k_2-1)}{3\left(k_2+2\right)}\left(V_L^{ab}-V_L^{bc}\right)$
L_{ind}^{cm}	$\dfrac{k_2}{k_2+2}L_{ind}$
LISN	
L_l^{cm}	$\frac{1}{2}L_l$
C_{lo}^{cm}	$2C_{lo}$
C_{li}^{cm}	$2C_{li}$
R_{lo}^{cm}	$\frac{1}{2}R_{lo}$
R_{li}^{cm}	$\frac{1}{2}R_{li}$
v_e^{cm}	$\frac{1}{2}\left(v_{e1}+v_{e2}\right)$
Artificial Network	
L_A^{cm}	$\frac{1}{3}L_A$
C_{Ao}^{cm}	$3C_{Ao}$
C_{Ai}^{cm}	$3C_{Ai}$
R_{Ao}^{cm}	$\frac{1}{3}R_{Ao}$
R_{Ai}^{cm}	$\frac{1}{3}R_{Ai}$

responding CEMs (such as those in Fig. 3.8) are established in one PLECS simulation environment with details (such as Table 4.1 and 3.2).

For example, in the three-phase full-bridge case, the voltage sources in the CEM are simultaneously fed from the MM model voltages, which have been mathematically manipulated as described in Table 3.2. The simulated VSI is operating at 450 V, 0.8 modulation index, 100 kHz switching frequency, 60 Hz modulated frequency, and 100 kW output. The values of k_1, k_2, L_M, and L_{ind} used through the testing are shown in the TCI section of Table 4.2.

The simulation environment also includes an EMI evaluation environment, where a set of LISNs are utilized as EMI quantification points, and a set of customized artificial

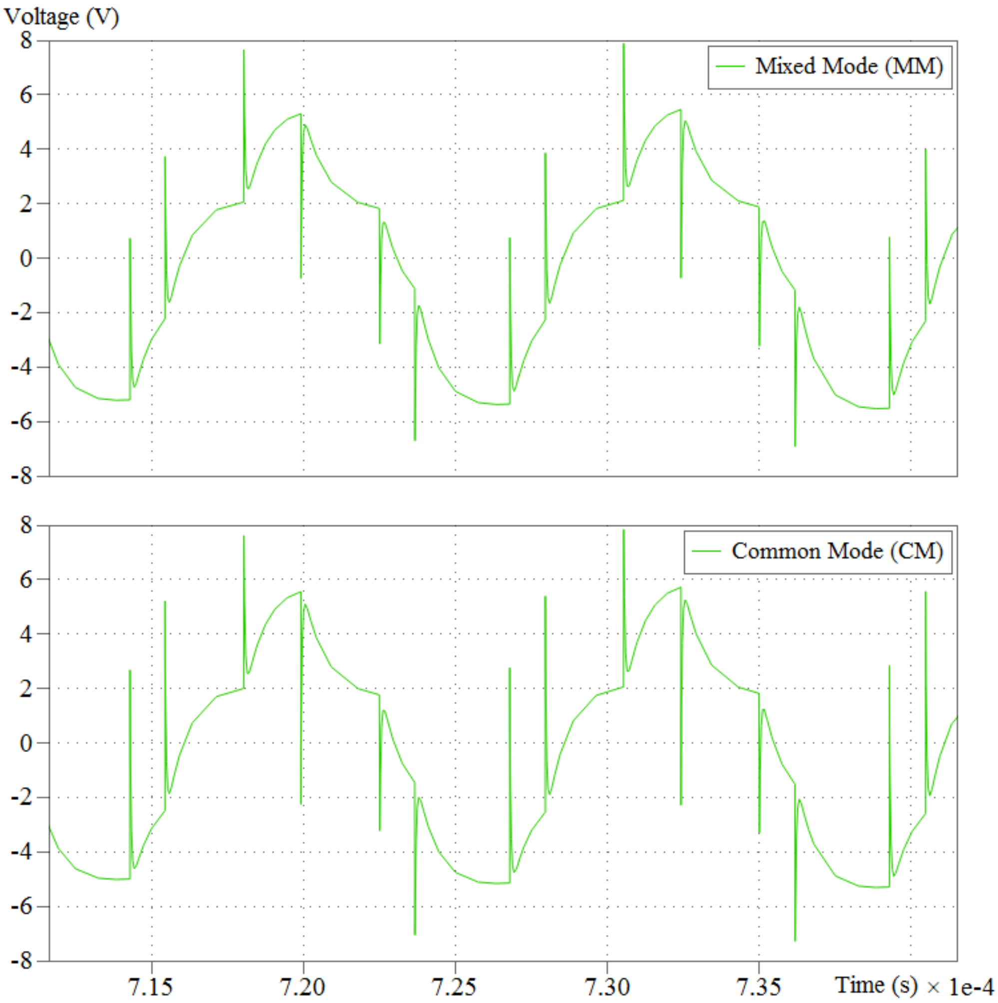
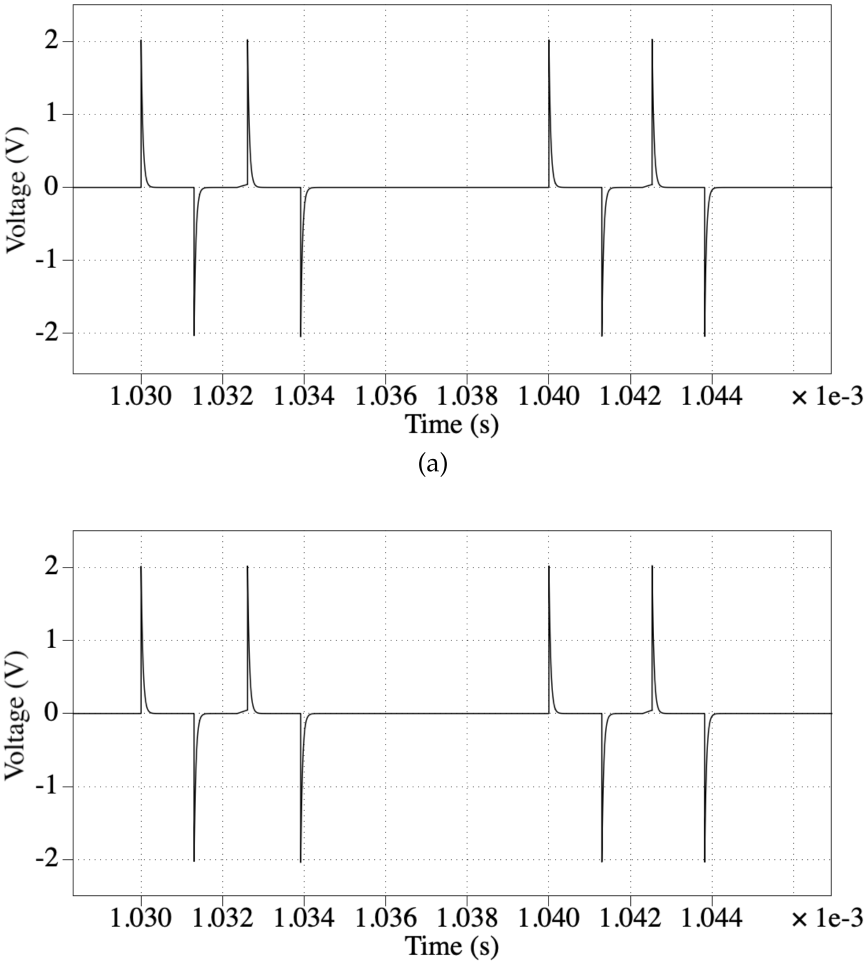


Figure 3.9: Simulated model validation v_e^{cm} (three-phase VSI)

networks are implemented to mimic the load impedance and load parasitics. Because those supporting circuits are all symmetrical, the CEM derivation is very straightforward and not included in this dissertation. The CM LISN measurement $\frac{1}{2}\left(v_{e1}+v_{e2}\right)$ from both the MM model and CEM are compared to validate the derived CEM. The comparison (Fig. 3.9) shows a close-to-identical result and hence verifying the derivation of the CEM.

Another verification example can be seen in (Fig. 3.10) for the four-pole converter CEM from Section 3.5. The comparison is made with the output CM output currents from both models.



(a)

(b)

Figure 3.10: Simulation model validation (four-pole converter) (a) sum of mixed-mode output current; (b) common-mode output current

Chapter 4

Voltage Source Converter Common-mode Model Validation

4.1 Validation of developed CM emission models in applicational scenarios

This section documents the hardware validation of all the CM models developed in Chapter 3. Two applicational scenarios were utilized: a four-pole DC-DC voltage source converter in a battery management unit and a three-phase VSI in a variable-frequency drive (VFD). Besides the CEMs of a one-phase (DC to DC) bridge and a three-phase full bridge, the CEM sections of the capacitor pair, three-capacitor group, inductor pair, and three-phase inductor are being utilized and validated. Validation environment development details are documented in Appendix A.

4.1.1 Battery management four-pole DC-DC converter (buck/boost)

The following material has been published at the Fourth IEEE International Conference on DC Microgrids (IEEE ICDCM 2021) [159].

The designed four-pole bi-direction DC to DC converter under study in this paper serves as a battery management system for a DC microgrid. It acts as a boost converter when the battery is discharging and a buck converter when the battery is being charged. The four-pole converter consists of eight discrete SiC MOSFETs (Cree C3M0030090K) (Fig. 4.2, 3.4). In operation, the low voltage side connects to a 200 V battery, and the high voltage side connects to a 400 V DC grid through proper filters. The four poles have evenly interleaved gating signals switching at 100 kHz, creating a maximum fundamental noise frequency of 400 kHz (Fig. 4.4) (Switching schemes vary in different operational conditions). In battery charging mode, the four-pole converter acts as a buck converter; in power supply mode, a boost converter. Utilizing the high switching frequency enabled by the wide-bandgap (WBG) devices allows a very power-dense design. However, the common-mode noise introduced by the high edge rate can be a nuisance not only to the converter itself but also to the surrounding system (Fig. 4.1). The physically compact

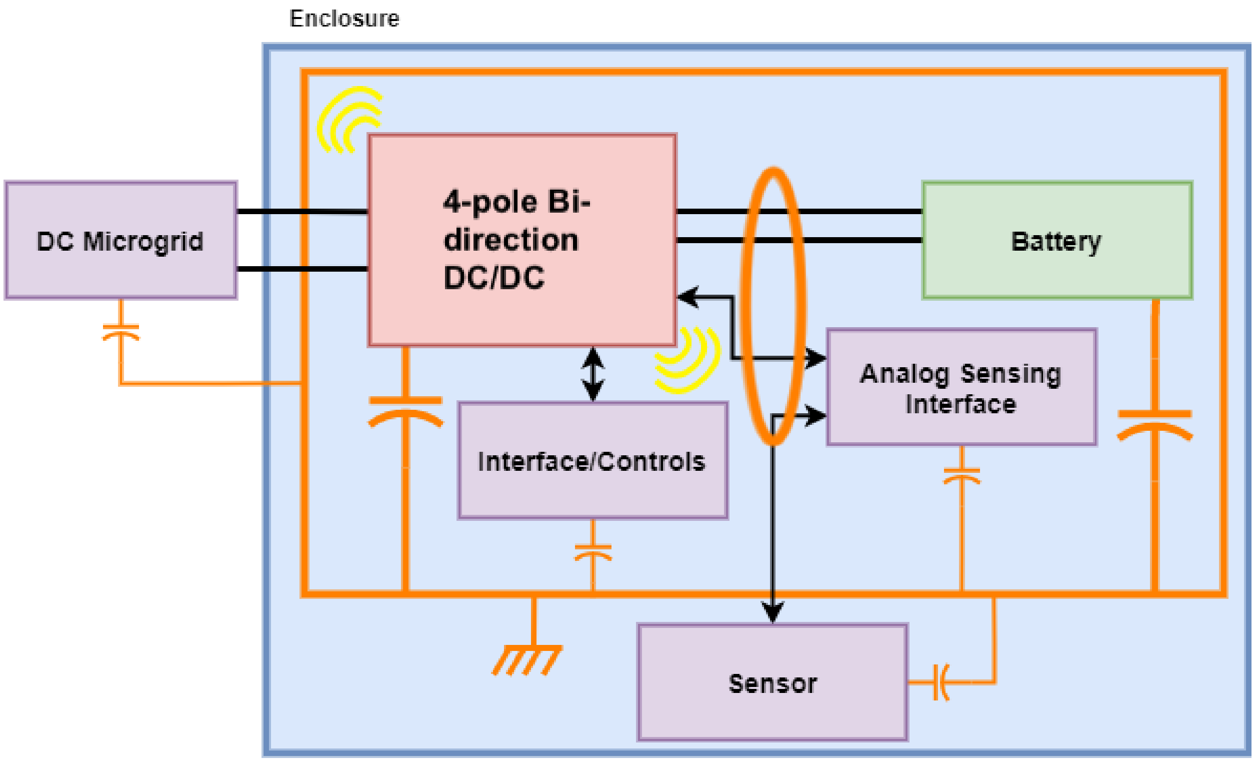


Figure 4.1: Battery management systems with common-mode noise paths (capacitances colored in orange marks where mutual coupling exist)

design also brings new restrictions to the electromagnetic interference (EMI) filter size. Identifying the common-mode noise is essential for filter design and optimization, enclosure design, and potential troubleshooting when intra-system and inter-system incompatibilities occur.

The dominating parasitics identified in the hardware under study in this paper are similar to the demonstration in [7]. As shown in Fig. 4.3, the authors of this paper modeled the mutual coupling between the SiC MOSFET and the converter chassis as C_{Dg} and C_{Sg}. C_{Sg} is negligible since the tab drain on the installed discrete SiC MOSFET covers most areas between the MOSFET and the chassis. However, the circuit analysis in this paper still keeps C_{Sg} as a variable to present a more generic derivation.

The circuit in Fig. 3.4 combines the capacitances from all eight MOSFETs into six equivalent capacitances, where $C_{Mg} = C_{Dg} + C_{Sg}$, $C_{Ug} = 4C_{Dg}$ and $C_{Lg} = 4C_{Sg}$.

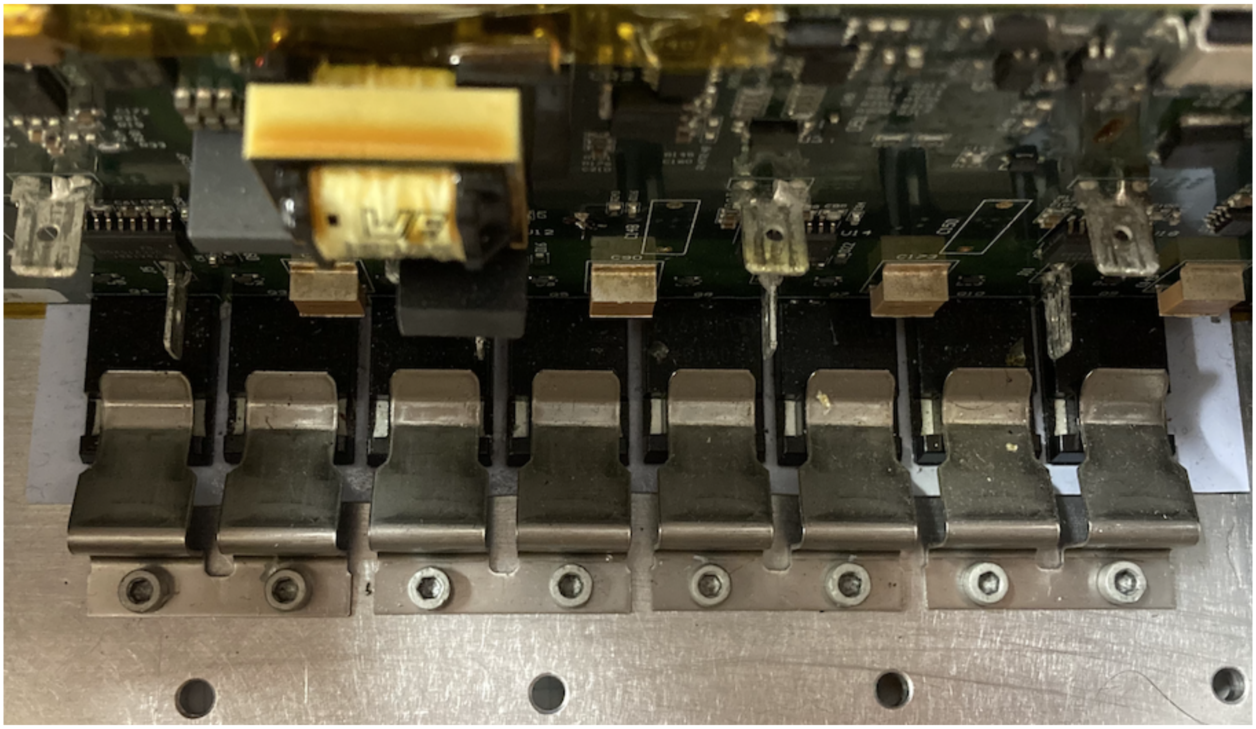


Figure 4.2: Eight SiC MOSFETs composing the four-pole bridge

Hardware data of the four-pole converter was taken from the EMI characterization platform to provide EMI baseline and insertion loss calculations. Based on the information provided by the methodology presented above, a common-mode EMI filter design is also proposed to reduce the common-mode component of EMI.

The unfiltered four-pole boost converter is placed in a testing environment shown in Fig. 4.6. The low voltage side is attached to a charged 200 V battery bank. The high-voltage side is connected to a resistive load bank through a pair of custom-made LISNs. The load bank is configured to draw 5 kW of power from the battery.

The voltages measured to support the CEM analysis are v_{AL}, v_{BL}, v_{CL}, v_{DL}, and v_{UL} from the converter (Fig. 3.4 and A.5). The parasitics are estimated as $C_{Dg} = 90$ pF and $C_{Sg} = 5$ pF.

The EMI measurement is defined as the voltage across R_{ib} in one of the LISNs. However, to extract the common-mode component of the EMI, both R_{ib} need to be measured.

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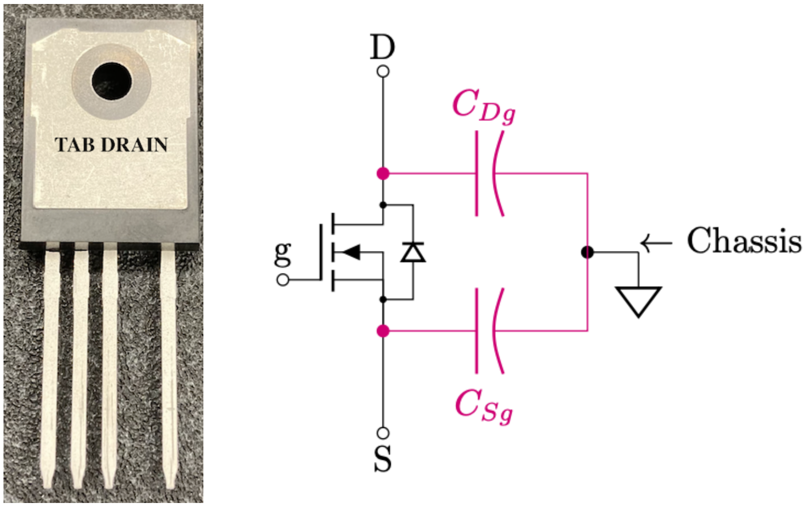

Figure 4.3: A discrete SiC MOSFET and the Dominating Parasitics inducing common-mode EMI (Note that the metal tab (drain) covering most of the base of the MOSFET.)

The common-mode component of the total mixed-mode EMI is defined as follows.

$$v_{emi}^{cm} \triangleq \frac{1}{2}\left(v_{emi1} + v_{emi2}\right) \tag{4.1}$$

This is also the voltage across R_{ib}^{cem} in the CEM. Running the measured voltage waveforms through the rapid frequency-domain solver, v_{emi}^{cem} from Fig. 4.7 can be obtained. The result is shown in Fig. 4.5. The two voltage measurements from LISNs are also measured for modeling validation. The comparison between prediction and measurement shows that the CEM is highly accurate below 30 MHz.

4.1.2 Unfiltered full-bridge inverter as DC-grid tied three-phase variable frequency drive

The following section contains material that is accepted to be presented at the Thirty-eighth Applied Power Electronics Conference (APEC 2023). [160]

Common-mode conducted EMI mitigation plays a significant role in the EMC design of power electronic converters utilizing WBG power modules and devices [161]. One common practice is to place an EE-core motor protection inductor ($\mathrm{d}v/\mathrm{d}t$ inductor) be-

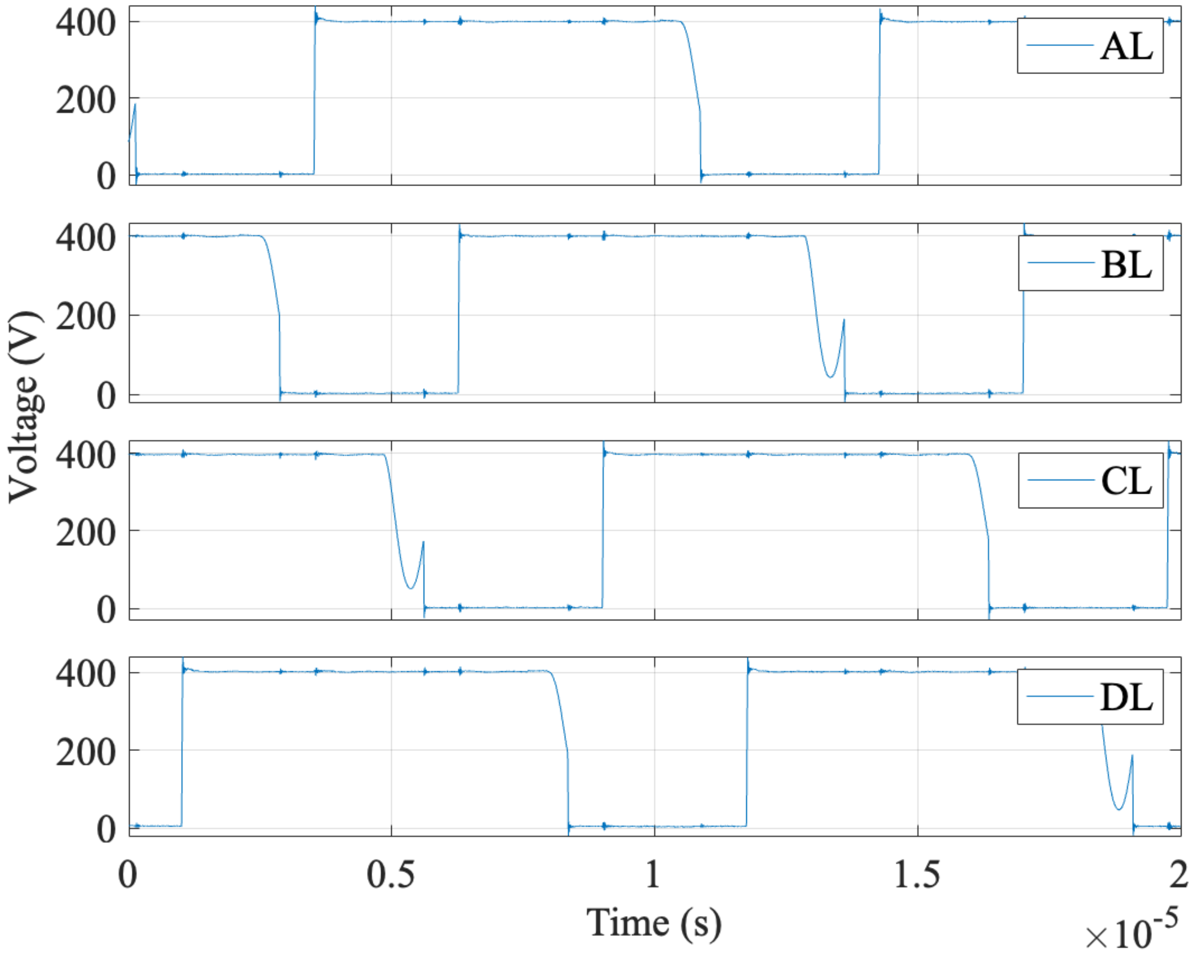

Figure 4.4: Four-pole converter switching waveforms (voltages across lower switches)

tween the AC output of the VFD inverter and the motor to reduce the reflective wave phenomenon in long motor cables [162,163]. If previously IGBT-based VFDs are replaced with VFDs utilizing WBG devices, such as SiC MOSFET modules, reflected wave sensitivity would occur with much shorter cable lengths. This concern over shorter cable lengths is a by-product of the increased efficiency of switching inherent to WBG devices, making the use of a $\mathrm{d}v/\mathrm{d}t$ filter increasingly common [56]. Although the $\mathrm{d}v/\mathrm{d}t$ filter is principally a differential-mode filter, it has also recently been recognized that the combination of $\mathrm{d}v/\mathrm{d}t$ filter with either AC- or DC-side CM inductance plays a role in reducing CM circulating current to the motor [56,67,164]. Various methodologies have been de-

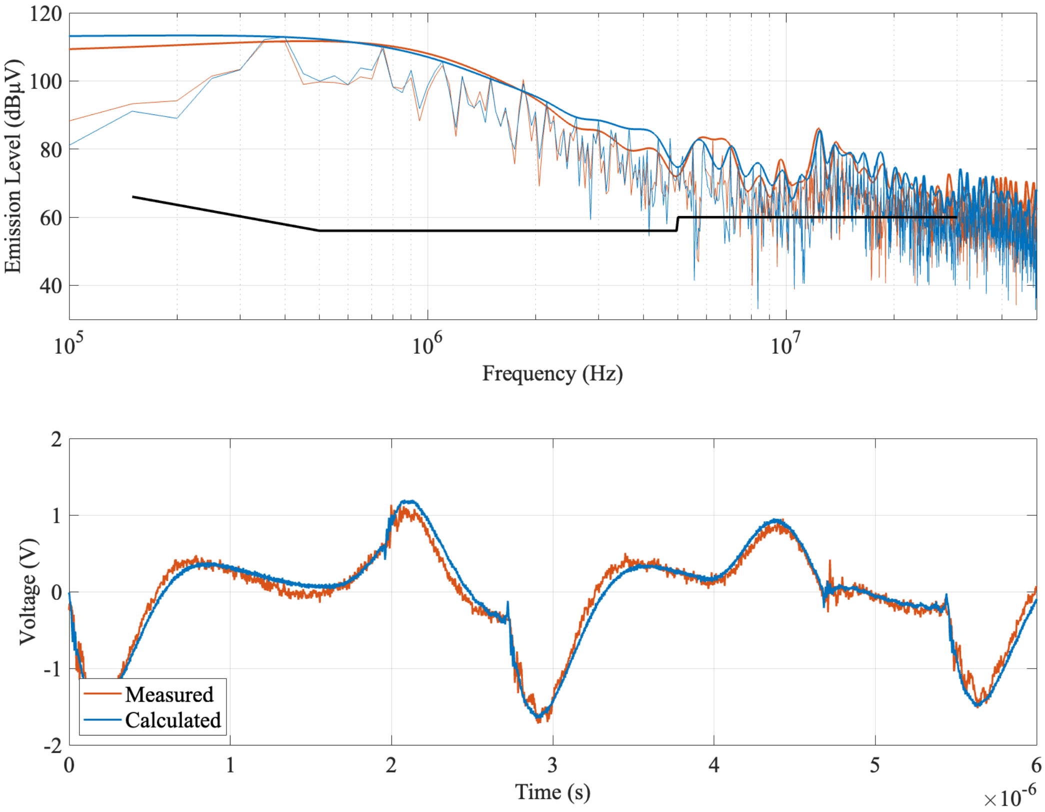

Figure 4.5: Unfiltered four-pole converter's rapid EMI measurement prediction vs. real-time LISN measurement (common-mode component) (black line is CISPR 32 Class B quasi-peak limit line [20])

veloped over recent years to achieve more accurate and efficient CM modeling in order to more effectively mitigate CM noise, which is the principal source of conducted EMI in the spectral range below 10MHz [30, 159, 165].

The parasitic capacitance between the three-phase voltage source inverter (VSI) and its chassis, the asymmetrical structure of the EE- or EI- core inductor, motor cable shielding, and the motor parasitics together form a complex path for CM current to circulate in the motor-drive system (Fig. 4.15). This study focuses on an unfiltered system that is rated 480 V and 100 hp.

Besides the WBG-enabled high switching frequencies and high $\mathrm{d}v/\mathrm{d}t$ waveforms, dom-

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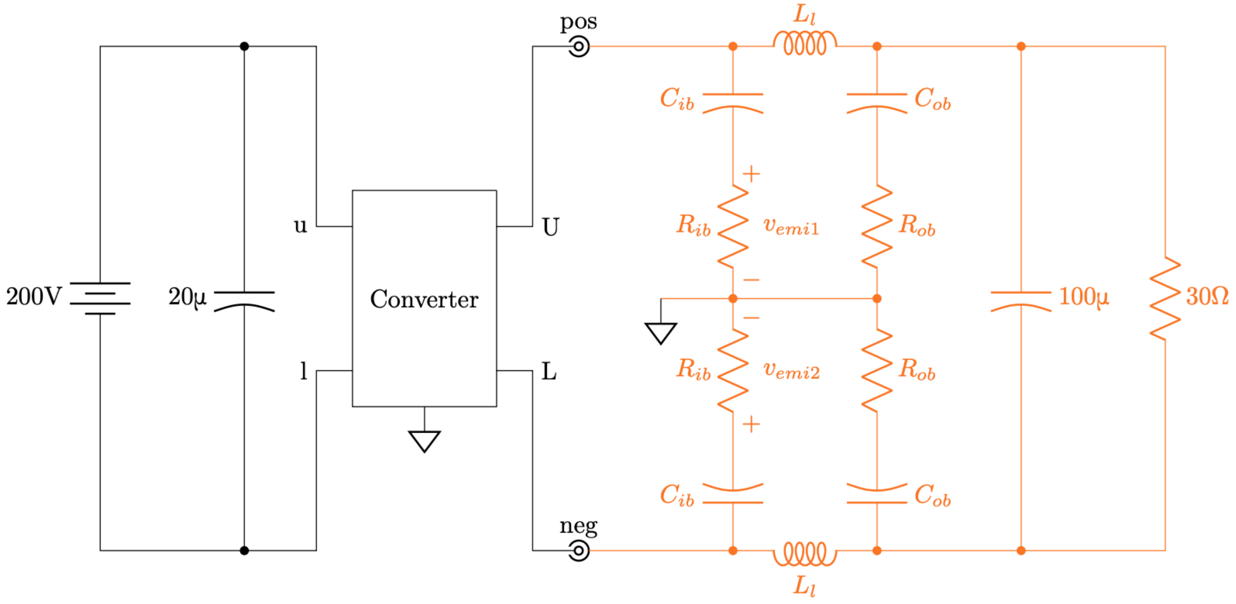

Figure 4.6: Unfiltered four-pole converter under EMI characterization (mixed-mode model) (The converter circuit is simplified in this schematic.)

inating circuit parasitics, *e.g.* parasitic capacitance within the multi-chip power modules are also identified as the dominating source of EMI emission [161] and included in the lumped-element circuit models. The dominating parasitic identified in the full-bridge VSI assembly is the capacitances between the drain of the upper MOSFET and the module chassis C_{UG}, mid-point of the module and the module chassis C_{AG}, and source of the lower MOSFET and the module chassis C_{LG}. By grouping the three C_{UG} and C_{LG} from

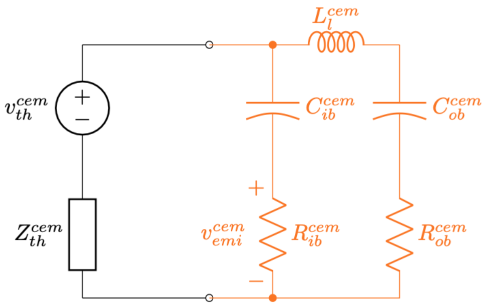

Figure 4.7: Unfiltered four-pole converter under EMI characterization (CEM) (The black part is the Thévenin equivalent circuit of the CEM circuit shown in Fig. 3.6.)

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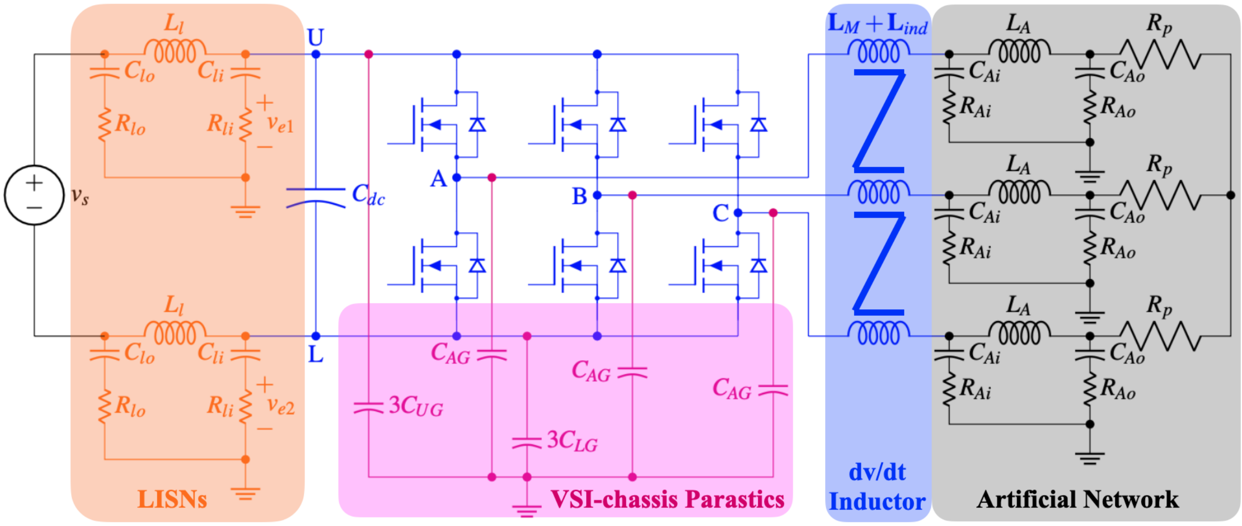

Figure 4.8: Mixed-mode circuit of the system under study

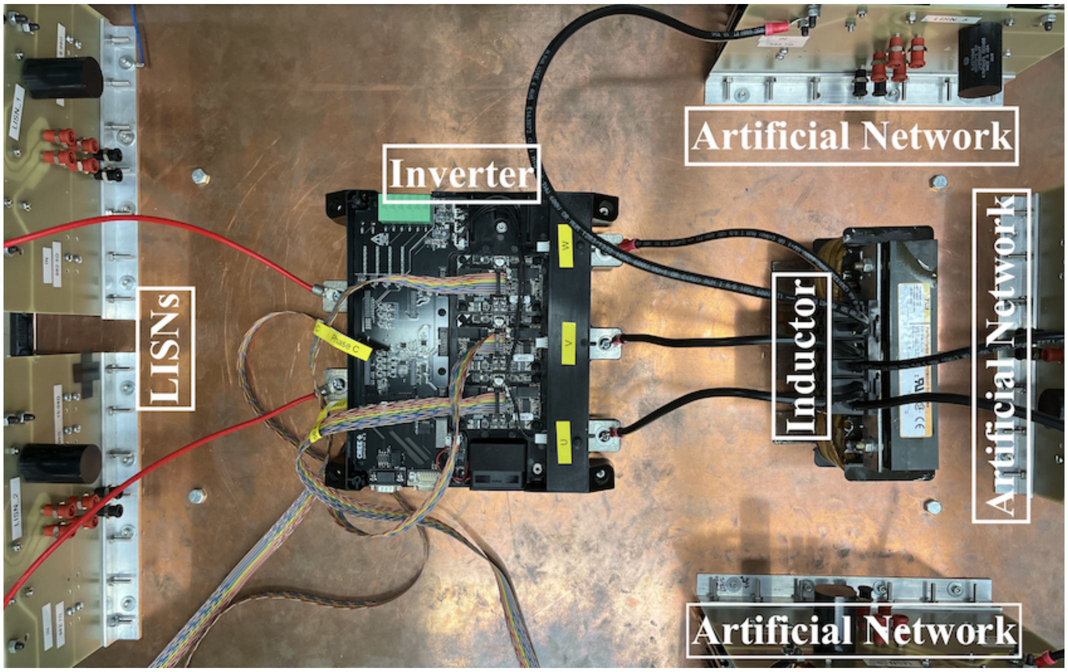

Figure 4.9: Equipment under test and the testbed

three paralleled switching modules, the parasitics can be expressed in the mixed-mode circuit as the pink shaded area in Fig. 4.8.

The CEM model derivation is described in detail in 3.6.

The VSI used in this study is a Wolfspeed CRD300DA12E-XM3 that contains three 1.2

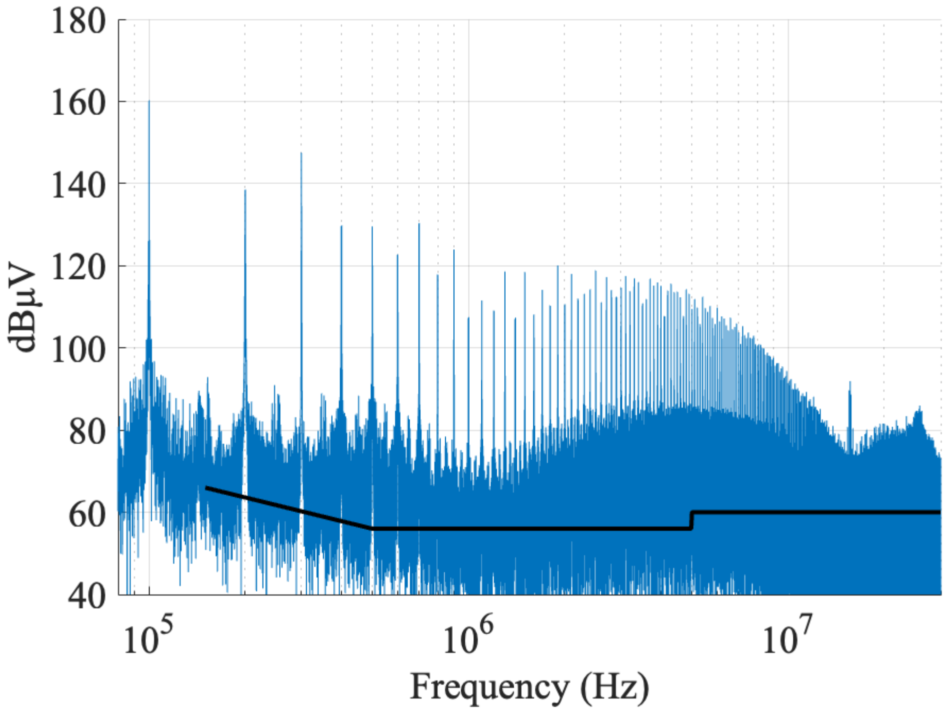

Figure 4.10: EMI measurement in CM (Unfiltered inverter only) (CISPR 11 class B [21] average reference line in black)

kV, 450 A SiC power modules. The VSI is operated with a 450 V dc bus, 0.8 modulation index, 100 kHz switching frequency, 60 Hz modulated frequency, and 10 kW output power. Due to equipment limitation, higher power output condition is not included in this study. However, the main driver of the CM current is not the fundamental frequency ac current but the voltage waveforms, which vary minimally between different load conditions. The testing environment is customized to support model validation and EMI characterization. The essential voltage waveforms are measured simultaneously (16 channels in-sync) utilizing two synchronized Tektronix MSO58 Oscilloscopes with HVDP0200 high voltage differential probes. The EMI test bed (Fig. 4.9) is custom-made, and all the essential impedances of the testbed are calibrated with impedance analyzers. This testbed contains a set of line impedance stabilization networks (LISN) that can be modified to match the requirement of different standards (shown in orange in Fig. 4.8, Fig. 3.8). These custom-made LISNs are able to perform while sustaining high power noise generated by

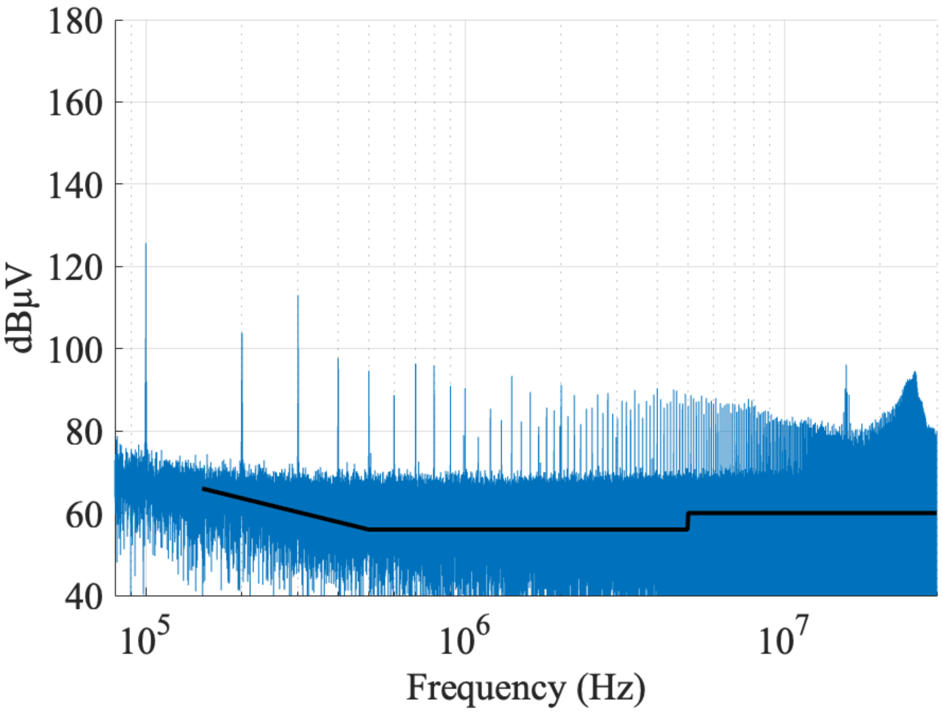

Figure 4.11: EMI measurement in DM (Unfiltered inverter only)

an unfiltered power converter operating at high switching speeds (80 kHz to 100 kHz), resulting in high $\mathrm{d}v/\mathrm{d}t$. The in-situ waveforms (*e.g.* source-drain voltages) which constitute the voltages that result in the voltage sources within the CEM (*e.g.* v_α, v_β, v_{Lxm}) are processed with a rapid frequency-domain solver to provide EMI characterization and model validation [159]. All the voltages included in Table 3.2 are probed (except the inductor section, which is not presented at this stage). Before the model validation, it is worth noticing that CM emission dominates most of the frequency range (150 kHz to 30 MHz) governed by common EMC standards [21,23].

It is worth noticing that the two sets of capacitances $3C_{UG}$ and $3C_{LG}$ on the DC-side, this capacitance asymmetry will result in a cross-mode coupling expressed as follows.

$$v_{Cxm} = \frac{C_{LG} - C_{UG}}{2\left(C_{LG} + C_{UG}\right)} v_{UL} \tag{4.2}$$

This cross-mode coupling is non-trivial to the CM behavior of the system. Using values

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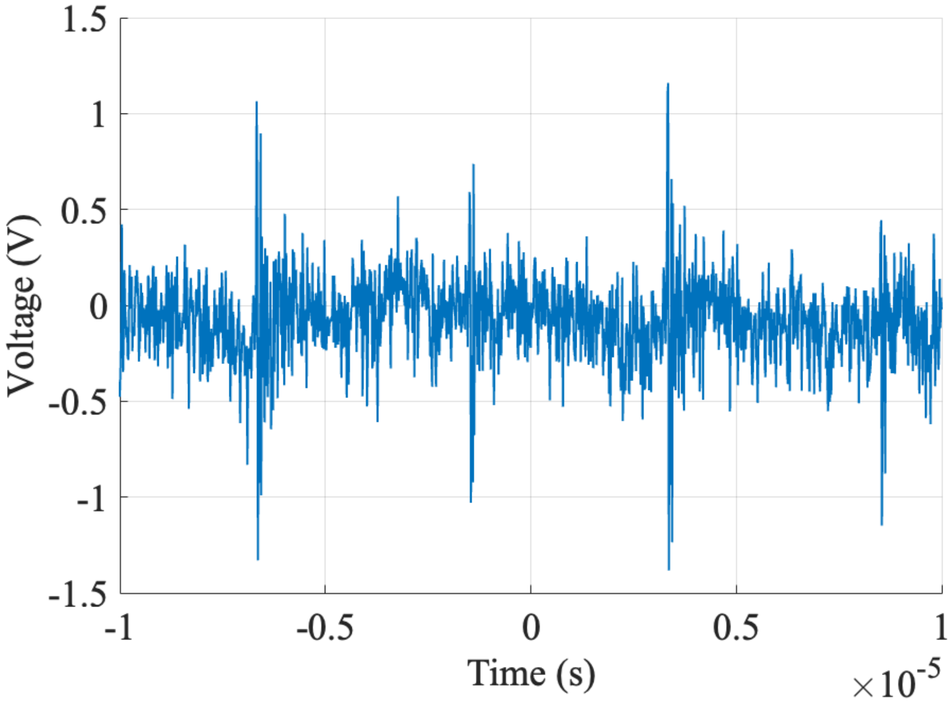

Figure 4.12: Cross-mode coupling v_{Cxm}

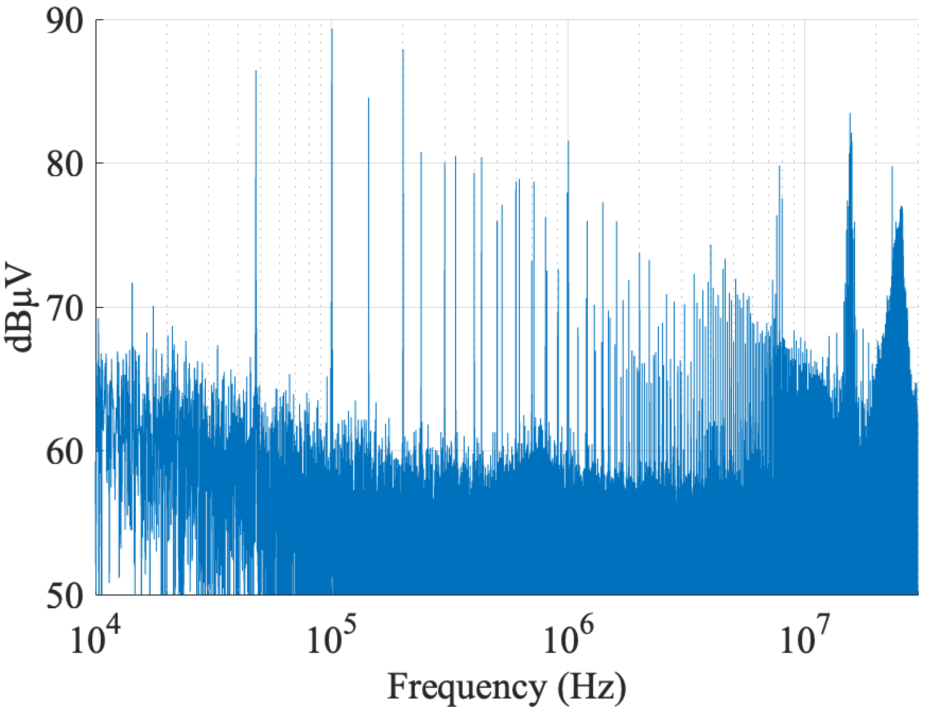

Figure 4.13: Cross-mode coupling V_{Cxm}

Table 4.1: Mixed-mode circuit detail

Element	Value/Expression
Inverter assembly [7]	
C_{dc}	350 µF
C_{UG}	191 pF
C_{AG}	255.7 pF
C_{LG}	102.6 pF
Inductor	
$\mathbf{L}_M$	(3.29)
$\mathbf{L}_{ind}$	(3.30)
LISN	
L_l	50 µH
C_{lo}	8 µF
C_{li}	0.25 µF
R_{lo}	5 Ω
R_{li}	1000 Ω//50 Ω
v_{e1}, v_{e2}	EMI measurements
Artificial Network	
L_A	50 µH
C_{Ao}	10 µF
C_{Ai}	0.2 µF
R_{Ao}	5 Ω
R_{Ai}	1000 Ω
R_p	4.5 to 90 Ω

published in [7] (Table 4.1), expression (4.2) quantitatively reflects that there is approximately 15% of the DC-bus ringing (DM) coupling into this CM branch. An example of this cross-mode coupling effect can be seen in hardware analysis (Fig. 4.12 and 4.13). Including this voltage term in CM analysis is essential for the modeling accuracy in high-frequency.

LISN EMI evaluation based on the CEM is compared with the LISN EMI measurement from the testbed to validate the CEM. Fig. 4.14 and Fig. 4.17, 4.18 present the model validation of the VSI. The CEM developed in this study highly matches the hardware measurement. The modeled result is a few dB over-estimation above 10 MHz but still manages to match a major spectral peak around 15 MHz. The The cross-mode coupling term v_{Cxm} described in (4.2) (Fig. 3.8) is also presented in Fig. 4.12, 4.13. It is observable

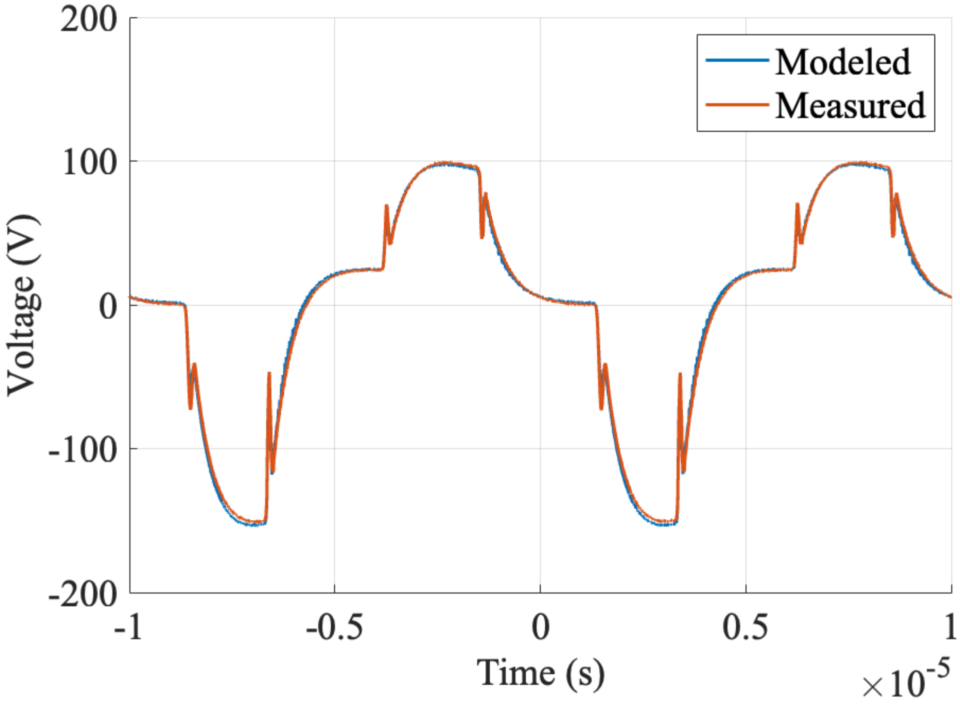

Figure 4.14: Model validation v_e^{cm} (Unfiltered inverter only)

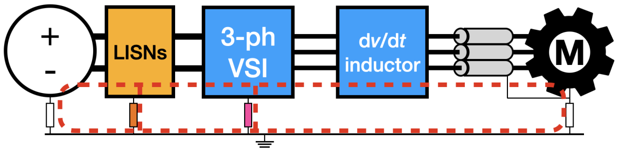

Figure 4.15: Illustration of the motor-VFD system under study (the red dotted line highlights the CM paths)

that this DM to CM influence is significant in the accuracy of the CM model.

4.1.3 Three-phase VFD with motor protection inductor

The model validation with the inductor is done with three types of three-phase inductors: off-the-shelf EE-core $\mathrm{d}v/\mathrm{d}t$ inductor (TCI V1K130A00), custom-made EE-core inductor, and separate-core individual inductors. All of the inductors are 2% inductors at 100 hp (Fig. 4.16). The custom-made EE-core has a significant k_1 value by using four U-shaped core materials. The separate-core individual inductor uses two of the same U-shaped

Table 4.2: Inductors under test

Details	Value
TCI EE-core inductor	
k_1	0.85
k_2	1.01
L_M	150.49 μH
L_{ind}	53.125 μH
Volume	530 in^3
Custom-made EE-core	
k_1	0.22
k_2	0.36
L_M	190.25 μH
L_{ind}	53.231 μH
Volume	40 in^3
Separate-core	
k_1	N/A
k_2	1
L_M	0
L_{ind}	113.23 μH
Volume	20in^3 × 3

core materials for size comparison. This means the separate-core structure uses at least 1.5 times more volume than the common-core case.

The mathematical expressions of the three-phase inductor can be seen in (3.30) and (3.32). It's worth notice that in the separate core case, $k_2 = 1$ and $L_M = 0$, which makes the CEM of the section (3.32) simpler without the cross-mode coupling term and $L^{cm} = \frac{1}{3}L_{ind}$.

To validate the CEM of the inductor, the empirical values of four terms k_1, k_2, L_M, and L_{ind} need to be acquired. Feeding one phase winding while open circuiting the other two causes two of the current terms to be zero in (3.30). Repeating this setup for each phase and measuring the voltages and currents allows the four terms to be solved. The results of this process for the three inductors used in this study are shown in Table 4.2. It is worth noticing that the nameplate inductance values of commercially available three-phase inductors are usually determined by $V_{L,a}/\left(2\pi 60 I_a\right)$ under a balanced, no common-mode, 60 Hz AC condition, where $I_1 = -\left(I_2 + I_3\right)$. This means the nameplate inductance is $\frac{3}{2}L_M + L_{ind}$.

Figure 4.16: Inductors used in this study (Upper: TCI V1K130A00; Lower-left: Custom-made separate-cores; Lower-right: Custom-made common-core.)

With these solved model details, the inductors are, in turn, connected to the inverter (Fig. 4.9) to investigate the system CEM's validity. Since the unfiltered VSI assembly CEM is already validated, it is considered part of the testbed at this stage. All the voltages included in Table 3.2 are probed. The same validation process is then performed as presented in the previous VSI-only validation. The validation results are plotted in Fig. 4.19, 4.21, and 4.22. The model successfully matches the measurement in all three cases with accuracy relatively similar to the VSI-only case. Mathematically speaking, the common-core structure cancels out the CM current-induced flux and provides significantly less CM attenuation than the separate-core structure. This CM behavior difference

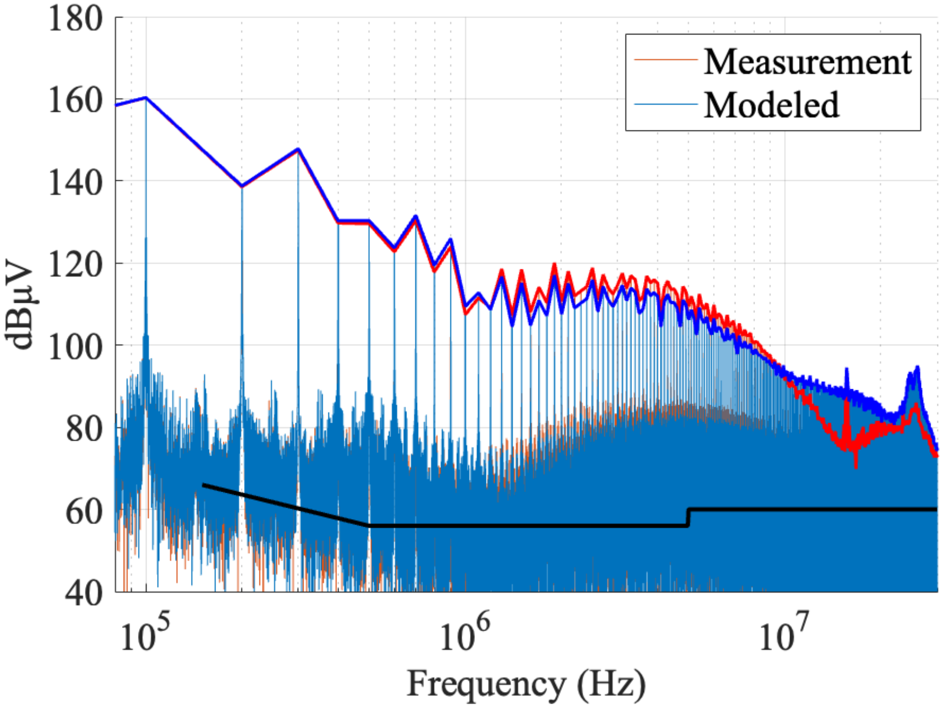

Figure 4.17: Model validation V_e^{cm} (Unfiltered inverter only)

can be seen in hardware measurement (Fig. 4.23).

Given the rapid advances in wide band gap power electronic devices, the ever-increasing switching frequencies, and the innate benefits of these advances. It is critical to the field to develop an understanding of the EMI/EMC implications of future designs. Higher switching frequencies result in higher $\mathrm{d}v/\mathrm{d}t$, which is one of the primary drivers of CM in systems. In the future, line filters on VFD outputs will be a design requirement on most VFDs due to the impact of the high $\mathrm{d}v/\mathrm{d}t$ resulting from higher switching frequencies [56]. The dominant CM implications of these advances are in the 80 kHz to 30 MHz range, making adherence to applicable standards no longer a design afterthought. The presented new methodology and analysis technique is necessary for the required collective understanding vital to future system design. The methodology presented above for analyzing a $\mathrm{d}v/\mathrm{d}t$ inductor is also a valid way of modeling conventional EMI inductors when designing an EMI filter. As shown from the hardware results in Fig. 4.23, the CM

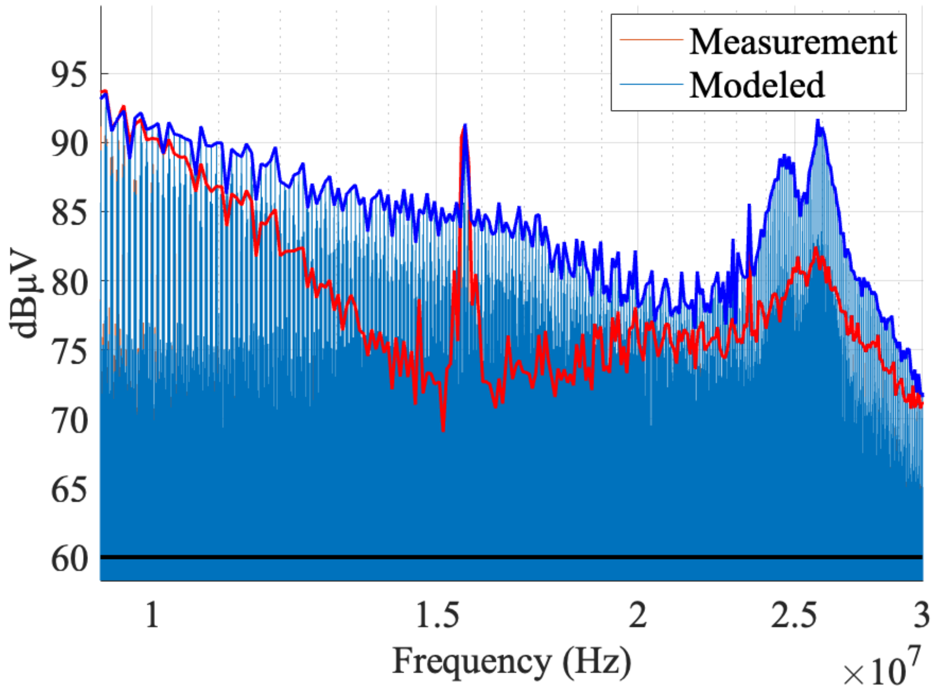

Figure 4.18: Model validation (detail) V_e^{cm} (Unfiltered inverter only)

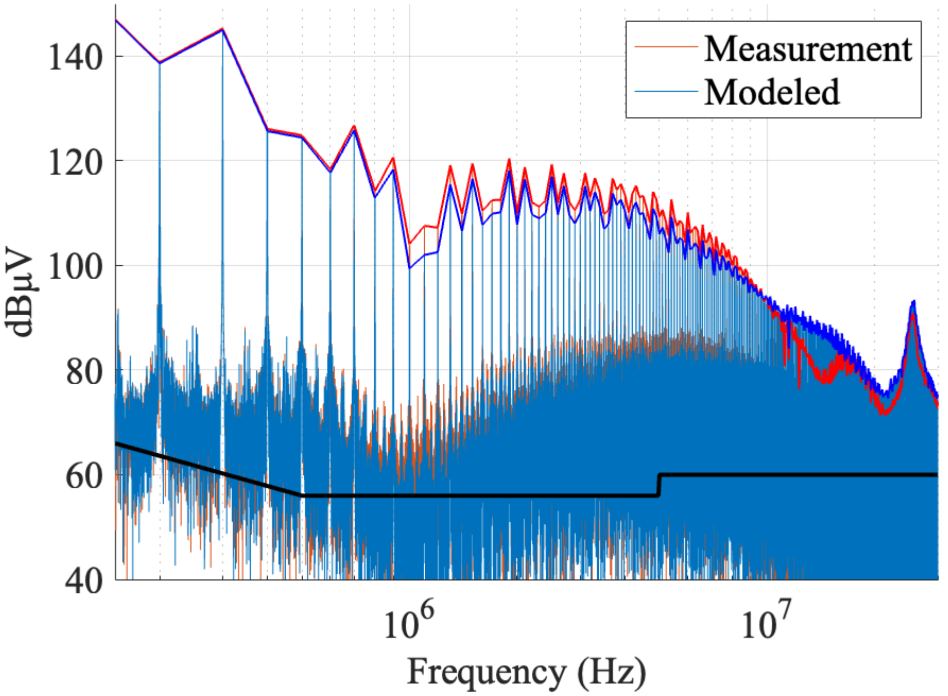

Figure 4.19: Model validation (detail) V_e^{cm} (Full system with TCI inductor)

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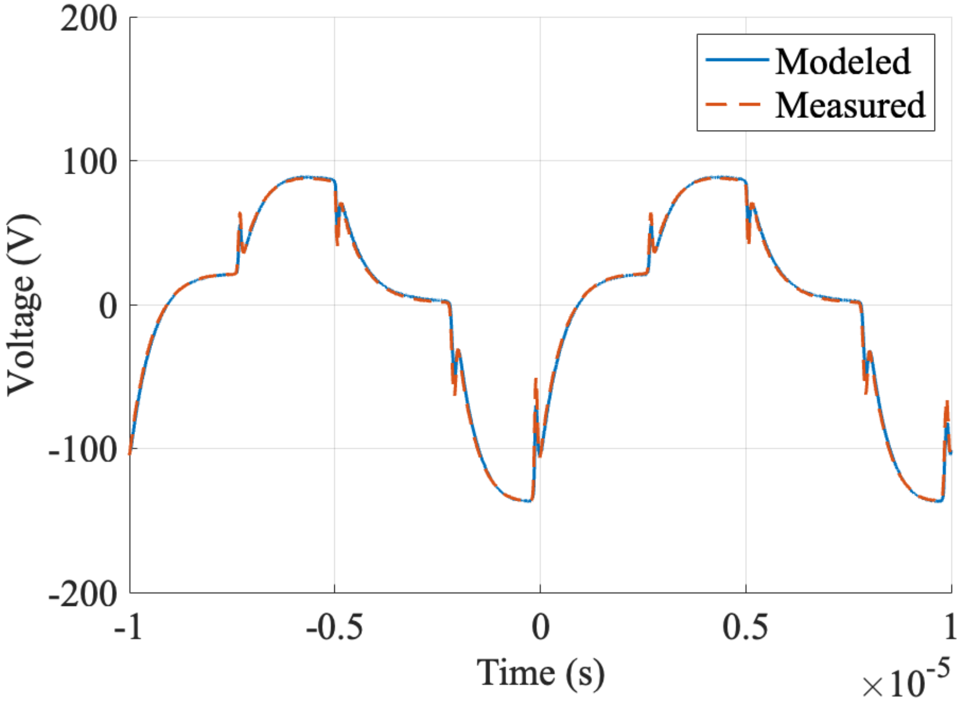

Figure 4.20: Model validation v_e^{cm} (Full system with custom EE-core inductor)

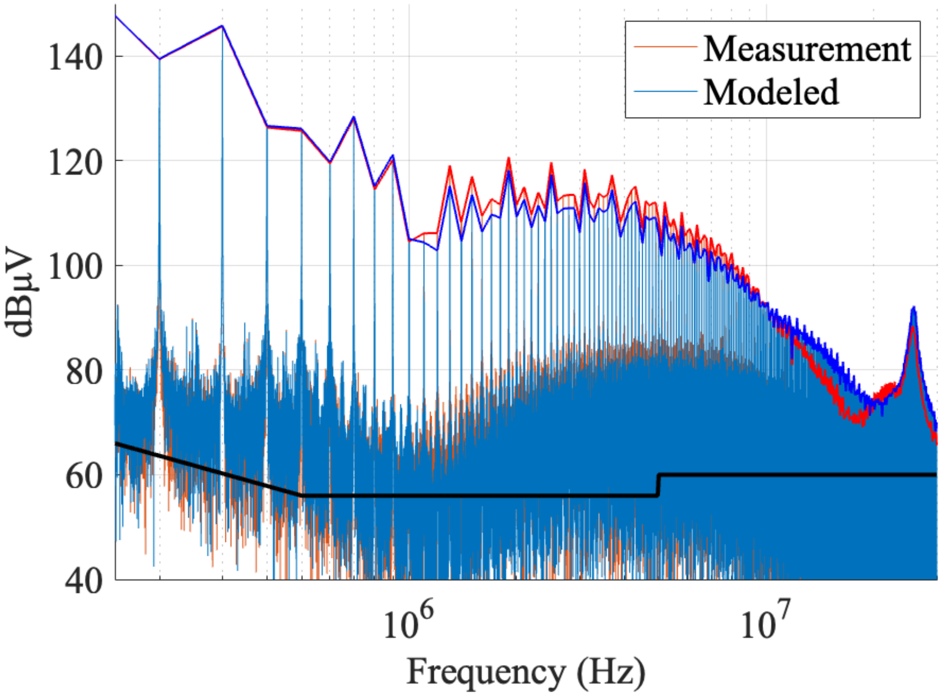

Figure 4.21: Model validation (detail) V_e^{cm} (Full system with custom EE-core inductor)

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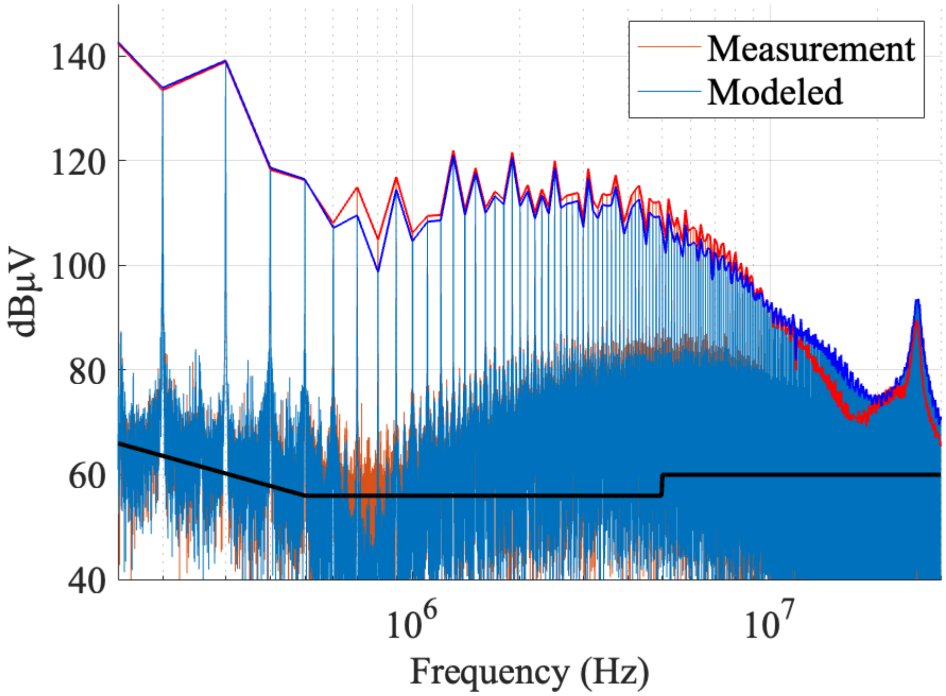

Figure 4.22: Model validation (detail) V_e^{cm} (Full system with custom separate-core inductor)

attenuation of the $\mathrm{d}v/\mathrm{d}t$ filter may relieve some of the burdens on CM mitigation that are required to make the VFD electromagnetically compatible. This methodology will help the designer in coming up with a more holistic and cost-effective approach to conduct EMI mitigation.

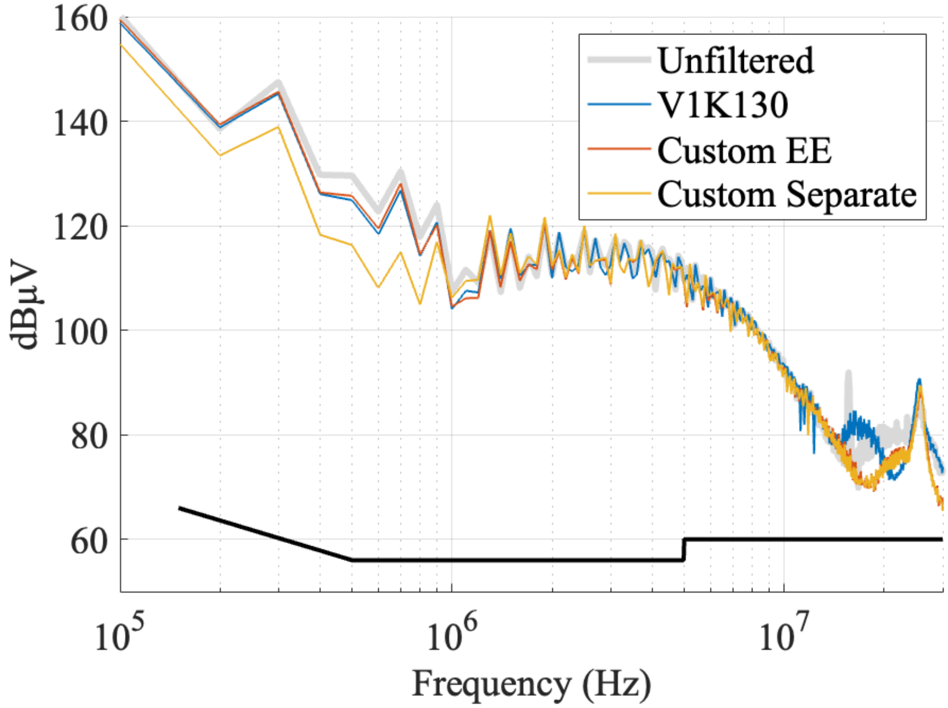

Figure 4.23: CM EMI measurement V_e^{cm} (envelope only) comparison among different $\mathrm{d}v/\mathrm{d}t$ inductors and unfiltered inverter

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Chapter 5

Summary

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Motivated by the increasing need for a new toolset for common-mode behavior modeling in high-voltage SiC MOSFET-enabled voltage source converters, the author successfully developed an innovating set of common-mode models for all the essential electrical circuit segments that form up these fundamental voltage source converters. These segments, *e.g.*, *switching modules, and filter structures*, can be easily used as building blocks to construct the common-mode models of converter systems, *e.g.*, *buck converter, boost converters, and VFD inverters with front-end and/or back-end filters*. The accuracy of these common-mode models is validated with two applicational scenarios [159, 160] at frequencies up to 30 MHz. The common-mode behavior modeling in these two scenarios is highly accurate in the frequency range of conducted emission EMI standards. With more electrical circuit segments, *e.g.*, transformers, being modeled, the common-mode behavior of more complicated *isolated converters* can also be modeled and analyzed. Such development efforts are already undergoing with the author's team [166]. Potentially, the spectral details and accuracy provided by the constructed common-mode models can also identify the sources of radiated emission EMI of voltage source converters and offer guidelines in radiation mitigation design, *e.g.* enclosure design and additional filtering, and inter-system EMC design.

This novel analytical methodology and common-mode equivalent model building blocks provided by this dissertation can be implemented in various development and research aspects regarding the utilization of SiC MOSFET in high-voltage, high-power-density voltage source converter applications. The modulized design and lightweight analytical methods will enable more thorough and larger-scale design optimization, *e.g.*, converter system virtual prototyping and multiobjective optimization [167]. Especially the close-formed common-mode behavior model of the three-phase common-core inductor, which results from the inductor's magnetic structure and parasitic analysis, will serve as a powerful tool to further realize the potentials and challenges in the utilization of WBG semiconductor power switches.

Appendix A

Custom-made Hardware Test Environment

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A.1 Custom-made EMI characterization testbed

The authors built a custom-made EMI characterization platform to validate and realize the developed methodology, which contains the instrumentation required, including measurement devices, FPGA controllers, and data acquisition devices. The EMI measurement devices, Line Impedance Stabilization Networks (LISN) (Fig. A.3), are custom-made to ensure accuracy of the methodology presented in [76].

A.1.1 Line Impedance Stabilization Networks

The LISNs are also capable of sustaining high power noise generated from an unfiltered power converter. The voltage waveforms are measured by Tektronix MSO58 Oscilloscope and HVDP0200 voltage probes. All the voltage waveforms are measured in synchronization with the converter in regular operation (Fig. A.5). All the attached hardware in the platform is calibrated so that the lumped element models included in the mixed-mode circuit models and CEM are accurate. The EMI measurement accuracy has been validated for the frequency range from 1 kHz to 30 MHz.

The LISNs are designed with parameters defined in MIL-STD 461G [25] where $L_l = 50$ µH, $C_{ib} = 0.25$ µF, $R_{ib} = 1000\ \Omega$, $C_{ob} = 8$ µF, and $R_{ob} = 5\ \Omega$. The configuration is different among standards, but the frequency response is sufficiently similar for characterization purposes. In the author′s test environment, the calibrated LISN schematics can be seen in Figure A.1. The impedance details can be seen in Figure A.2.

A.1.2 Measurement metrology

The voltage waveforms are measured by Tektronix MSO58 Oscilloscope and HVDP0200 voltage probes. All the voltage waveforms are measured in synchronization with the converter in regular operation (Fig. A.5). All the attached hardware in the platform is calibrated so that the lumped element models included in the mixed-mode circuit mod-

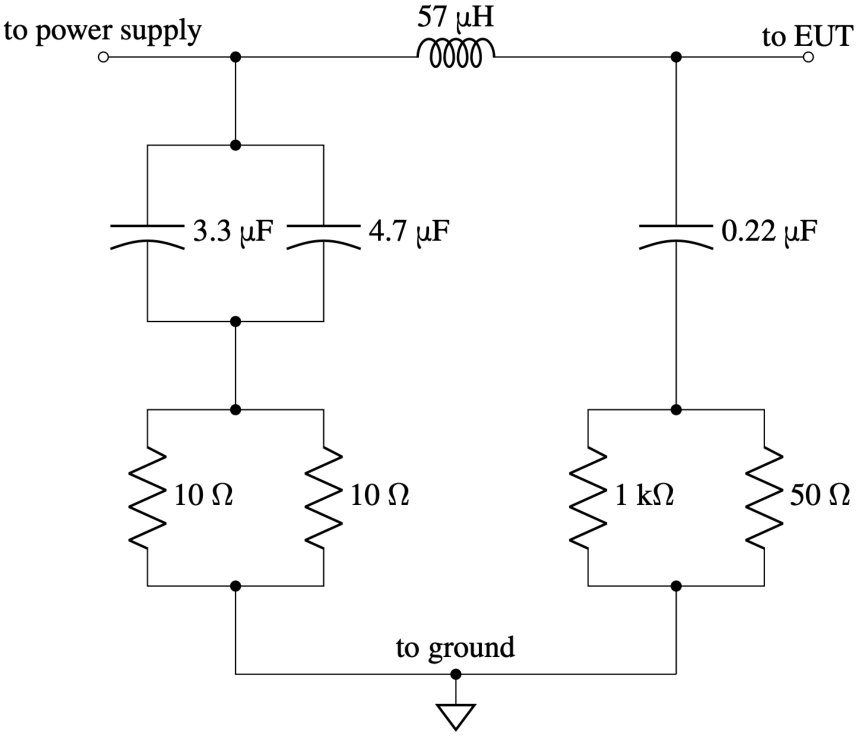

Figure A.1: LISN schematics

els and CEM are accurate. The EMI measurement accuracy has been validated for the frequency range from 1 kHz to 30 MHz.

A.2 Custom-made semi-anechoic EMC chamber

During study at the University of Wisconsin-Milwaukee, the author designed a power electronics specialized semi-anechoic EMC chamber in collaboration with *AP Americas*. The chamber was purchased from and assembled by *AP Americas* at a local laboratory space. The chamber's nominal dimension is 13.4 m by 6.1 m by 3.2 m (length by width by height), and the door is 2.7 m by 2.4 m (height by width, Figure A.7), which allows heavier and larger power converter-enabled equipment to fit in. With specialized cable access (Figure A.6), the power supply and LISNs are sized to enable 300 A at 1600 V DC operation, which will allow EMI characterization of unfiltered high-power power converters. At the completion of this dissertation, the shielded enclosure (*performs isolation from ra-*

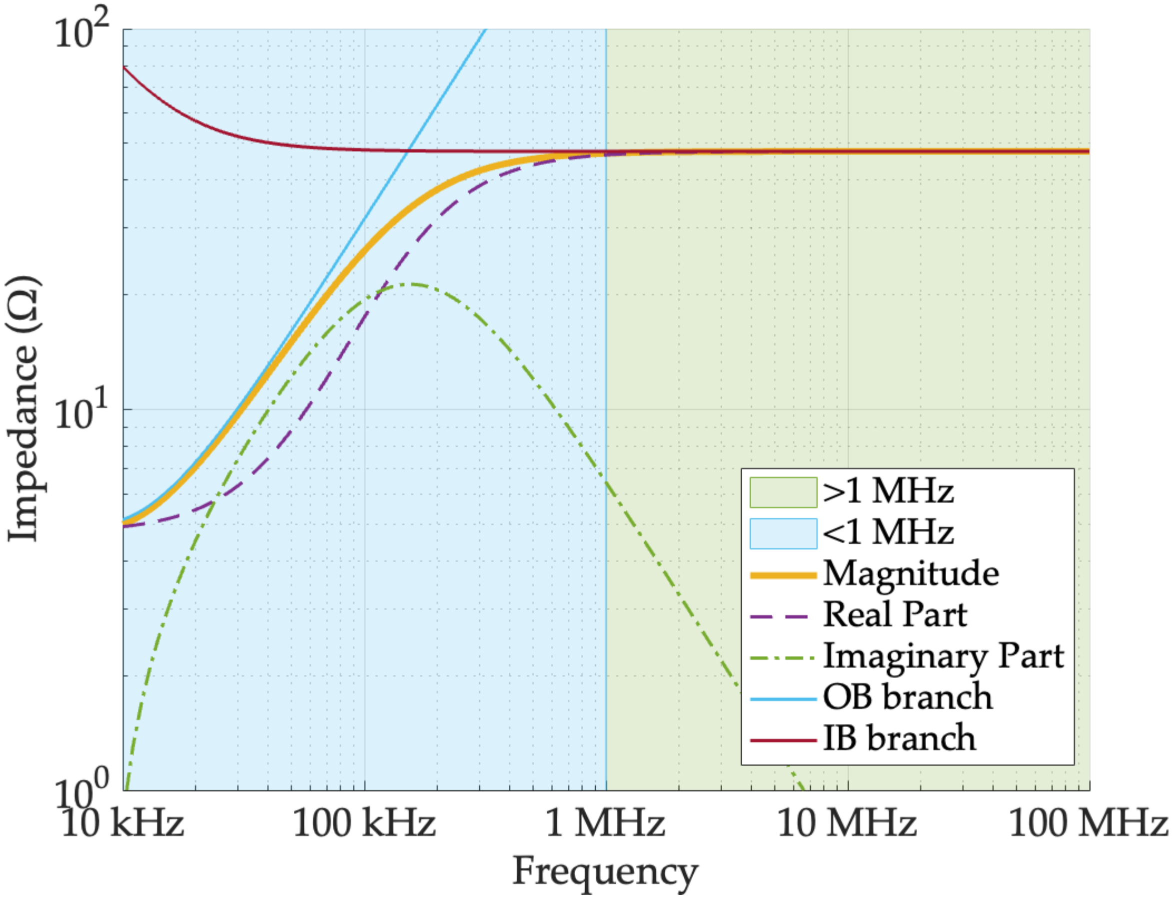

Figure A.2: LISN impedance detail

diation up to 20 GHz) and wall and ceiling ferrite absorbers (*perform radiation absorption between 30 MHz to 1000 MHz inside the chamber*, Figure A.8).

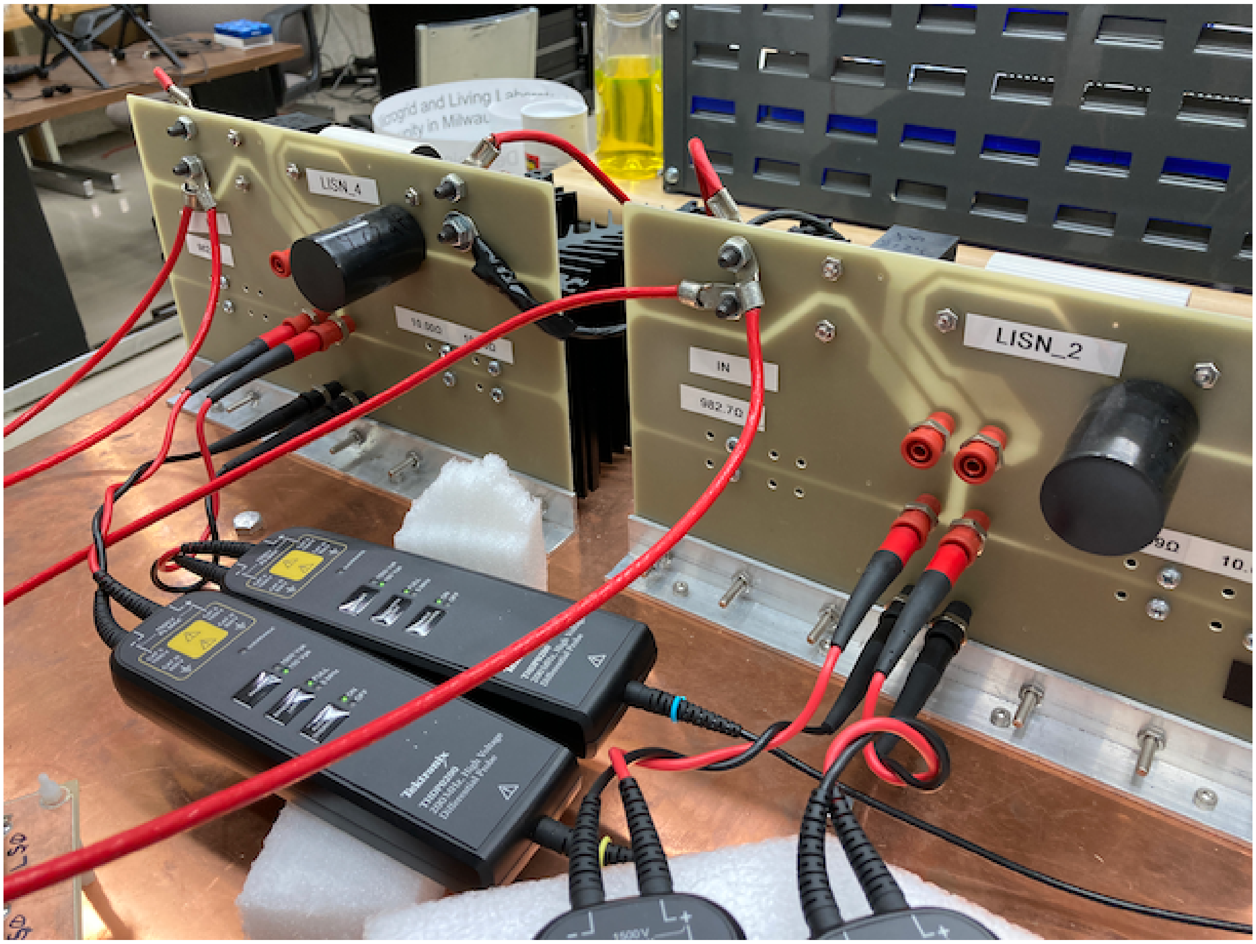

Figure A.3: Line Impedance Stabilization Network used in test

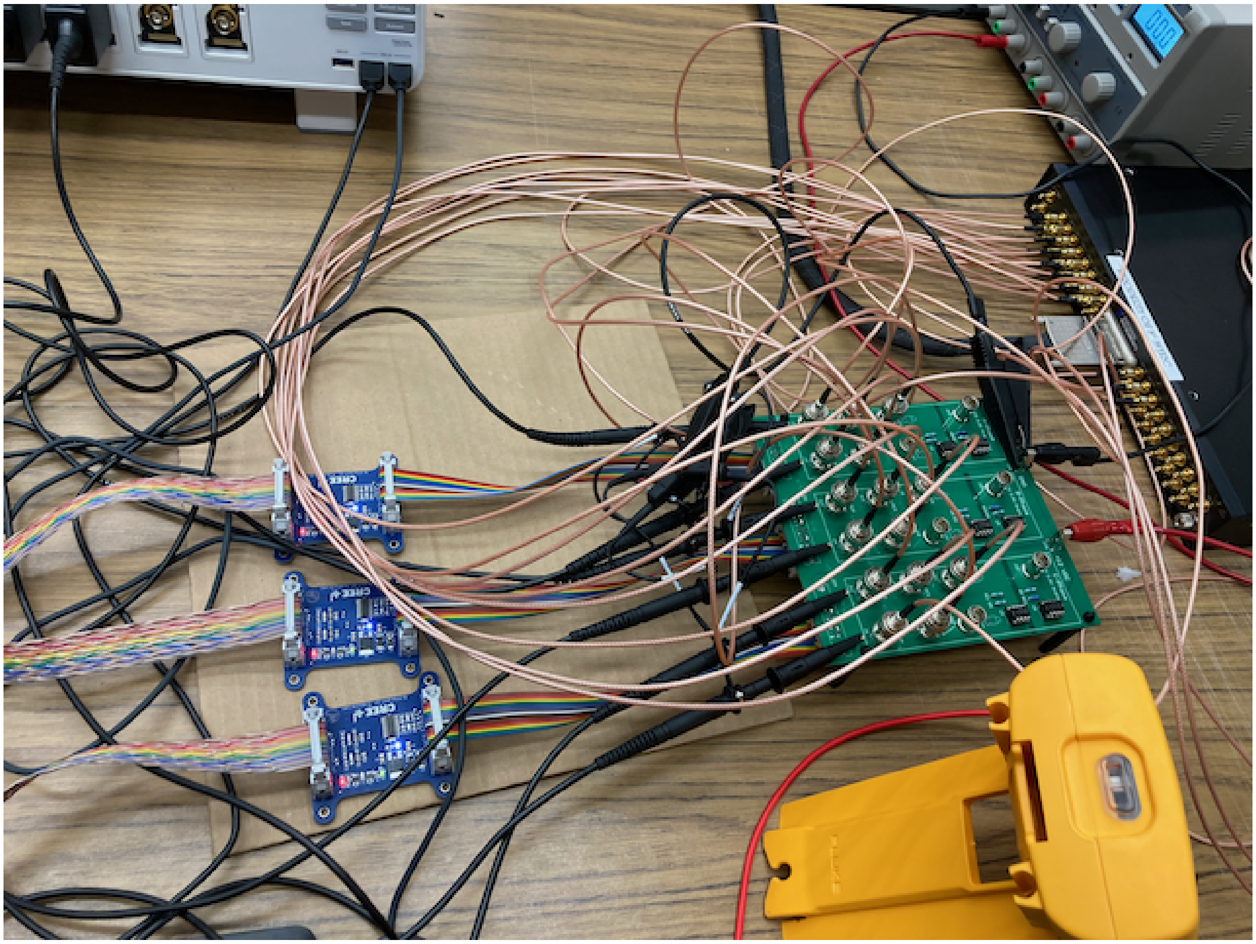

Figure A.4: Interface boards between FPGA-based control and gate drives

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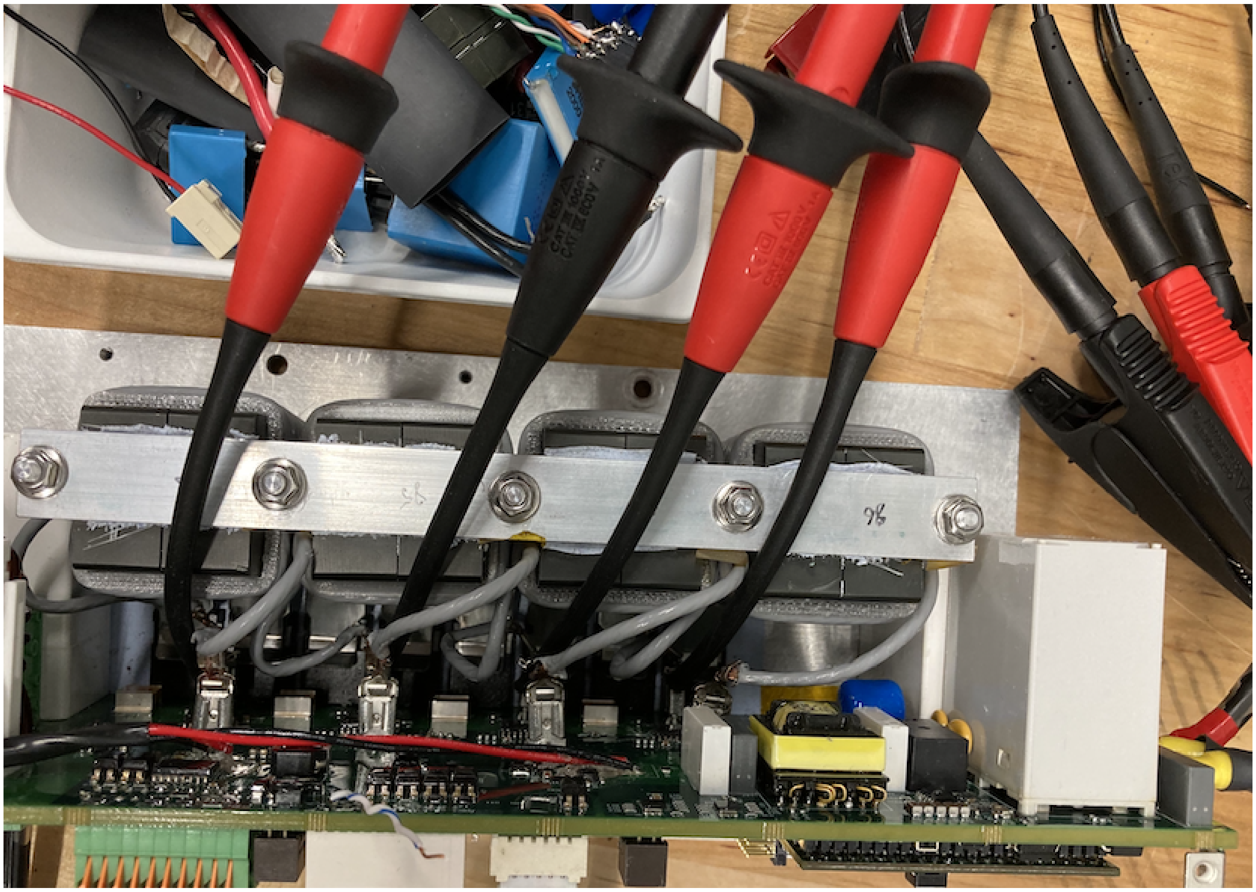


Figure A.5: Voltage probing example: Unfiltered four-pole converter with voltage probe tips

Figure A.6: Author and teammates standing next to the chamber interface side

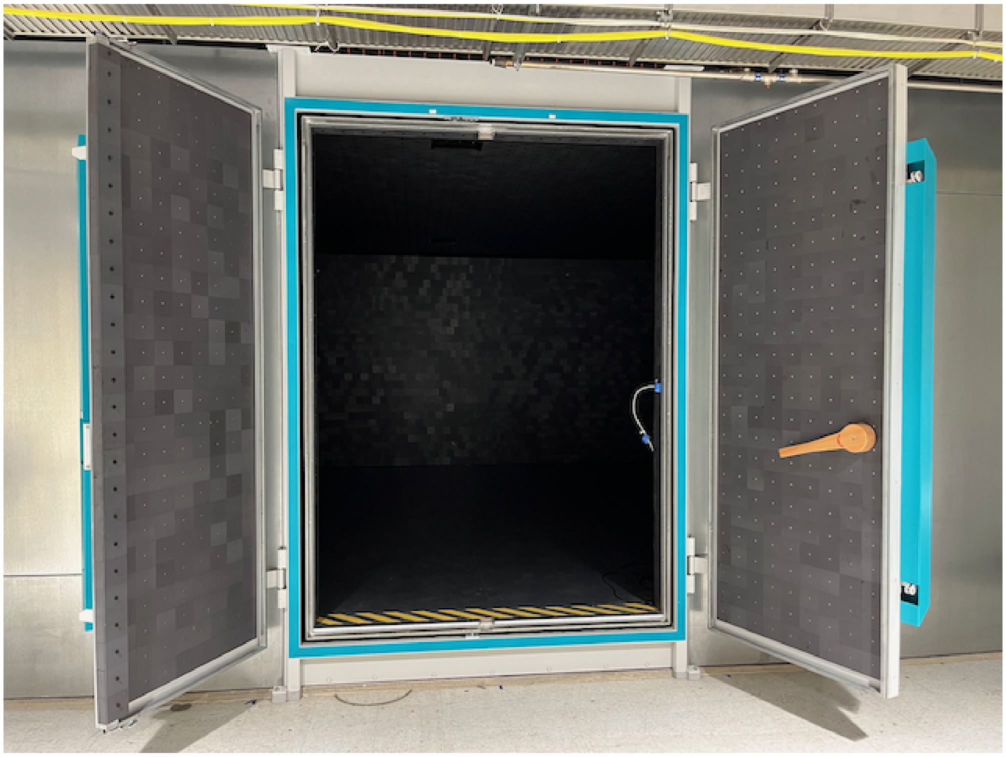
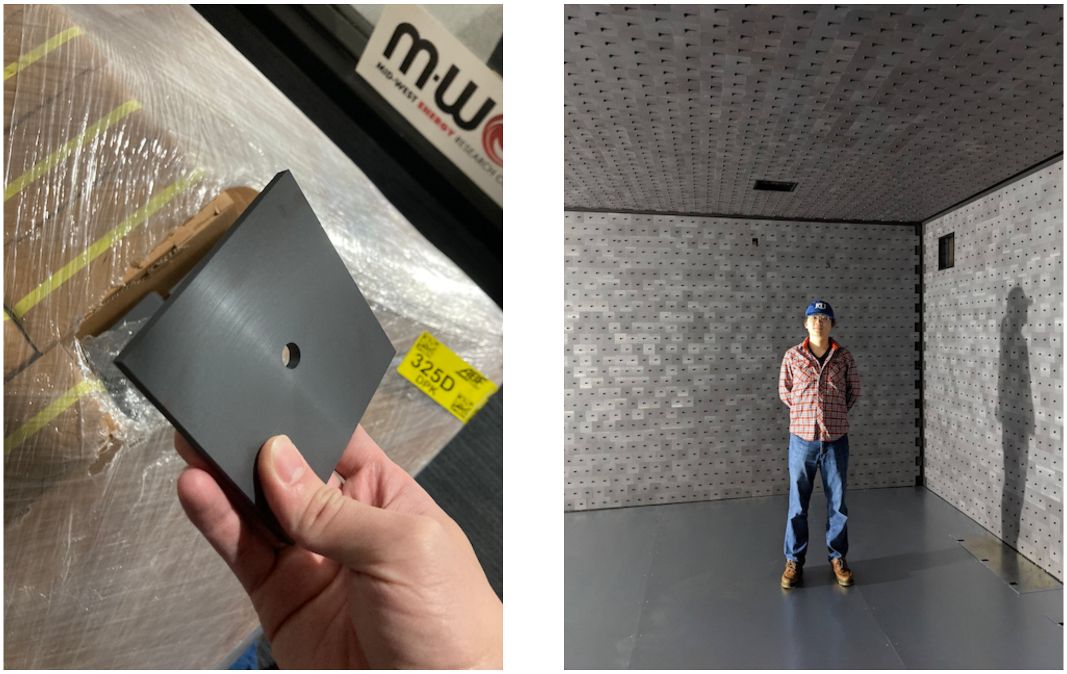


Figure A.7: Chamber door



(a) Ferrite tile used in chamber

(b) Author standing in the chamber with absorbers visible on interior walls and ceiline

Figure A.8: Ferrite absorber

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Appendix B

Rapid frequency-domain circuit analysis

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B.1 Overview

A rapid frequency-domain circuit solver was developed for the modeling validation process. The solver converts the measured time-domain waveforms into the frequency-domain by performing Fast Fourier Transform (FFT). EMI prediction can be extracted from this solver in the frequency domain by feeding the converted waveforms to a complex frequency domain equivalent circuit (*e.g.*, a capacitor is described as its equivalent impedance $Z_C = \frac{1}{j\omega C}$, an inductor, $Z_L = j\omega L$). The computation contains the complex number form generated by FFT. Therefore, the vital phase information is retained during the analysis. A time-domain waveform is also acquired using inverse Fast Fourier Transform (IFFT) for waveform comparison.

This solver uses significantly less computation time compared with simulation software such as Simulink and PLECS. Using in-situ steady-state measurement data, the solver skipped the start-up transient needed to reach steady-state in most circuit solvers. The use of in-situ switching waveforms also avoids the complicated and inaccurate lumped-element-based behavior models provided by most circuit solvers. Softwares like the PSpice model switch behavior very accurately but have very limited ability in performing larger systems. The light computational cost allows fast design iterations, which in turn makes it possible for designers to efficiently design the EMI filter optimally and virtually before building filter prototypes.

In most cases, electrical engineers only use single-sided spectra for frequency-domain analysis. A single-sided spectrum usually demonstrates the level of measured or simulated signal with respect to a frequency range from a 0 Hz, *i.e.* DC term, to the upper limit of measurement bandwidth. However, most built-in FFT algorithms provided by modern engineering software, such as MATLAB, present the transform results in a double-sided spectrum that starts at the negative bandwidth limit and ends at the positive bandwidth limit. The linear transformation provided by the common FFT algorithm is an efficient and close approximation to the Fourier Transform in continuous time.

$$F(f) = \int_{-\infty}^{+\infty} f(t)e^{-j2\pi ft}\mathrm{d}t \tag{B.1}$$

$$f(t) = \int_{-\infty}^{+\infty} F(f)e^{j2\pi ft}\mathrm{d}f \tag{B.2}$$

The "negative" frequency represents a result of utilizing the complex exponential to isolate the spectral content at each frequency. Mathematically, the "negative" frequency is the complex exponential vector in the complex plain spinning in the reverse direction of its positive counterpart. Physically these pairs will sum up a real waveform. A common example is $\cos\theta = \frac{1}{2}\left(e^{-j\theta} + e^{j\theta}\right)$.

The common practice to turn a double-sided spectrum into a single-sided one is to sum the magnitude of each side of the complex spectrum. The result will clearly show the amplitude spectrum of the measured or simulated signal. But this process eliminates the phase information of the complex spectrum. The developed method keeps the double-sided complex spectrum throughout the solving process. The complex impedances used also matches the FFT-generated double-sided frequency dimension.

Due to the nature of the standard FFT algorithm, in this case, 1-D FFT, the complex spectrum result does not start from the corresponding negative limit of the frequency range. As a matter of fact, FFT, like Fourier Transform, simply transforms the original function from one domain to another, namely x to ξ. The input 1-by-N size array, namely $f(x)$, is fed into a generated N-by-N size matrix. The process results in a new 1-by-N size array, namely $f(\xi)$. When used as a spectrum generator, the domain x is tied to time-domain t, and domain ξ is tied to f. The time-axis can be aligned easily since most time-shift of the entire input signal does not affect the data process and analysis. The time stamps step is the same with the inverse of signal sampling rate f_s. but ξ is not exactly f-axis, nor is it a simple shift. The ξ-axis, when tying to frequency, the array starts from 0 Hz, and at $\frac{1}{2}N$, it reaches the upper spectrum range $\frac{1}{2}f_s$. Starting from $\frac{1}{2}N+1$ to the end of the array, the f should start from $\left(-\frac{1}{2}+\frac{1}{N}\right) f_s$.

The author currently codes the solver in MATLAB. Essential parts of the coded functionalities are included in Appendix B.1.

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B.2 Time-domain to frequency-domain

```
function [A, f] = fftt2f(a, ts)
%   fft2f: FFT for time -> frequency
%   a - time domain signal
%   ts - sampling time interval
%   A - double-sided (frequency) complex spectrum
%   f - frequency axis
    if size(a,2) == 1
        a = a.';
    end
    L = size(a,2);
    if mod(L,2)
        L = L-1;
    end
    fs = 1/ts;
    f = [fs.* (-L/2+1:-1)/L, fs .* (0:L/2)/L];
    A = fft(a(1:L))/L;
    A = [A(L/2+2:L) A(1:L/2+1)];
end
```

B.3 Frequency-domain to time-domain

```
function [a,t] = ifftf2t(A,fs)
%   ifftf2t Inverse FFT for frequency -> time
%   WARNING: Only use double-sided complex spectrum with even length!
%   A - double-sided spectrum
%   fs - sampling frequency
```

```
%   a - time domain signal
%   t - time axis centered at 0
    ts = 1/fs;
    if size(A,2) == 1
        A = A.';
    end
    L = size(A,2);
    if mod(L,2)
        L = L-1;
    end
    A = [A(L/2:L) A(1:L/2-1)];
    t = -ts*L/2+ts/2:ts:ts*L/2-ts/2;
    a = ifft(A*L);
end
```

B.4 EMI test style spectrum

```
function [P,Pdb,freq] = fftemi(signal,fs)
%FFTEMI Quick FFT time -> frequency (single-sided)
%   INPUT parameters
%       signal: Time domain signal
%       fs:     Sampling frequency
%   OUTPUT parameters
%       P:      Spectrum magnitude absolute value
%       Pdb:    Spectrum magnitude in dB
%       freq:   Spectrum frequency axis
    if size(signal,2) == 1
```

```
            signal = signal.';
        end
        L = size(signal,2);
        if mod(L,2)
            L = L-1;
        end
        Y1 = fft(signal(1:L));
        P2 = abs(Y1/L);
        P = P2(1:L/2+1);
        P(2:end-1) = 2*P(2:end-1);
        Pdb = mag2db(P);
        freq = fs*(0:(L/2))/L;
    end
```

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