Fabrication of InAs/AlSb/GaSb heterojunction bipolar transistors on Al_2O_3 substrates by wafer bonding

P. D. Moran[a)]
Department of Chemical Engineering, University of Wisconsin, Madison, Wisconsin 53706

D. Chow and A. Hunter
HRL Laboratories, LLC, Malibu, California 90265

T. F. Kuech
Department of Chemical Engineering, University of Wisconsin, Madison, Wisconsin 53706

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High-frequency integrated circuit applications of GaSb-based materials are hampered by the lack of a suitable lattice-matched insulating substrate. Wafer bonding was used to fabricate InAs/AlSb/GaSb-based heterojunction bipolar transistors (HBTs) on an insulating sapphire substrate through a low temperature bonding process that results in a high bond strength and permitted the mechanical and chemomechanical removal of the initial GaSb substrate. The use of selective etches allows for the retention of the epitaxial device layers over virtually the entire wafer area. Minimal degradation of the transferred layers occurred in the bonding and substrate removal process. The resulting transferred structures were fabricated into functional HBTs exhibiting a dc current gain of ~5. [DOI: 10.1063/1.1359140]

Significant interest is presently focused on the development of electronic devices based on InAs, GaSb, AlSb, and their alloys with lattice constants near 0.61 nm. These semiconductors can have a high electron mobility[1] and offer a wide range of electronic band gaps, band offsets, and electronic barriers.[2] Although several notable device[3–5] and circuit[6,7] demonstrations have been made using these materials, the absence of lattice matched, insulating substrates remains an issue, particularly for minority carrier devices. Bulk-grown GaSb is the most widely available substrate for the near lattice-matched epitaxial growth of these materials. GaSb is not, however, available in semi-insulating form. A semi-insulating substrate or insulating platform is critical for many applications due to high parasitic capacitances which arise when metal interconnect lines are placed above conductive substrate materials. Sapphire substrates have the dielectric properties suitable for such applications,[8] but are not suitable for direct heteroepitaxial growth due to the large lattice and thermal expansion coefficient mismatch.

To realize InAs/AlSb/GaSb heterostructure devices on insulating substrates, we have grown epitaxial layers on lattice-matched GaSb substrates and directly bonded the layers to a suitable insulating platform, i.e., Al_2O_3. The initial GaSb substrate is removed and the remaining layers are processed into device structures. The wafer bond between the Al_2O_3 and the epitaxial surface layer is demonstrated to be strong enough to withstand the subsequent processing associated with GaSb substrate removal. In this process, the ~500 μm GaSb substrate is completely removed, leaving the <1 μm thick device layer intact. Highly selective etching is used to fabricate a device from the transferred layers. Additionally, any structural degradation or changes in strain of the layers due to the bond-and-transfer processes is assessed. The characterization of devices fabricated from the transferred layers is used to determine the device-level impact of the bond-and-transfer processing.

Heterojunction bipolar transistor (HBT) structures were grown by molecular beam epitaxy (MBE) on (100)-oriented GaSb substrates at a substrate temperature of 480 °C. An inverted HBT structure was used in which the normal layer growth sequence of substrate, subcollector, collector, base, emitter, and emitter contact was inverted during growth: i.e., substrate, emitter contact, emitter, base, collector, and subcollector. The inverted HBT structure, after bond-and-transfer, results in a sequence of device layers identical to that encountered during processing of the noninverted device layers on their conventional GaSb substrate. The layer structure and band diagram for the HBT are given in Fig. 1. The structures consist of a 300 nm n^+ InAs/InAsSb superlattice subcollector, a 300 nm *n*-type InAs/AlSb (2 nm/2 nm) superlattice collector, a 75 nm p^+ $Al_{0.2}Ga_{0.8}Sb$ base, a 63 nm *n*-type InAs/AlSb (1 nm/2 nm) superlattice emitter, a 36 nm digitally graded n^+ InAs/AlSb superlattice (graded to InAs), and a 600 nm n^+ InAs/InAsSb superlattice emitter contact layer which serves as both an electrical contact to the emitter and as an etch stop for substrate removal. The InAs/InAsSb superlattice layers were grown by periodically exposing the substrate to a relatively low Sb flux for 4 s out of every 20 s during steady state growth of InAs.

Both the surfaces of the inverted HBT structures and sapphire substrates were cleaned by exposure to an oxygen plasma, subsequent rinsing by megasonically excited DI water in a class 10 clean environment, and spin dried at 2000 rpm for 1 min. The GaSb and sapphire wafers were then loaded, still in a class 10 environment, face-to-face in a vacuum chamber at a wafer separation of 50 μm through three supporting metal flags on the periphery of the wafers. The center of the wafer pair was brought into contact and the

a)Electronic mail: pmoran@itis.com

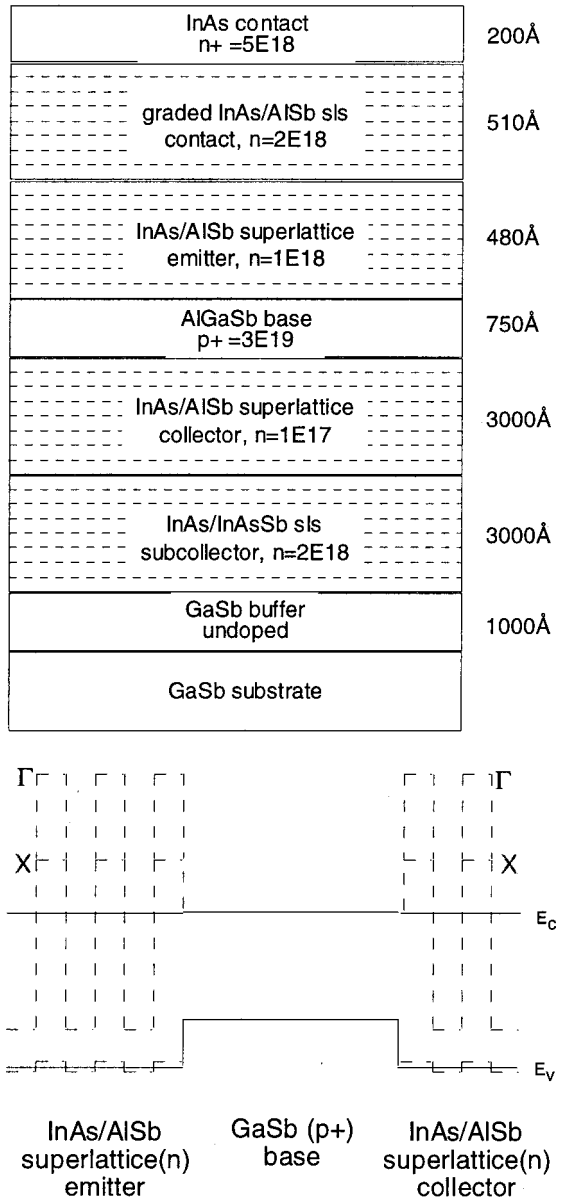

FIG. 1. Layer sequence and band edge diagrams, drawn at flat band conditions, for the inverted InAs/AlSb/GaSb HBT structure. The inverted sequence allows for conventional device processing after wafer bonding. The use of short period InAs/AlSb superlattices for the emitter and collector layers provides significant valence band confinement of holes in the $Al_{0.2}Ga_{0.8}Sb$ base layer, while allowing electron injection into the base and subsequent transport into the collector.

flags separating the wafers at the periphery were removed. No other applied force or heat treatment was employed to bond the wafers. The bonded GaSb substrate was then mechanically lapped to ~45 μm using 9 μm alumina grit. Subsequent chemomechanical polishing, using 0.3 μm alumina grit suspended in a sodium hypochlorite solution, removed additional substrate material to within 30 ± 2 μm of the bonded interface. The bonded samples were subsequently spin etched at ~200 rpm using $HF:H_2C_4H_4O_6:H_2O_2:H_2O$ (1:10:20:100, by weight) to remove the remaining GaSb native substrate. This etch was terminated upon substrate color change from silver-gray to gold corresponding to the removal of the GaSb substrate. The bonded structure was then rinsed for 5 min in flowing DI H_2O and blown dry with nitrogen.

Wafer bonding between the device layers grown on a GaSb substrate and the sapphire substrate was achieved over most of the 2 in. wafer, with the exception of small circular regions in the vicinity of asperities present on the surface of the MBE layers after growth. The bond was sufficiently strong to withstand substrate removal, and the substrate removal process was sufficiently selective so that the device layers remained intact over the majority of the 2 in. wafer after complete removal of the substrate.

The device structures were characterized by high-resolution x-ray diffraction (HRXD) both as-grown, still on the native GaSb substrate, and after transfer to the sapphire substrate. Rocking curve measurements of the device structures were performed with detector acceptance angles of greater than 1°. The absolute (004) Bragg angle of the device layers was determined by performing rocking curve measurements of the sample before and after rotating the samples 180° about the sample surface normal for both the nonbonded and bonded structures. The absolute Bragg angle of the device layers on the GaSb substrate was determined by reference to the (004) peak from the bulk GaSb substrate, while that of the device layers, after transfer to sapphire, was determined by reference to the (006) peak of the sapphire substrate.

Triple crystal diffraction (TCD) analysis of the device layers after transfer to the sapphire substrate was performed by limiting the acceptance angle of the detector to less than 10 arcsec. The contribution to the breadth of the rocking curve from the distribution of angular misorientation or ''bending'' of the lattice planes was estimated by measuring the peak breadth of an ω scan. In an ω scan the detector (with the analyzer crystal in place) is fixed at twice the Bragg angle (2θ) for the (004) diffraction peak from one of the device layers and the diffracted intensity is recorded as a function of the deviation (ω) of the incident angle from θ. The portion of the breadth of the rocking curve due to a distribution of lattice parameter, or strain distribution, within the device layer was estimated by measuring the peak breadth of an $\omega/2\omega$ scan. In an $\omega/2\omega$ scan the diffracted intensity is recorded while varying ω and simultaneously moving the detector (with the analyzer crystal in place) by precisely 2ω.

HRXD rocking curves of the device structures before and after transfer to the sapphire substrate are shown in Fig. 2. The absolute angular position of the device layer peaks, and so their lattice constants, were not changed by the bond-and-transfer process. A broadening in the full width at half maximum (FWHM) of the rocking curve peaks from ~120 arcsec obtained from the layers before transfer to ~260 arcsec after transfer to the sapphire substrate is observed. Further TCD analysis of the diffraction peak due to the InAs/AlSb superlattice emitter revealed that while the FWHM of the $\omega/2\omega$ scan, corresponding to the strain distribution in the device layers, was only 103 in., the FWHM obtained from the ω scan, which corresponds to the spread in angular orientation of the diffracting planes, was 203 arcsec. The increased breadth of the rocking curve observed after transfer to sapphire is therefore interpreted as being due primarily to an increase in the angular misorientation of the device layers

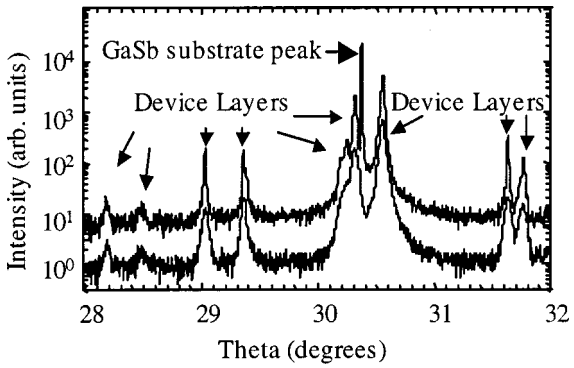

FIG. 2. HRXD (004) rocking curves from the unbonded inverted device structure (top trace) and the bond-and-transferred structure on the sapphire substrate (bottom) show that absolute peak positions of the device layers were unchanged. The diffraction peaks are broadened in the bond-and-transferred scan. This broadening is due to a ''bending'' of the lattice planes of the device structure, rather than due to an increase in the breadth of the strain distribution, e.g., defects, in the device layers. This broadening is attributed to bending of the device layers as they conform to the slight deviations from planarity of the sapphire substrate surface.

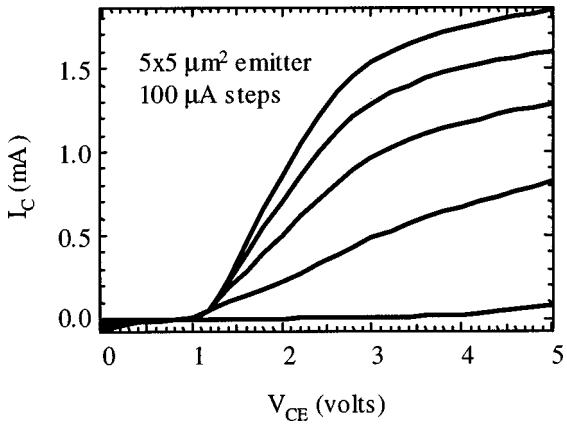

FIG. 3. Collector current as a function of collector-emitter bias at base currents ranging from 0 to 400 μA for HBTs fabricated from the inverted *npn* layers after transfer to the sapphire substrate and removal of the GaSb substrate. The inverted, bond-and-transferred devices exhibited a dc gain of 5, compared to a dc gain of 10 for the noninverted devices on a GaSb substrate.

as they bend to conform to the surface of the sapphire substrate.

Device processing methods developed for the fabrication of HBTs on GaSb substrates were used for the formation of the HBTs bonded and transferred to Al_2O_3 substrates. The process begins with selective wet etching of the 600 nm InAs/InAsSb superlattice, using Au as both an etch mask and emitter contact metal. This selective etch removes virtually all remaining thickness nonuniformity left by the substrate removal process (except for the tops of the emitter mesas, which remain at varying heights). A brief, nonselective wet etch is then used to remove the InAs/AlSb superlattice emitter material, isolating the emitter-base junction. Base contacts, base-collector junction isolation, and subcollector contacts are then achieved through routine processing. The final step in the process is to isolate the HBTs from each other by etching through the $InAs_{0.95}Sb_{0.05}$ subcollector layer to the sapphire substrate.

Current–voltage characteristics of the HBTs on sapphire are presented in Fig. 3. The collector current is plotted as a function of collector–emitter voltage (V_{CE}) for a sequence of base currents ranging from 0 to 400 μA. Similar devices grown and fabricated on GaSb substrates, in a noninverted structure, exhibit a dc gain of 10 whereas those fabricated from inverted structures transferred to the sapphire substrate exhibit a dc gain of 5. Measurements of individual junctions showed an emitter-base characteristic as expected for a high performance HBT, while the collector-base junction had higher leakage than in a control device. The reduced gain of the transistors as well as the nonoptimal IV characteristics is primarily attributed to remaining problems with the growth or processing of the inverted HBT structure. We believe that the increase in the x-ray linewidths do not correspond to the introduction of additional defects, such as dislocations, into the device structure during the wafer bonding process. Rather, the increased x-ray linewidths are due to the conformation of the thin device layers to surface undulations on the sapphire wafer of a long wavelength often seen in polished surfaces. Further improvements will be achieved through additional refinements of the growth procedure, particularly for heterointerfaces in which the potential for anion exchange complicates the growth.

In summary, working *npn* HBTs were formed on sapphire substrates from antimonide based materials grown on a GaSb substrate through a bond-and-transfer process. The low temperature bonding process, combined with a substrate removal and selective etch process, did not significantly alter the strain state and structural integrity of the grown structure. The device characteristics of the HBTs on sapphire substrates exhibited some changes from the control samples which are attributed primarily to the nonoptimized MBE growth of the inverted device structures. These results demonstrate the feasibility of integrating high speed and low power devices and circuits based upon the 0.61 nm materials with sapphire using a process extendable to other insulating substrates.

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