COMMON-MODE MODELING OF NEUTRAL POINT CLAMPED CONVERTER BASED DUAL ACTIVE BRIDGE

by

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A Thesis Submitted in

Partial Fulfillment of the

Requirements for the Degree of

Master of Science

in Engineering

at

The University of Wisconsin-Milwaukee

December 2021

ABSTRACT

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The University of Wisconsin-Milwaukee, 2021
Under the Supervision of Professor Robert Cuzner

Modern power converters designed with wide-bandgap semiconductors are known to generate substantial conducted electromagnetic interference as a side effect of high edge rate and high frequency switching. With the advancement in power electronic converters, the significant EMI challenges need to be addressed for distribution level power systems. The goal is to provide a computationally efficient method of EMI characterization for conducted emissions for this future generation of power distribution systems. The first step in making this possible is through creating an accurate EMI characterization platform for the neutral point clamped dual active bridge. In this thesis, a formalized common-mode modeling approach is carried out for transforming this mixed-mode power system into its common-mode equivalent circuit. The approach is validated through comparison of time-domain waveforms predicted by detailed mixed-mode and common-mode equivalent models of the representative power distribution system, with a proposed future validation using hardware measurements. The experimental studies highlight the utility of the proposed modeling approach to assess design mitigation strategies.

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This thesis work is dedicated to my mother, Peggy, who has always loved me unconditionally and whose good examples have taught me to work hard for the things that I aspire to achieve.

TABLE OF CONTENTS

1 Introduction **1**

1.1 Power Systems 1

1.1.1 Power Electronics 2

1.2 Designing Electrical Systems 3

1.2.1 Grounding 3

1.3 Electrical Distribution Systems 4

1.4 Objective and Motivation 9

1.5 EMI Characterization Methodology 9

1.6 System Description 11

1.7 Thesis Organization 12

2 State of the Art Methodologies **15**

2.1 White-box Modeling 16

2.2 Black-box Modeling 17

2.3 Gray-box Modeling 17

2.3.1 Unterminated Behavioral Modeling 22

2.3.2 CM Equivalent Modeling with Dominant EMI Sources 27

2.4 Transformer Modeling 31

3 Common Mode Modeling of Asymmetric Power Electronic Systems **35**

3.1 Methodology 36

3.1.1 Common-Mode and Differential-Mode Definitions 37

3.1.2 Derivation of Voltage and Current Matrices 40

3.1.3 Common-Mode Equivalent Circuit Model 48

3.2 Derivation of Voltages for Asymmetric Parasitic Capacitor Models 50
3.3 Full-Bridge CM Modeling 57
3.3.1 Derivation of the DC-side CM expression 57
3.3.2 Derivation of the AC-side CM expression 59
3.3.3 Full-Bridge Common-Mode Equivalent Circuit 60
3.4 Three Phase Inverter CM Modeling 60
3.4.1 Derivation of the DC-side CM expression 61
3.4.2 Derivation of the AC-side CM expression 62
3.4.3 3-Phase Inverter Common-Mode Equivalent Circuit 63
3.5 Neutral Point Clamped Full-Bridge CM Modeling 63
3.5.1 Derivation of Super-Node (U,L,N) CM expression 64
3.5.2 Derivation of Super-Nodes (U_A,L_A) and (U_B,L_B) CM expressions . . 65
3.5.3 Derivation of Super-Node (A,B) CM expression 66
3.5.4 Derivation of Input Node (U,L) CM expression 68
3.5.5 NPC Full-Bridge Common-Mode Equivalent Circuit 69
3.6 3-Phase Neutral Point Clamped Inverter CM Modeling 70

4 Medium-Frequency Transformer 73
4.1 Parasitic Effects 74
4.1.1 Leakage Inductance 75
4.1.2 Parasitic Capacitance 76
4.2 Common-Mode Modeling: Method 1 77
4.2.1 Leakage (Stray) Capacitance 78
4.2.2 Intra- and Inter-Winding Capacitance 80
4.2.3 Medium-Frequency Transformer Common-Mode Equivalent Model . 81
4.3 Common-Mode Modeling: Method 2 81

5 EMC Testing and Validation of Models 85
5.1 Electromagnetic Compatibility (EMC) Testing 85
5.1.1 EMC Testing Lab Setup 89
5.2 Common-Mode Modeling and Validation 91

5.2.1 CM Displacement Current 94
5.2.2 Construction and Validation of CEM 96
5.2.3 Floating Heatsink vs. Nuetral Point Clamped Heatsink 105

6 Conclusion **109**

6.1 Summary 109
6.2 Future Work 110

Bibliography **112**

Appendix **117**

A.1 NPC to 2-Level Full-Bridge DAB 117
A.2 AC to AC Converter using 3-Leg ANPC/NPC 118
A.3 AC to DC Isolated Converter 119

LIST OF FIGURES

1-1 Land and Marine based electric power systems 1

1-2 Pre-Electrical Distribution Stage using a Transformer 5

1-3 Conducted emissions in the distribution stage when transformer is excited with higher frequency content 7

1-4 Distribution stage with LISNs 8

1-5 Neutral Point Clamped Dual Active Bridge 11

2-1 Impedance circuit of a Japanese automobile 18

2-2 Artificial network of a Japanese automobile 18

2-3 Noise and Susceptibility measurement systems using artificial network . . . 19

2-4 Equivalent Norton circuit for a switching phase leg module 20

2-5 Two terminal model 21

2-6 Three terminal model 21

2-7 Three phase inverter and DM one-port terminal model 23

2-8 Modular terminated model and proposed DM model with LISN 24

2-9 CM Unterminated-behavioral model 25

2-10 Measured and predicted input and output CM current spectra where SiC inverter was operating without and with CM filters 26

2-11 DC based ship power system 27

2-12 CM equivalent circuit for ship power system 28

2-13 CM currents through parasitic capacitance at source and in buck converter 28

2-14 Half-bridge testbed for characterization of conducted EMI 29

2-15 CM equivalent circuit of half bridge testbed 30

3-1 Transmission Line Model used for CM Methodology 37

3-2 Common-Mode Equivalent Model for Transformer Model 49
3-3 SiC Power Module with Parasitic Capacitance 50
3-4 2 and 3-Line Parasitic Capacitor Models 53
3-5 Full-Bridge Circuit with Parasitic Capacitance 57
3-6 Full-Bridge, DC Parasitic Capacitance Model 58
3-7 Full-Bridge, DC Side CEM 58
3-8 Full-Bridge, AC Parasitic Capacitance Model 59
3-9 Full-Bridge, AC Side CEM 59
3-10 Full-Bridge Common-Mode Equivalent Model 60
3-11 3-Phase Inverter Circuit with Parasitic Capacitance 60
3-12 3-Phase Inverter, DC Parasitic Capacitance Model 61
3-13 3-Phase Inverter, DC Side CEM 61
3-14 3-Phase Inverter, AC Parasitic Capacitance Model 62
3-15 3-Phase Inverter, AC Side CEM 62
3-16 3-Phase Inverter Common-Mode Equivalent Model 63
3-17 NPC Full-Bridge Circuit with Parasitic Capacitance 63
3-18 NPC Full-Bridge, Super-Node (U,L,N) Parasitic Capacitance Model 64
3-19 NPC Full-Bridge, Super-Node (U,L,N) CEM 65
3-20 NPC Full-Bridge, Super-Nodes (U_A,L_A) and (U_B,L_B) Capacitance Models . 65
3-21 NPC Full-Bridge, Super-Nodes (U_A,L_A) and (U_B,L_B) CEM 66
3-22 NPC Full-Bridge, Super-Node (AB) Parasitic Capacitance Model 67
3-23 NPC Full-Bridge, Super-Node (A,B) CEM 67
3-24 NPC Full-Bridge, Input Node (U,L) 68
3-25 NPC Full-Bridge, Input Node (U,L) CEM 68
3-26 NPC Full-Bridge Common-Mode Equivalent Model 69
3-27 NPC Inverter Circuit with Parasitic Capacitance 70
3-28 NPC Inverter Common-Mode Equivalent Model 71

4-1 Simplified Transformer Parasitic Model 77

4-2 HF Transformer, Input Nodes (A,B) and Output Nodes (C,D) Leakage Capacitance Models . . . 78
4-3 HF Transformer, Input Nodes (A,B) and Output Nodes (C,D) Leakage Common-Mode Equivalent Models . . . 79
4-4 HF Transformer: Inter-Winding Capacitance Model(left) and Equivalent Model(right) . . . 80
4-5 HF Transformer CEM . . . 81
4-6 Flyback HF Transformer Parasitic Model Example . . . 82
4-7 Flyback HF Transformer Superposition . . . 83
4-8 Capacitor Voltage Divider . . . 83
4-9 Flyback HF Transformer CEM . . . 84

5-1 Line Impedance Stabilization Network (LISN) . . . 88
5-2 Lab Validation of ANPC Dual Active Bridge . . . 89
5-3 PLECS MM Circuit of ANPC Dual Active Bridge . . . 91
5-4 Steady State Operating Conditions for NPC DAB . . . 94
5-5 Typical Voltage TransitionRate (dv/dt) for a MOSFET during Turn On . . . 95
5-6 CM Displacement Current through Primary Heatsink . . . 95
5-7 2-Line LISN CEM . . . 97
5-8 NPC Full-Bridge CEM w/ P = N . . . 98
5-9 HF Transformer CEM . . . 99
5-10 Full System CEM - NPC DAB CEM . . . 100
5-11 CEM PLECS Circuit used for Validation . . . 101
5-12 CM Currents used for Validation of CEM . . . 102
5-13 CM Validation Current Error: MM vs. CEM . . . 102
5-14 CM Currents: MM vs. CEM(No DM Coupling) . . . 103
5-15 CM Validation Current Error: MM vs. CEM(No DM Coupling) . . . 104
5-16 CM Displacement Current w/ Neutral Clamped Heatsink . . . 106
5-17 NPC Full-Bridge CEM w/ P = L, Neutral Clamped Heatsink . . . 106

A-1 NPC to Full-Bridge DAB CEM . . . 117

A-2 AC/AC Converter using NPC CEM 118
A-3 AC/DC Isolated Converter CEM 119

LIST OF TABLES

5.1 HF Transformer Parameters 92

5.2 System Specifications 93

ACKNOWLEDGEMENTS

Throughout the writing of this thesis I have received a tremendous amount of support and assistance.

I would first like to thank my supervisor, Dr. Robert Cuzner, whose expertise was invaluable in formulating the research development and methodology. Your insightful feedback has pushed me to sharpen my thought process and brought my work to a higher level.

I would like to acknowledge my colleagues in the Power Electronics group at UWM. I want to thank all of you for your patient support and continued collaboration for all of the opportunities I was given to further my research.

I am greatly indebted to my family and would like to thank them for their continued guidance and sympathetic ear. You guys have always been there for me.

Finally, I could not have completed this thesis without the support of my friends, who have provided thoughtful discussions as well as happy distractions to rest my mind outside of my research.

Chapter 1

Introduction

1.1 Power Systems

Electric power systems are comprised of many components that produce electrical energy and transmit this energy to consumers. A electric power system is composed mainly of six main components: power plants which generate electric power, transformers that raise or lower the voltages as needed, transmission lines that carry power, substations at which the voltage is stepped down for carrying power over the distribution lines, distribution lines, and distribution transformers which lower the voltage as needed for the consumer equipment.

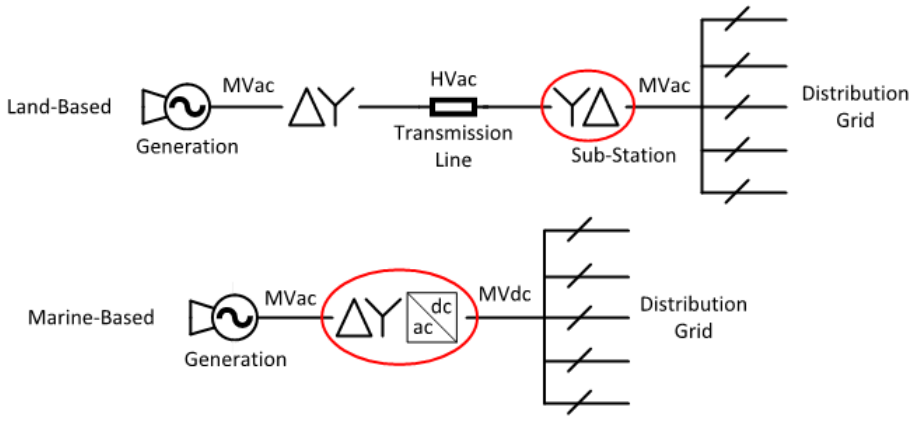

Figure 1-1: Land and Marine based electric power systems

Here are two simple single line diagrams that illustrate a typical land and marine based electric power system from generation to distribution. They are typically composed of all or most of the main components of an electric power system explained before. The main

difference between land-based systems and marine-based systems is the fact that the marine power system is an isolated system with short distances from generated power to load, very comparable to a microgrid. In contrast, land-based systems can have hundreds of kilometers between power generation and the load, with long transmission lines and several voltage transformations between them.

Research in electric power systems concentrates on the study of the emerging technologies of power electronics, distributed energy sources on the electric power system operation, and protection.

1.1.1 Power Electronics

Power Electronics is a technology within power systems that deals with the conversion and control of electrical power with high efficiency solid-state electronics for a wide range of applications. The 21st century has been widely defined as the golden age of power electronic applications after the evolution of technology and major innovations in the past century. It has emerged as the high-tech frontier in power engineering due to its important role in energy conservation, renewable energy systems, and electric and hybrid vehicles. The technology embraces the areas of power semiconductor devices, converter circuits, electrical machines and drives, advanced control techniques, computer-aided design and simulation, as well as artificial intelligence.

The power conversion systems can be classified according to the type of the input and output power. These classifications are; AC to DC (rectifier), DC to AC (inverter), DC to DC (DC/DC converter), and AC to AC (AC/AC converter). Research in this area includes power electronic applications to control large scale power transmission and distribution as well as the integration of distributed and renewable energy sources into the grid.

A lot or research lately has gone into the development of power semiconductor devices with the growing demand for high power density and high efficiency systems. The performance of power semiconductor devices is currently being pushed to the limit for silicon (Si) material. We are now entering a new generation of power semiconductor devices with the development of wide bandgap (WBG) semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN), which provide many advantages over Si. WBG semicon-

ductor materials permit smaller, faster, more reliable power electronic components with a higher efficiency allowing power electronic devices to operate at much higher temperatures, voltages, and frequencies compared to the conventional silicon based materials. However, high dv/dt and di/dt during switching transient as well as high operating frequency, mixed with their unique structure raises the concern of electromagnetic interference (EMI) and converter reliability issues.

1.2 Designing Electrical Systems

When designing an electrical system, you have many specifications and requirements that must be acknowledged. In particular, we want to ensure the safety of people, provide protection of equipment through insulation reliability, and provide mitigation efforts toward EMI. The International Electrotechnical Commission (IEC) has established protection classes for electrical equipment. Classes I and II provide user and equipment protection from electric shock. They provide protection from hazardous voltage with one or more types of insulation systems, a basic insulation system and a reinforced insulation system. Insulation typically uses a material as an isolation barrier to help keep an electric current safely in its proper circuit and prevent leakage. In addition to insulation, a protective earth connection is provided for diverting fault energy if there should be an accidental breakdown of the basic insulation. A protective earth connection uses a protective conductor to direct a fault current safely into the earth and away from a human in contact, as well as diverting current from a faulty circuit for protecting devices.

1.2.1 Grounding

Proper grounding is an important aspect of electrical system design for both safety and electromagnetic compatibility (EMC). Ground plays a crucial role in determining what happens in the event of unintentional faults, transients, and EMI. Improper grounding can impair the safety and EMC of a product or system, and is one of the leading contributors to EMC related failures. The biggest misconception that leads to improper grounding is confusing the terms ground with current return. When current return conductors are treated

like grounding conductors it often results with significant EMC problems. Ground serves as a circuit or system zero-volt reference, or more specifically defined as "the connecting of an electric circuit or equipment to earth or some conducting body of relatively large extent that serves in place of earth." So ground is a reference potential and ground conductors are normally non-current carrying, because significant currents flowing in a conductor can prevent it from being a reliable reference potential. The current return path is a wire or plane used to return the signal, which is usually referenced with a low voltage with respect to ground but should not be confused with ground itself.

An important part of designing safe electrical systems is knowing where and when unsafe voltages may appear on various conducting surfaces. Since ground is the zero-voltage reference, that means the voltage on every other conductor is the difference between its voltage and ground. For land-based systems, the ground reference is usually the earth. This is convenient because the earth is large and all other large metal structures can easily be connected or referenced to earth ground. Earth grounds, or protective earth connections, are typically metal rods driven into the dirt near power service entrances. Substantial exposed metal surfaces or chassis are typically required to ground the metal to the earth ground connection to ensure it cannot reach an unsafe potential.

Grounding strategies are not only important for safety, it also plays an important role in meeting conducted emissions where the ground structure is both the zero-volt reference and the preferred path for interfering common mode noise currents. It is important to know that while the ground cannot carry intentional currents, it is expected to carry fault currents and induced common mode noise currents. The proper utilization of the ground structure depends on its ability to carry unintentional currents with sufficiently low impedance to control unintentional voltages.

1.3 Electrical Distribution Systems

The focal point of this thesis revolves around the electrical distribution stage of power systems, which is very important because it is one of the final stages before power consumption. From Figure 1-1, the electrical distribution system is highlighted by the red circle. A sim-

plified look at a common electrical distribution stage can be seen in the figure below.

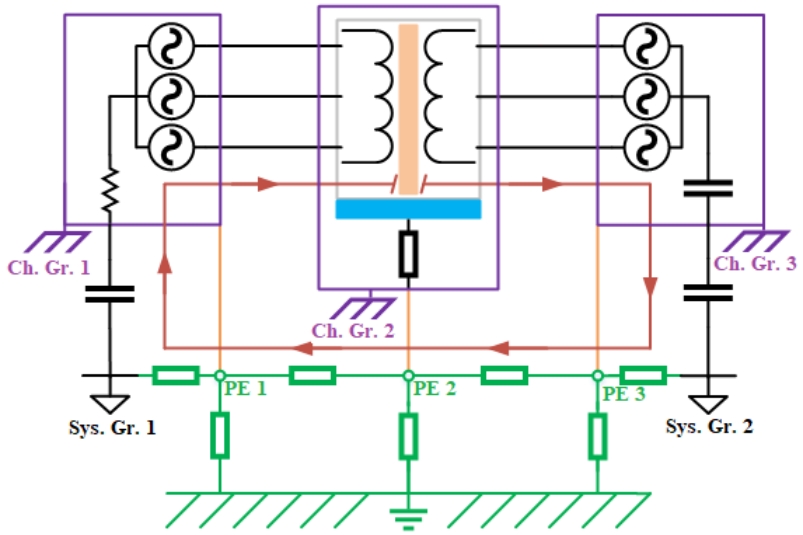

Figure 1-2: Pre-Electrical Distribution Stage using a Transformer

In this simplification of a pre-distribution stage we have two three phase voltage supplies on either side of a transformer, which will be raising or lowering a voltage as needed. On the primary side of the transformer we can consider this power supply as either a generator or a grid tied power service entrance, and the secondary side power supply can be considered as a grid tie for the distribution grid network. There are system ground reference points for both sides of the transformer due to the fact that the transformer provides isolation between primary and secondary sides. The system is much more complicated than this but it has been simplified to get the major points across to the reader.

Now, following the protection classes and grounding structures talked about in the previous section, we enclose the transformer and each power supply inside their own metal enclosure. These metal enclosures, or chassis, are then bonded to a protective earth connection. The protective earth connections are metal rods that are driven into the earth and there is a connection between each one of them through rebar or other means, which creates this equipotential surface at ground level. There is also basic insulation on the transmission lines and between each part of the system with their corresponding chassis. All of this provides safety measures to protect humans from electric shock in case of faults. The primary side supply has a high impedance path to chassis, which is used for detection

of fault current. If a fault occurs that causes a short between the power conductor and the exposed chassis, the ground connection ensures that a large amount of current is drawn and forces a circuit breaker to open and remove power from the rest of the circuit. This ensures equipment safety for downstream devices, and once the fault is cleared the circuit breaker is closed again for system operation. With a grounding strategy like this, it is expected that fault currents are carried away from the system into ground to protect humans and sensitive electrical equipment.

Another safety measure is through the use of the transformer, which is a key asset component of any electrical distribution system. A transformer has two main jobs, one is voltage transformation by stepping up or down the voltage to the desired level, and the other is to provide galvanic isolation between system ground potentials. Galvanic isolation can be extremely effective for providing human safety and improving noise immunity between circuits. Galvanic isolation is a principle of isolating functional sections of electrical systems to prevent current flow, where no direct conduction path is permitted. This type of isolation is used where two or more electric circuits must communicate, but their grounds may be at different potentials. It is an effective method of breaking ground loops by preventing unwanted current from flowing between two units sharing a ground conductor.

With safety concerns met, we can now begin to understand the impact that this system and its grounding structure has on conducted emissions. The term conducted emissions refers to the mechanism that enables electromagnetic energy, in the form of common-mode (CM) current, to be created in an electronic device and coupled back to its AC supply through unintentional paths, with its intent to close the current loop. These CM currents that are coupled back to the AC power can find its way to the entire power distribution network that the circuit is connected to and use the larger network to cause radiated emissions much more efficiently than the circuit could by itself. One may think that transformers and their galvanic isolation can solve this problem of conducted emissions, which may be true at low frequencies but CM currents are typically composed of much higher frequencies. At these higher frequencies, galvanic isolation can have the side effect of increasing CM coupling between the isolated circuits through parasitic capacitance.

So where is this high frequency content coming from? Well, it is the introduction of

power electronics, especially WBG devices, with their high dv/dt during switching transient as well as their high operating frequency that is the main driver for higher frequency content. Figure 1-3 introduces some power electronics to the circuit to understand the impact that higher frequency content has on conducted emissions.

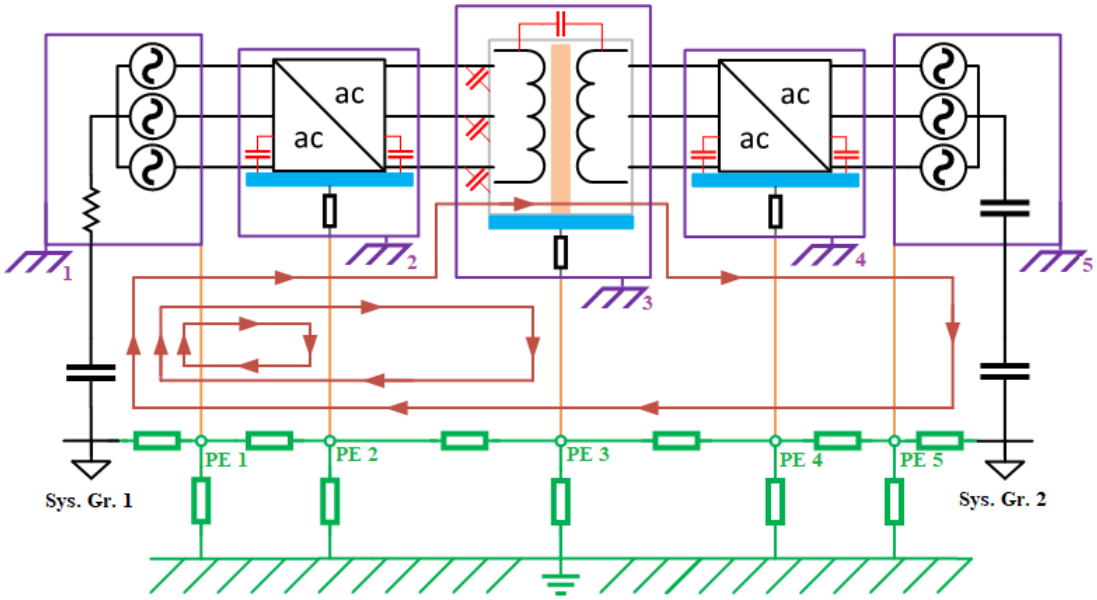

Figure 1-3: Conducted emissions in the distribution stage when transformer is excited with higher frequency content

These power electronics are producing multiple step trapezoidal waveforms that are exciting the transformer at much higher frequencies than the standard 60 Hz AC from the grid or generator. The power electronics are used as a way of changing the frequency of the sinusoidal-like waveforms and has many practical applications. Instead of using an AC to AC conversion stage on the secondary side, a AC to DC converter could be used for a DC distribution grid. At any rate, the transformer is being exposed to much higher frequency content and starts to exhibit different side effects that actually increase the CM coupling between isolated circuits. It is not that the galvanic isolation is breaking down, instead the higher frequency content is introducing parasitic coupling paths based on the geometric layout of the device. These parasitic coupling paths are in the form of leakage capacitance between the windings and the core, and winding capacitance from primary to secondary sides. The parasitic winding capacitance provides a coupling path across the transformer

allowing CM current into other parts of the distribution network and back to the AC supply, giving the circuit a much larger CM ground loop. The parasitic leakage capacitance allows CM current to flow from the windings to the core, into the heatsink, finds a path to the chassis, and then couples back to the AC source. The transformer is not the only device that has parasitic CM coupling paths, the power electronic devices do as well. Based off of these trapezoidal waveforms that it produces, there is parasitic paths that are induced from the device to its substrate, through the heatsink, into the chassis, and then coupled back to the AC source. All of these CM current paths provide a lot of coupling back to the source, which can then be distributed throughout a much larger system and cause a great amount of interference in these devices and other devices connected to the distribution system. As an unavoidable design consideration, EMI issues must be addressed properly otherwise the benifits of WBG power devices and medium frequency transformers can be jeopardized.

To fully understand CM conducted emissions of a system we must introduce the Line Impedance Stabilization Network (LISN). The intent of the LISN is to create an artificial impedance and ground path for conducted emissions for a specific device and its electrical system.

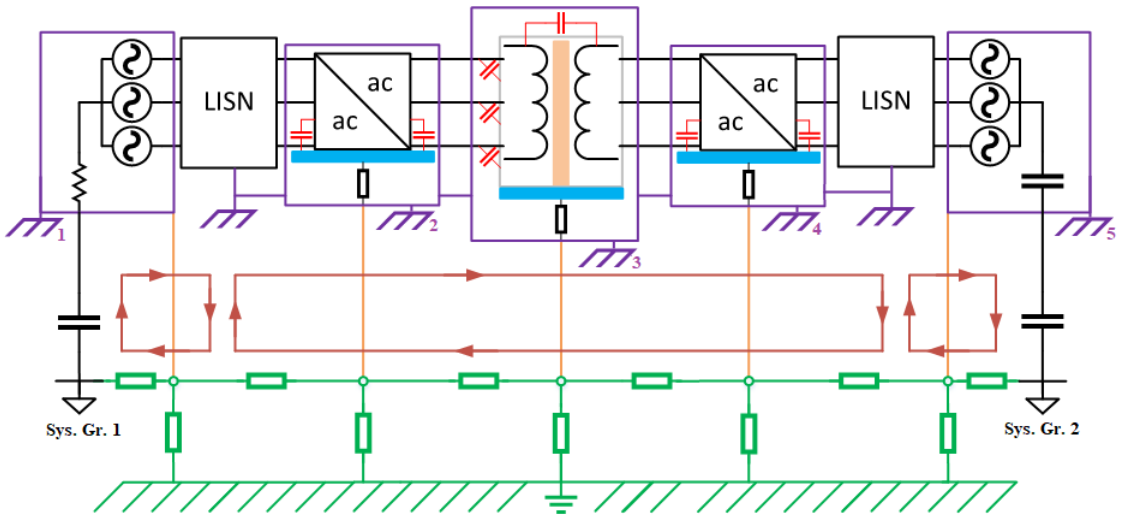

Figure 1-4: Distribution stage with LISNs

Here we have placed main components of interest between the LISNs to understand their CM emissions and the impact they have on conducted emissions as a whole. We connect

common grounds between all Devices Under Test (DUT) to localize the ground path for CM conducted emissions. The LISN acts as a specialized low pass filter. The filter is designed to prevent unwanted noise from coming in on the power leads and mixing in with the DUT, likewise it will also prevent noise from leaving the DUT and getting back onto the power leads. This allows us to isolate the conducted emissions within the DUT and eliminate unwanted noise from entering the circuit so that we can design filters or other mitigation efforts to lower the amount of conducted emissions passed through or generated by the DUT. Over the years, the LISN has evolved and has been primarily used to perform CM conducted emissions measurement on common coupling power leads. The standardized impedance provided by the LISN ensures consistency between multiple tests, and an EMI receiver can measure the isolated CM conducted interference voltage produced by the DUT.

1.4 Objective and Motivation

With the advancement in power electronic converters, the significant EMI challenges need to be addressed for distribution level power systems. It is important that we address these EMI issues properly such that the benefits of WBG devices are not compromised, and we can continue to develop cutting edge devices for the future generation of power electronic systems. Our goal is to provide a computationally efficient method of EMI characterization for conducted and radiated emissions for this future generation of power electronic converters.

1.5 EMI Characterization Methodology

EMI characterization methodology has been emphasized in recent years. Modern power converters designed with WBG semiconductors are known to generate substantial amount of EMI as a side effect of high edge rates and high frequency switching. This has brought increased attention on filtering EMI signals for power converters and no longer focusing just on a power quality standpoint. The EMI spectrum for conducted emissions is in the 100 kHz to 30 MHz range, and anything above the conducted emissions up to 10 GHz is in the radiated emissions range. To better understand the EMI emission sources and

design optimized EMI mitigation strategies, we need to develop characterization methods and models to accurately predict EMI.

For a system to achieve electromagnetic compatibility (EMC) with itself or its surrounding environment, we must ensure that our electrical devices don't emit a large amount of EMI, through either radiated or conducted emissions, and that our device continues to function in the presence of other electromagnetic phenomena [1]. There are many regulatory agencies that have placed limits on the level of emissions that our electrical devices are allowed to generate, and often times we are mandated to abide by these limits. There is a finite region of the electromagnetic spectrum that is used on a daily basis (i.e., radio waves, microwaves, x-rays) within a huge number of products. Even if electronic devices don't contain transmitters, they can still emit electromagnetic radiation as a byproduct of their switching voltages and currents. Without a limit on the level of radiation from these unintended emitters, the electromagnetic spectrum for intended transmission could be compromised. Safety is a huge concern when it comes to compromised spectra, especially in military, medical, aerospace, and automotive products. If products in these areas were to fail from EMI such as power surges or radiated electrical fields, then peoples lives could be at serious risk. So rigorous EMC testing ensures that electrical systems can withstand and continue to function properly in the presence of these electromagnetic environments. Fines and serious action is enforced if you are caught with a non-compliant device in the market.

Different EMI characterization methodologies have been explored by many researchers around the world [2] - [31]. EMI characterization provides quantified insights into the EMC design challenge. This quantification makes the design of EMI mitigation more oriented towards optimization and more efficient by reducing the scale and number of physical experiments, reducing simulation time, and reducing unnecessary design margins. If a method quantifies the EMI with very light weight computation, the iteration process is manageable to allow the implementation of automated optimization algorithms, such as the Virtual Prototype Process (VPP) conducted within our research team.

1.6 System Description

In our area of research, we are confronted with a wide range of power electronic converters. The dual active bridge (DAB) converter has been a hot topic in research lately and is well suited for applications in power distribution systems due to their high power density, low device stresses, galvanic isolation, and bidirectional operation. DAB converters have been considered as a candidate topology for solid-state transformers, and have been studied in context with renewable energy, automotive, aerospace, and marine power systems. A DAB bidirectional DC/DC converter is a topology with the advantages of decreased number of devices, soft switching commutations, low cost, and high efficiency. The use of this topology is proposed for applications where the power density, cost, weight, and reliability are critical factors. With its high demand in power electronics, we have directed our research towards an accurate EMI characterization and reduction methodology to support the design of the DAB as a sub module for much larger system applications.

For the main topology of this thesis, the neutral point clamped (NPC) dual active bridge has been chosen.

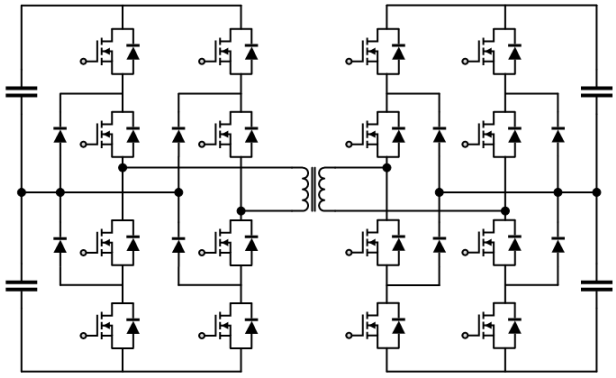

Figure 1-5: Neutral Point Clamped Dual Active Bridge

The NPC DAB is a bidirectional DC/DC converter based on two active NPC full-bridges interfaced and isolated through a medium-frequency (MF) transformer enabling power flow in both directions in case of an active load. The main reason for choosing the NPC DAB over a conventional DAB is the decrease of voltage stress on power switches, making it a prime subject for medium voltage systems. For the conventional DAB, the input and output

voltages are applied to the power switch as a voltage stress. Therefore, with increased system voltage, there will be a need for higher rated devices to withstand the increased voltage stress. In order to solve this problem, the voltage stress applied to the power switch can be distributed using a multi-level topology, where the NPC converter is the most commonly used multi-level structure. The DC link of the NPC converter is connected in series with two capacitors to ensure a neutral point voltage. Thus, the maximum voltage applied to any power switch will be half the DC link voltage. Even though the voltage stress is reduced on devices during normal operation, there is still a chance that a switch can encounter almost twice the DC link voltage during a fault. With this in mind, there is still a need for higher rated devices to make the NPC DAB a feasible option for MV voltage systems. There is much on going research in designing higher rated switching modules, specifically the 10 kV SiC module, to enable the design of the NPC DAB as a feasible option for MV distribution systems.

The NPC DAB was described as a sub module earlier, that is because the NPC DAB alone is only an isolated DC to DC converter, but the addition of other components or converters makes it a power distribution system. On the primary side we could add in a grid tied AC supply with an active front end converter, which would allow us with opportunities for vehicle charging systems or a DC distribution system for marine applications. Or we could add a DC to AC converter on the secondary side, which would allow us to tie to the AC grid for renewable energy systems. All of these will be possible applications for the future, but we should first start with an accurate characterization of the NPC DAB.

The bulk of this thesis will be around the CM EMI methodology for the NPC DAB. A CM model of the topology for EMI studies will be derived, the CM model will be validated with simulation software, and some techniques will be performed that decrease the amount of CM emissions.

1.7 Thesis Organization

A literature review on current and state of the art major modeling methods for EMI characterization performed by academic scholars and industry partners will be discussed in

Chapter 2. A computationally efficient mathematical method to isolate the common-mode paths and create equivalent circuit models for common-mode EMI conducted emissions will be discussed in Chapter 3. This method will be carried out for multiple power electronic converters including the neutral point clamped converter. An extension of this method to the high-frequency transformer will be performed and a common-mode equivalent model is developed in Chapter 4. All of the created CM equivalent models will be brought together to form a complete NPC DAB system CM equivalent model, and then validated along side a mixed-mode model created in the PLECS environment in Chapter 5. EMC testing environments and potential lab test setups is discussed, and a novel idea for reducing CM emissions within the NPC converter will also be covered in this chapter. Then finally, a summary and suggestions for future work will be described in Chapter 6.

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Chapter 2

State of the Art Methodologies

To characterize EMI produced by a power electronic converter, a model must be developed for the converter and its surrounding system with accuracy that meets system requirements and is validated within a required frequency range. To ensure compatibility with filter designs the models are mostly developed into an electrical circuit representing the dominant EMI producing behavior for the physical system.

With the aim to derive these hehavioristic models, various methodologies have been applied. In engineering we tend to break a modeling approach into three different categories; white-box modeling, black-box modeling, and gray-box modeling. Engineers use a white-box model when it is possible to describe the whole system using physical equations and data sheets. Such models have understandable, reasonable, and observable behaviors between influencing variables and output predictions. However, this is a rare type of modeling approach and is commonly used on very basic systems. The opposite of white-box is black-box modeling, where a model is estimated mathematically from a measured input and output. These models have an observable input and output behavior, but how the model works inside the black-box is more or less unknown. The third type of model is the gray-box model, which is a mixture of the white-box and black-box modeling approaches. In a gray-box model, a part of the model is estimated and the other part is described with measurements and formulas. Picking the right type of modeling approach for an application depends on many different factors.

In this literature review of behavioral models, these modeling methodologies will be described and categorized based under these three different categories.

2.1 White-box Modeling

White-box modeling is used when it is possible to describe the whole system using physical equations and information from data sheets. This modeling approach comprises the use of direct circuit modeling and simulation, and finite element method (FEM) assisted modeling.

Several direct circuit modeling methods have been developed to predict the EMI emissions of power converters [2], [3]. These methods are implemented in simulation software tools that can be used to predict the EMI noise generated up to several MHz, which is sufficient for the design of EMI filters as these are typically determined by the first switching harmonic component that falls inside the frequency range of interest. Direct circuit modeling constructs a full system circuit and maps out as much information and behavioral details as possible, with the use of measurement and data sheets for the power semiconductor components. The modeling process involves the formulation of high-frequency models for all main subsystems, including switching devices and packages, passive components, interconnections, and grounding. To account for the effect of high dv/dt in WBG devices, detailed switch models for SiC have been used. This modeling procedure is able to provide a significant EMI prediction throughout the whole system, but based on the different operating conditions, data sheets are not always valid and this could lead to misleading information. Even though these types of models can produce a significant amount of information, it is often dependent on the researchers bias and as a result could miss out on important information regrading EMI emissions.

With FEM modeling procedure, you can virtually construct entire parts of power electronic systems and compute the electromagnetic (EM) response within a designated frequency, which would otherwise be extremely hard to compute by hand using equations. Passive component models can also involve more detailed modeling phenomena, self-capacitance, or parasitics of components using FEM simulation [4], [5]. The EM response obtained from FEM can be used for the structural design of a system to reduce induced EMI from the

geometrical layout of the physical structure. This type of modeling procedure can provide a very accurate behavioral model within a desired frequency range.

Disadvantages to white-box modeling

Direct circuit modeling can provide great insight to CM EMI analysis, but often times these models are very difficult to construct for very large systems. Whereas, FEA provides little insight into CM EMI analysis. These modeling processes can tend to be very complex and very time consuming. The tuning of these models requires manual changes and a whole new simulation of the entire model, making the computational cost of these models too high to achieve an efficient iterative process.

2.2 Black-box Modeling

Black-box modeling makes use of network or impedance analyzer to acquire scattering parameters and impedance profiles for certain parts of the power electronic system. Based on the information gathered, researchers can interpret a behavioral model without the use of data sheet information or specific details of the system itself [6]. Even with many EMI prediction techniques available, the most common method for studying EMI is to do so with a black-box approach after the design process. This entails measuring the EMI followed by implementing various techniques to reduce the emissions. This often results in reduced efficiency and power density and increased cost to a product.

2.3 Gray-box Modeling

Instead of mapping out an immense amount of behavioral details like you do in the white-box modeling procedure, the grey-box modeling method only models the behavior of the major sources of EMI with measured data. These major sources of EMI are typically considered to be the switching waveforms and dominant parasitics.

Gray-box modeling started with recognition that behavioral models of the energized system are required to capture the high frequency behavior and the interaction with other parts of the system. These studies truly began with the introduction of electronic devices

into car systems. Two fundamental aspects where discovered in studying the electrical system of a car: firstly that the electronic device is disturbed by the disturbances present in the electrical network itself, secondly the device is a disturbance generator and the electrical network is the load. This recognition led to the methods used today to test for conducted emissions and complying to EMI/EMC standards. This suggested the adoption of the first LISN, or artificial network, as a means of measuring noise emission and susceptibility for electrical devices [7], [8]. The authors were able to perform laboratory measurements connected to an artificial network that represented the electrical networks used on compact passenger vehicles. The model of the electrical system was first seen as a simple impedance network with a battery source.

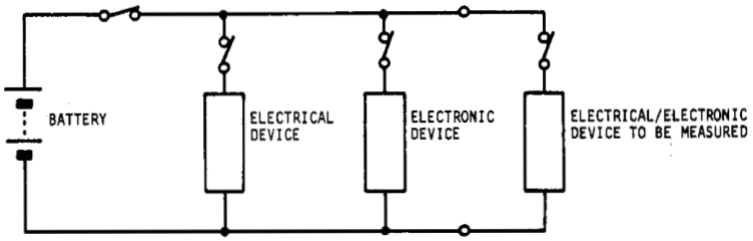

Figure 2-1: Impedance circuit of a Japanese automobile [8]

The intention was understand the noise emission and susceptibility of the device downstream from the rest of the electrical system, and be able to conduct these tests in a lab setting. So they began by measuring the impedance seen looking into the system by open circuiting the terminals of the device under test. With the impedance of the system, they created an artificial network to model this system.

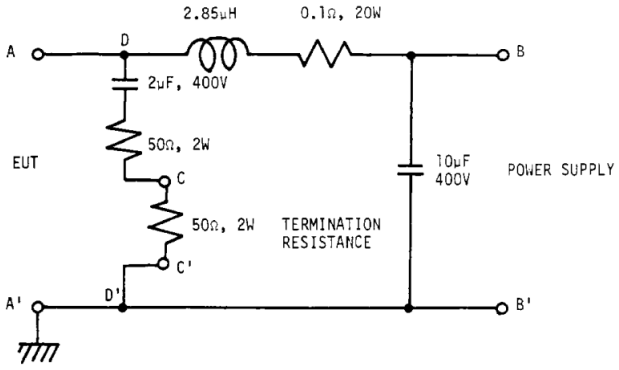

Figure 2-2: Artificial network of a Japanese automobile [8]

From comparison you can see the resemblance to the modern day LISN. Using this artificial network, the RF conducted noise measurement systems were developed for laboratory measurements of emission level from automotive electrical devices and susceptibility level of electronic devices.

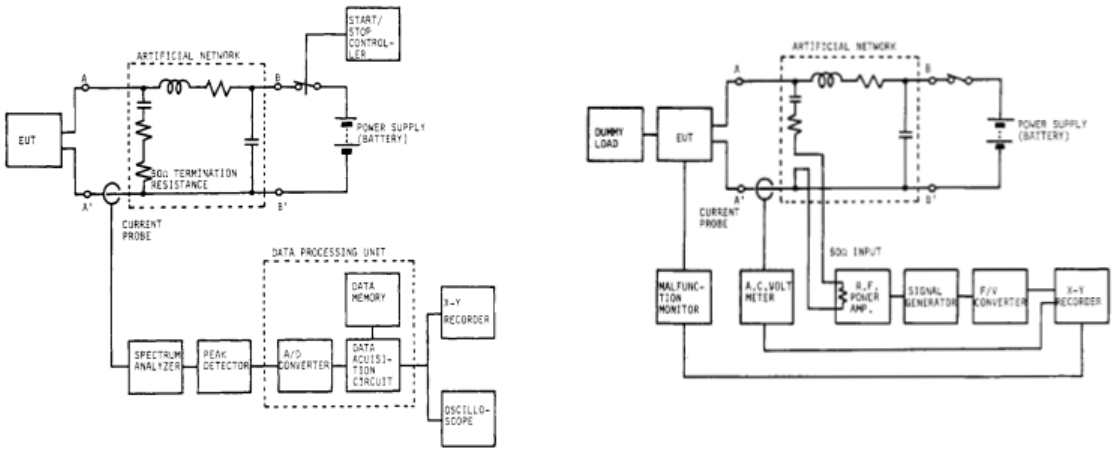

Figure 2-3: Noise and Susceptibility measurement systems using artificial network [8]

Advocates of Gray-box modeling have tried to find ways of extracting the important high-frequency characteristics, say dominant EMI producing sources, using standardized methods of accounting for interaction of the high-frequency noise producing component within a power system. For power electronic systems gray-box models were proposed that directly correlate the high-frequency stimulus to a power semiconductor in power electronic converters. This led to modeling approaches for behavioral models that represent the EMI noise source with an equivalent circuit, typically a current or voltage source or an ideal switch, together with some equivalent impedance representing parasitic impedances to model conducted emission propagation paths [9] - [12]. This type of behavioral model employs a time-invariant linear equivalent circuit, which can reduce the EMI computation and simulation time, but there are issues with modeling accuracy because of the simplifications involved. This oversimplification can lead to to errors in the higher frequency range. These behavioral models also characterize EMI noise source into separate CM and DM noise sources to understand the noise generation and propagation behavior, but this is based on

the assumption that there are no interactions between these noise sources.

This led to terminal gray-box modeling approach to be performed [13] - [18]. This consisted of two and three terminal modeling to separate CM and DM equivalent circuits. The terminal models were developed to overcome the oversimplified aspects of previous models. The basic concept is to model the EMI emission from a switching module via a Thevenin or Norton equivalent source consisting of equivalent voltage or current sources and equivalent source impedances.

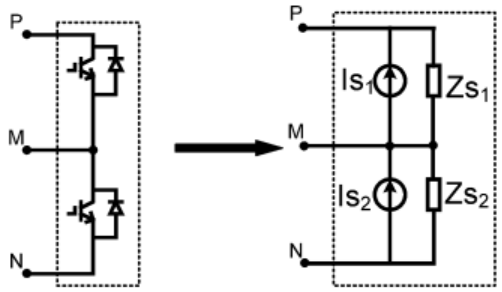

Figure 2-4: Equivalent Norton circuit for a switching phase leg module [14]

The model includes two noise current sources and two noise source impedances. The noise sources are connected with external circuit propagation path via the three terminals. The equivalent model can represent various switching patterns of this phase leg module. Different from existing modeling approaches, this method does not populate a source using assumed switching waveforms and estimated parasitic impedances. Instead, the equivalent current source and impedance are established through standardized tests and a characterization process under the specified operating conditions.

A two terminal model is a DM model, and is evaluated first since the concepts are easier to visualize and understand. The Norton equivalent circuit in Figure 2-5 is usually chosen since it closely represents the physical representation of a DM system. The model is created by using a nominal case and an attenuated case (shunt). Typically, the Norton equivalent parameters are defined by short- and open-circuit conditions, but this cannot be done for an operating converter. That is why a second measurement that is different from the nominal case is imposed. With the knowledge of the shunt impedance and the difference between the two terminal voltages, the unknown equivalent circuit can be solved.

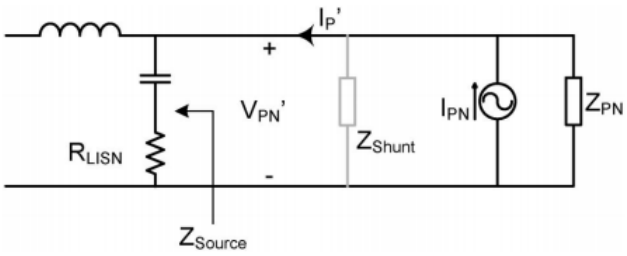

Figure 2-5: Two terminal model [17]

A three terminal model is composed of three impedances and two sources, because there must be an impedance between every terminal.

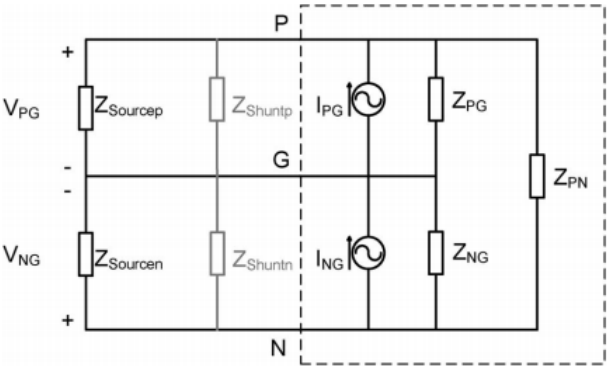

Figure 2-6: Three terminal model [17]

Similar to the two terminal case, the model is created by using a nominal case and at least two attenuated cases. There are several different attenuation schemes that can be implemented, but at least two attenuated cases along with the nominal system will provide enough information to solve all the unknowns. With the knowledge of the shunt impedances and source impedances along with the difference between the terminal voltages the unknown equivalent circuit can be solved.

The difference between the three and two terminal models is the method of solving for the unknowns. The two terminal model is a trivial case where there are two equations and two unknowns with an explicit solution. The three terminal model has many determining factors that have to be taken into account. Therefore, they impose a method to solve an over-determined system of nonlinear equations to minimize the error.

It took a year of refining this method but they eventually addressed the quality and challenges of EMI terminal modeling technique for switching power converters and extended

the modeling technique to three phase AC systems [19]. They were able to show that the models are accurate even outside the conducted emissions range, making it a promising modeling technique.

The mixed-mode noise had been studied and there is an effective method of filtering conducted EMI separately by CM and DM, where each noise is dealt with the respective section of the EMI filter. But the fundamental mechanism by which the mixed-mode noise is excited and coupled had not been adequately investigated. The recognition of mixed-mode effects was eventually modeled and analyzed for conducted emissions at higher frequencies [20]. It wasn't until the unterminated behavioral model and the common-mode equivalent models with dominant parasitics that truly were able to predict conducted emissions at higher frequencies when mixed mode noise becomes significant.

2.3.1 Unterminated Behavioral Modeling

Behavioral models are usually based on Thevenin or Norton equivalents. The two-terminal and three-terminal models were used in the past to model the CM and DM noise separately in the power converters. But it has been shown that these models have a limitation when mixed mode noise becomes significant at higher frequencies, which is usually the case with converters that are asymmetric with respect to ground. These models were also treated as one-port models and have a limitation that they can only model the input-side EMI of power converters. Since these models are extracted for specific load conditions, they are referred as "terminated" behavioral models. In certain EMI standards they authorize limits on conducted emissions for all power lines and interconnecting cable bundles. Thus, for converters where coupling between the input and output side is significant, there is a need for an "unterminated" EMI model that not only predicts the interaction of EMI on both sides but also predicts changes in EMI at the input side due to changes on the load side parameters and vice versa.

This change from terminal to termination nomenclature brought in a new behavioral modeling approach where power converters are modeled instead as multiterminal networks, single-port or two-port, using an impedance network and a number of sources to model their operation. This new behavioral model builds up a thevenin equivalent circuit representation

without knowledge of the converter internal structure, with more of a black-box approach implemented. The impedance and sources are obtained empirically by directly performing a series of standardized measurements, which are conducted from the terminals of the converter in accordance with the multiport network theory. This behavioral modeling approach has been studied in great detail and has evolved into unterminated behavioral models for predicting conducted emissions at higher frequencies with mixed mode coupling [21] - [23].

For power converters, single-port behavioral models were first developed to predict the EMI noise in converter structures. In [22], the authors explain the limitations of using single-port terminal behavioral models and propose a mixed-mode unterminated behavioral model. Their research was toward motor drive applications, which meant that the converter topology used was the power inverter system.

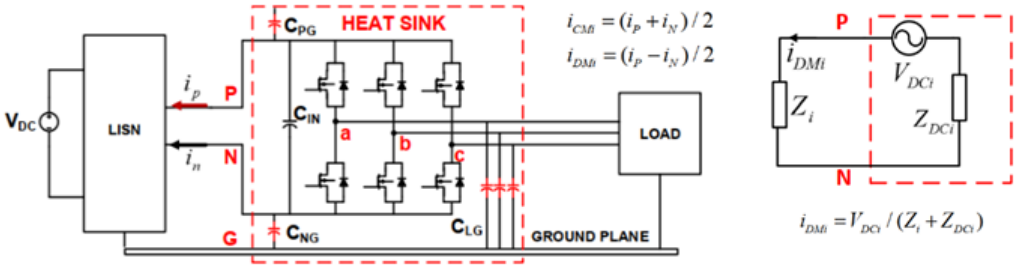

Figure 2-7: Three phase inverter and DM one-port terminal model [22]

Figure 2-7 shows a DM power inverter system under study that was used to predict DM EMI noise. The one-port terminal model used to predict DM noise at the inverter input side, and is composed of one noise source and one equivalent impedance. The impedance is dependent on the DC bus capacitor at low frequency and its equivalent series inductance at the high frequency part, while the voltage represents the switching effect of the active devices. The input impedance represents the impedance outside the inverter on the input side, which includes the LISN. With the extracted model, the DM input noise can be calculated with different input impedances. A three-phase SiC MOSFET inverter setup was built to asses the feasibility of the EMI modeling technique. The prediction matched the measurement results only during low frequency harmonics, at higher frequencies the model failed to capture the system input DM noise. Experimentally, they found out that the DM input noise is coupled with CM noise and is dependent on the CM noise propagation

path in the system. Thus, they concluded that the one-port terminal model fails to predict the DM input noise precisely when the CM and DM noise is coupled.

To include the CM parts in the DM model, they developed a mixed-mode unterminated behavioral model that includes the entire propagation path, including the parastics which are the main propagation paths of the CM noise for the inverter input side.

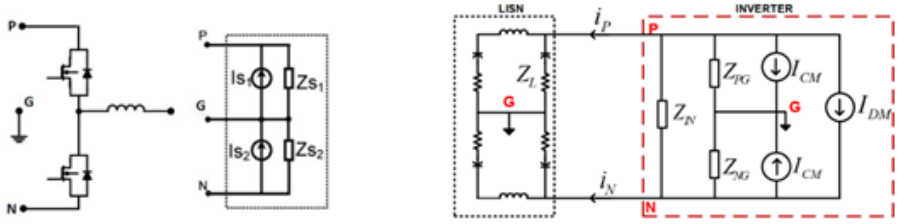

Figure 2-8: Modular terminated model and proposed DM model with LISN [22]

The model originated from the modular terminated model which was proposed to predict conducted noise in one phase leg system. It uses two noise sources and two impedances to describe the one leg, it was then extended to the three-leg system. Z_{PG} and Z_{NG} are mainly dependent on C_{PG} and C_{NG}, and a third impedance Z_{IN} is added to represent the DC bus capacitor. The noise sources are separated into CM and DM noise sources to help show how the noises are generated. The input DM noise is independent on the CM propagation when the system is strictly symmetric. In the asymmetric system, the CM propagation effects the DM noise. Compared to the one-port terminated model, the new unterminated model has one more source to include the CM noise source effect, and two more impedances to consider the propagation path form the inverter to the CM ground. The authors conclude through experiment, that when the system is strictly symmetric, there is no mixed CM noise in the DM loop, and the one-port model is a viable option. Otherwise, the mixed-mode unterminated model is an effective tool in predicting DM noise throughout the entire conducted EMI noise range.

This unterminated behavioral model has evolved over many years since the first unterminated common-mode EMI model proposed in [21], they eventually addressed the concern that the previous models cannot predict changes in the input side EMI due to the change in load side parameters. For converters where the coupling between the input and output

side EMI is significant, there is a need for a unterminated model that not only predicts EMI on both sides but also predicts changes in EMI at the input side due to changes in the load side parameters. This intrinsic requirement of any DM-only or CM-only EMI model is not applicable when predicting the EMI behavior of power converters using WBG power semiconductors which heightens the sensitivity of the circuit layout for previously negligible parasitic components. Which effectively rendered the derivation procedure previously developed for these models ineffective. To address this shortcoming, they introduced a high-frequency unterminated behavioral model to predict the conducted CM EMI emissions of WBG-based power semiconductors [23]. Using the same circuit schematic of the SiC MOSFET-based three-phase inverter used as a test bed seen in Figure 2-7. They proposed a high-frequency unterminated behavioral model that captures the CM circuit behavior of the three-phase inverter, which is highlighted in the dashed red box in Figure 2-9

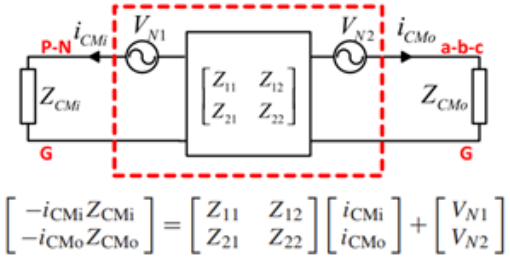

Figure 2-9: CM Unterminated-behavioral model [23]

The distinct feature of the unterminated modeling approach is that it enables the prediction of EMI under different input and output terminal configurations. The model structure comprises two noise sources and two-port impedance network elements. The figure also shows the total CM impedance seen by the inverter at its dc terminals, and the corresponding output CM impedance. This model can be formulated in closed form. With the unterminated behavioral model in place the extraction process is done empirically, where the extraction procedure can be summarized as follows. First, measure the inverter impedances in the power-off state with a vector network analyzer. These measurements yield a close estimation of the impedances under the assumption that the impedance of the switching devices is sufficiently large. Secondly, the noise sources cannot be directly measured, so a standardized test is performed in which a CM choke is placed at the input and output

of the inverter to swamp out the inverter impedance in the conducted EMI range. This yields a high accuracy approximation for the noise sources. Once the impedance network is measured and the noise sources are obtained, the unterminated behavioral model can be used to predict the inverter CM current with different input and output configurations. Next, a second standardized test is performed to compensate for the approximated nature of the inverter impedances and thus inmprove the model accuracy. In this test, the inverter CM currents are measured with shunt impedances at both the input and output terminals of the inverter. These impedances are much smaller than the inverter impedances in the range of conducted emissions. The CM currents are then calculated for this test using the unterminated behavioral model parameters. Finally, comparing these values to the measured quantities, an optimization procedure can be applied to compensate the inverter impedances.

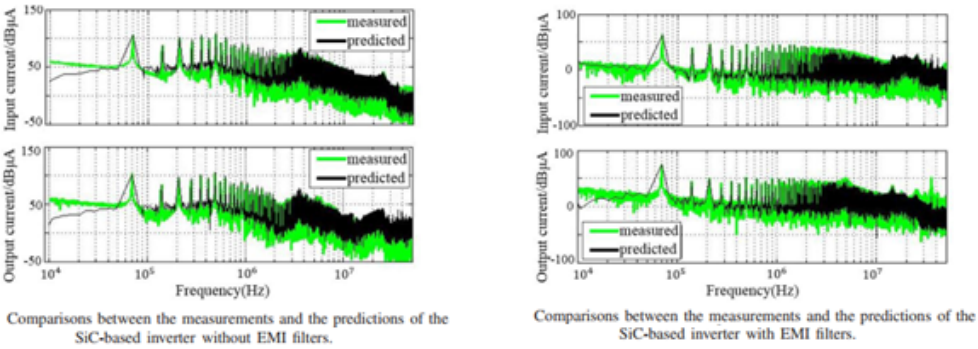

Figure 2-10: Measured and predicted input and output CM current spectra where SiC inverter was operating without and with CM filters [23]

The proposed high-frequency unterminated behavioral model was validated on the SiC-based inverter setup. Figure 2-10 show the measured and predicted input and output CM current spectra where the SiC inverter was operating without and with CM filters. It can be observed that the models extracted matched very well with the spectra measured up to 30 MHz.

This process provides a very accurate prediction of EMI in CM and DM generated by an inverter, but it is empirically driven and the overall process is not very straight forward or easy to accomplish. It has truly gotten away from the idea of gray-box modeling and has implemented a black-box behavioral model. This process also does not quantify the rela-

tionship between EMI and the circuit parasitics or really any inner workings for the system. With being empirically driven is is practically impossible to model the difference between different circuit topologies (i.e., two-level full-bridge, NPC, floating ground reference, or transformer) without producing a hardware setup for every case scenario.

2.3.2 CM Equivalent Modeling with Dominant EMI Sources

From a design perspective, one would prefer to reduce CM voltage/current just enough to meet relevant reliability, safety, and emission standards. But, for large complex systems, establishing the optimal location and degree of such mitigation remains a challenge. To support CM analysis and design, one modeling approach is to derive CM equivalent circuits in which the dominant parasitic paths are parameterized and coupled to CM voltage sources that represent the impact of power electronic switching [24] - [26]. This approach has computational advantage, since the need to identify switching instants through simulation is eliminated and techniques for linear circuit analysis are applied to predict CM behavior.

A formalized approach was proposed where the CM voltage is defined with respect to an arbitrary reference [24]. This method leads to a straight forward transformation of mixed-mode power system models into their corresponding CM equivalent circuits. With this, there is a simple connection of these CM equivalent components that can be used to form the CM models for an entire system. The method was demonstrated and validated by comparing results of the proposed CM modeling approach with a detailed mixed-mode simulation of an example ship power system.

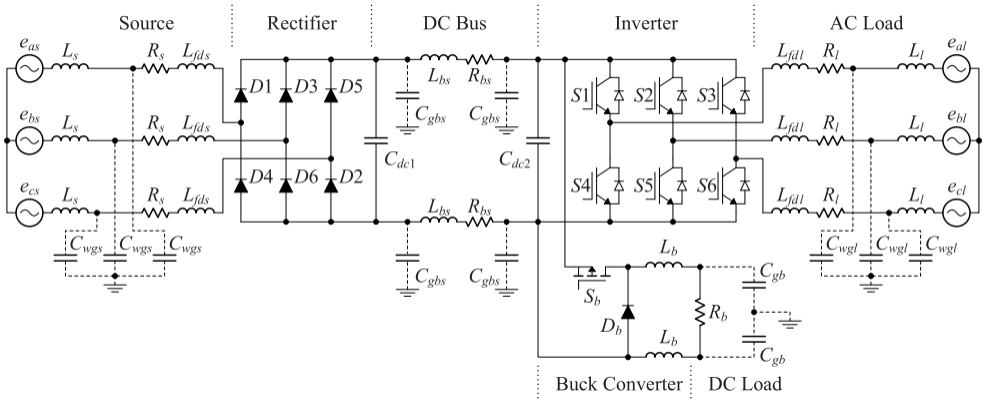

Figure 2-11: DC based ship power system [24]

The first step in the proposed method is to generate a CM equivalent circuit for each component of the power system. The general procedure for producing such an equivalent circuit from the component's DM model is broken into three steps. First, parasitic couplings that provide paths for CM currents are identified and added to the DM model to form a mixed mode model. Secondly, line voltages for the mixed mode model are determined with respect to an arbitrary reference point. Lastly, the line voltages are averaged, and the CM definitions are applied. Once this is applied to each component of the power system, the connection of each system is pieced together to form a CM equivalent circuit for the entire system.

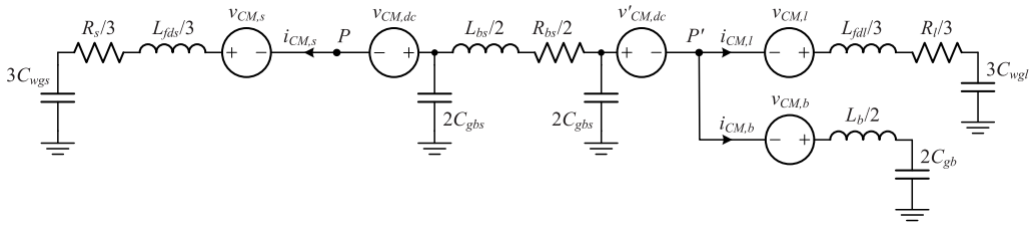

Figure 2-12: CM equivalent circuit for ship power system [24]

To validate the CM analysis, a time-domain simulation was performed for the detailed mixed-mode model of the ship power system. All of the CM voltage inputs to the model were determined analytically from the steady-state DM operating point of the system. Some of the simulation waveforms are produced from the detailed and CM equivalent model and are used for validation purposes, and these results can be seen in Figure 2-13.

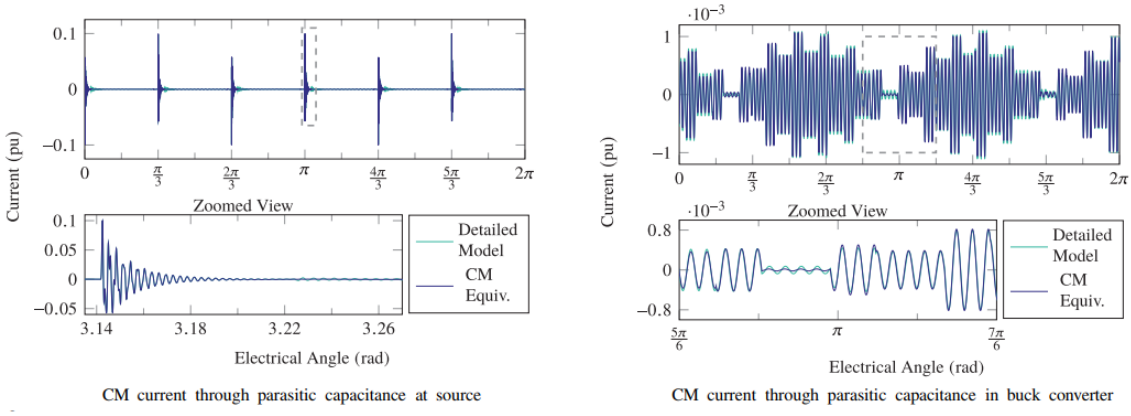

Figure 2-13: CM currents through parasitic capacitance at source and in buck converter [24]

The plots shown are the CM current through parasitic capacitance at the source and in the buck converter. A highly accurate relationship was observed between the mixed-mode model and the CM equivalent circuit results. They stated that the minor discrepancies were the result of approximating the CM voltage inputs to the equivalent circuit model, and that they would disappear entirely when simulated CM voltages are used as inputs.

The authors were able to successfully employ an equivalent circuit transformation to model the system level CM behavior of a symmetrical DC microgrid with multiple converters and CM loads. Due to the accuracy, ease of use, and computational efficiency that this method ensured, it started to gain traction for EMI studies. Soon after, they provided an extension to their work in modeling EMI behaviors by employing an equivalent circuit based modeling framework to quantify the common-mode to differential-mode coupling that is observed in asymmetric converter structures [25]. Converter structures that are symmetric from the system view may be found to have significant CM/DM coupling due to parasitic imbalances, which are usually thought to be negligible in analysis involving non-WBG systems. The authors presented a theoretical treatment of CM and DM interaction that is known to exist in switch-mode converter systems, and demonstrated that displacement currents through module baseplate can be quantitatively predicted through theoretical analysis based on asymmetry in the converter system. The authors also developed an empirical test platform for the evaluation and characterization of conducted emissions in converter systems based on WBG semiconductors.

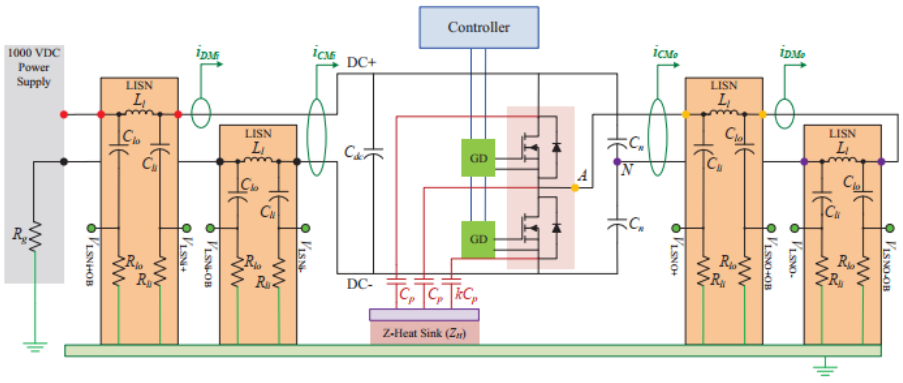

Figure 2-14: Half-bridge testbed for characterization of conducted EMI [25]

The custom designed EMI characterization platform in Figure 2-14 uses an unorthodox

configuration of LISN's on both the input and output of the converter. This configuration allows observation of the conducted emissions generated by the converter, which is a half-bridge in this setup. By taking the difference of the input and output CM currents, they were able to determine the displacement current through the baseplate of the module.

To produce the CM equivalent circuit, the mixed mode model in Figure 2-14 was split into three sections: the input LISN, output LISN, and module parasitics. The arbitrary reference point chosen was A and each section produced a branch that originate from this point. Each branch consists of a equivalent CM impedance and CM voltage source, following the systematic approach described in [24]. The only difference is that the module parasitic branch includes an additional "parametric" voltage source that results from the asymmetry between the three components of the module baseplate capacitance. The resulting CM equivalent circuit is shown in Figure 2-15, this "parametric" voltage source is the DM coupling into the CM circuit.

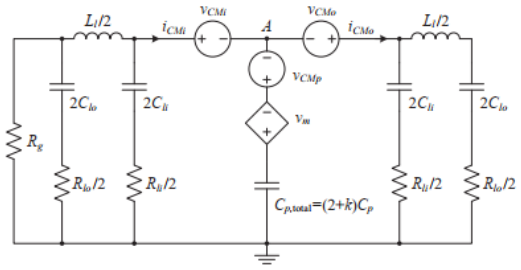

Figure 2-15: CM equivalent circuit of half bridge testbed [25]

This DM coupling voltage source is distinguished from the CM sources in the CM circuit as a dependent voltage source, seen in the middle branch. The CM equivalent model was validated using a time-domain simulation, and provided near perfect agreement between the two. The authors narrowed down two key features of the module that influence the CM current through the baseplate: the asymmetry of the capacitance and the total capacitance. The recognition of these key features is important to designers for the purpose of system optimization, especially WBG converters.

With the near perfect agreement between the developed CM equivalent models and time-domain simulation for modeling conducted emissions in asymmetric power electronics eventually led to a generalized approach for building up these CM equivalent models [26].

The generalized approach allowed for the decomposition of mixed-mode conducted emissions in power electronic systems into their differential and common-mode components. The decomposed system of equations provides mathematical descriptions of differential and common-mode couplings induced due to asymmetries in the system.

This method provides an accurate prediction of CM and DM conducted emissions in symmetrical and asymmetrical systems. The CM equivalent circuit contains accurate and mathematical information for the CM and DM coupling. Making this method a very powerful tool for EMI characterization, CM conducted emissions, filter design, and system optimization. The method has extended efforts for EMI mitigation in uninterruptible power supplies [27], EMI characterization and modeling of a neutral point clamped half-bridge module [28] - [29], in depth modeling and validation of a half-bridge inverter [30], and cancellation of leakage current through the half-bridge module baseplate capacitance [31].

This work has stayed true to the idea of gray-box modeling and the continued efforts has paved the way for future extensions to this methodology.

2.4 Transformer Modeling

The medium frequency transformer is a critical component of the isolated DC/DC converters in higher frequency, medium-voltage operation. The operating conditions of the MF transformer strongly influence its design. Therefore the design of a MF transformer requires thorough and careful considerations to ensure an optimum electrical and magnetic utilization, an acceptable level of electrical, magnetic, and thermal stress, as well as minimized parasitic parameters [32]. Winding, core, and dielectric losses are frequency and waveform dependent and influence the choice of winding conductor and core material. Accurately estimating the copper losses is vital for the design of MF transformers used in MV isolated DC/DC converters. Higher edge rates on the transformer windings makes the classical analytic method for calculation of copper losses inaccurate. An accurate evaluation of MF copper losses in layered windings through 2-D FEM simulations to establish semi-empirical formulas has been proposed [33]. The insulation also plays an important role when designing MV converters where high isolation levels are required. The design

and impact of the insulation on the performance of the MF MV transformer has been studied, and a proposed insulation design for MV transformer has been developed [34]. The winding arrangement determines the electrical parameters of the transformer, such as its leakage inductance and parasitic capacitances, and thus the higher frequency behavior of the transformer. The calculation of a transformer's parasitics is fundamental for predicting the frequency behavior for a device, and reducing EMI effects. The extraction and calculation of self-capacitance [35], leakage inductance and parasitic capacitance [36], and couplings between windings, core, and enclosures [37] have been developed. These calculation processes use FEM extraction and semi-empirical formulas.

In an isolated power converter, the winding parasitic capacitance of the MF transformer plays a critical role for generating CM noise. Switch converters generate high edge rates for voltage and current waveforms due to the high frequency switching action. The CM noise is created by the displacement current which flows on the voltage pulsating node of the circuit to ground through the parasitic capacitance. In general, the leakage inductance of the transformer should be relatively small to achieve high efficiency and reliability for the converter. Therefore, tight coupling of the windings is usually produced, meaning that the windings need to be close in proximity. Consequently, the inter-winding capacitance becomes relatively large due to the adjacent winding structure. With the pulsating voltage on the transformer windings applied to these large distributed parasitic capacitances, a large displacement current is generated, which flows through leakage paths returning to ground, resulting in large CM noise. Currently, there are a few available methods for suppressing the CM noise in isolated power converters which can be categorized into frequency modulation techniques, soft switching techniques, displacement current cancellation techniques [38] - [39], and shielding techniques [40].

Although it is known that parasitic capacitance plays a critical role in generating and coupling CM noise, efforts have primarily focused in mitigating CM noise in transformers and little effort has gone into EMI characterization or prediction of CM emissions. Currently there are two and three capacitor equivalent models for winding parasitic capacitance [41] - [43], but these models tend to be oversimplified and use assumptions to qualify them as equivalent models. A more sophisticated method for analyzing CM noise in isolated power

converters has been proposed [44], where a generalized lumped capacitance model of the inter-winding capacitance is paired with equivalent noise source. This method is based on thevenin theory and is verified with experimental results.

The only problem with these methods is that they are primarily focused on the inter-winding capacitance and lack knowledge in leakage paths that may cause asymmetrical current distributions through the transformer. There isn't much mathematical information outlining the EMI behavior of the coupling or leakage paths, and the models aren't easily applied to other CM models to conduct full system analysis.

With the gray-box modeling technique, more importantly the CM equivalent modeling technique, explained in the previous section there are ways of providing a formalized mathematical approach to understanding the EMI behavior of the transformer. This method would extract dominant EMI sources from the transformer for an elevated understanding and should quantify insights into the EMC design challenge.

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Chapter 3

Common Mode Modeling of Asymmetric Power Electronic Systems

In general, black-box methodologies lack high-frequency accuracy, and white-box methodologies are a burden on computation power and time. To balance the analysis accuracy and simulation efficiency, the grey-box methodology is best suited for EMI characterization of the NPC DAB. More specifically, the CM equivalent modeling technique will be extended and performed for our system topology. This modeling methodology establishes a mathematical equivalent circuit modeling technique where the dominant EMI sources are measured in hardware for an accurate prediction of conducted emissions, providing a computationally efficient method for EMI characterization.

A systematic Common-Mode (CM) modeling approach was proposed where the objective was to define a CM voltage with respect to an arbitrary reference point which is *distinct* from ground [24] - [26]. This "extra" floating reference makes it possible for the transformation of Mixed-Mode (MM) system components into CM equivalent components which can then be systematically assembled to form CM equivalent models. The equivalent circuits accurately model the effects of mutual coupling between common-mode and differential-mode voltages and currents due to circuit asymmetry. In *symmetric* systems, the Differential-Mode (DM) and CM are fully decoupled, whereas in *asymmetric* systems, the DM definitions are integral in understanding the CM behavior.

The intent of this chapter is to inform the reader on the CM modeling approach by

linearly transforming MM line-to-ground voltage equations to a "decomposed" Differential-Common-Mode (DCM) set of DM equations that are independent of ground and a CM equation describing the average behavior of the lines with respect to ground. This DCM system explicitly provides the coupling relationships between the differential and common modes induced by asymmetries between the lines, which provides us with greater insight in CM conducted emissions. Most CM modeling procedures produced in the past disregard this DM coupling into the CM circuit because they believe that is it negligent or are just interested in finding a close approximation. But this procedure gives us more than just an approximation, it gives us a mathematical expression in understanding what causes the DM coupling and possible methods in mitigating conducted CM emissions.

The chapter will have the following layout. First, the methodology for the approach used to derive CM models will be covered; wherein CM and DM definitions will be established, the derivation of voltage and current matrices will be produced and a CM expression will be extracted, and then all of it will be brought together to form a Common-Mode Equivalent Model (CEM). A generalized approach for the derivation of parasitic capacitor voltages in power electronic converters will also be established. Once the foundation is set, CEMs for commonly used power electronic converters will be developed. The NPC full-bridge converter will be the focal point and will eventually be paired with the Dual Active Bridge. The next chapter will provide the modeling of the High-Frequency Transformer, which will then provide us with a complete model of the Dual Active Bridge for testing and validation purposes.

3.1 Methodology

To understand the approach used to derive CM models, let us look at a simple example of a transmission line model with N set of lines.

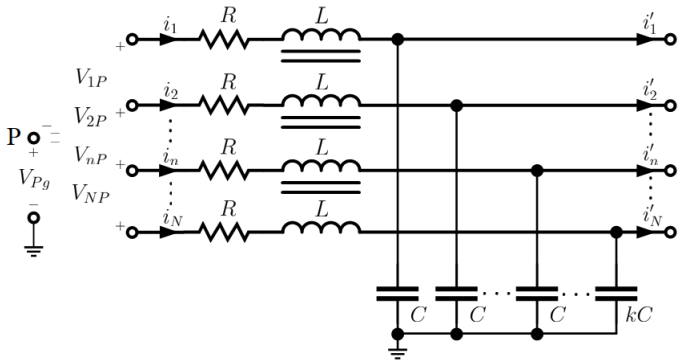


Figure 3-1: Transmission Line Model

3.1.1 Common-Mode and Differential-Mode Definitions

The circuits employed in electronic equipment almost always use differential-mode currents. In differential mode, current is carried from a source to a load on one conductor, and the return current is carried form the load back to the source on the second conductor. The return current from load to source should be equal in magnitude to the signal current from source to load, leaving a net current of zero for the two conductors combined.

Common mode currents are currents that flow in the same direction on two or more conductors. The return current for a common mode circuit is typically carried on a reference conductor or ground plane. Common mode currents are almost always unintentional and often arise due to imperfections or imbalance in differential mode circuits, particularly when the return current for a differential mode circuit finds an unintended return path from the load back to the source. Current flowing in these unintended paths creates a non-zero current in the conductors that were intended to carry only a differential mode current. This non-zero net current can be seen as a common mode current that is superimposed on the differential mode current carried in the conductors.

We can then define Differential-Mode (DM) operation as the signals or noise that flow in opposite directions in a pair of lines. This modeling approach defines the DM current

and voltage, for any pair of the N lines in Figure 3-1, as

$$i^{(d)}_{n(n+1)} \triangleq \frac{1}{N_i}\left(i_n - i_{(n+1)}\right) \tag{3.1}$$

$$V^{(d)}_{n(n+1)} \triangleq V_{nP} - V_{(n+1)P} \tag{3.2}$$

where, N_i is a specified normalization factor.

The Common-mode (CM) operation is defined as signals or noise that flow in the same direction in a pair or set of multiple lines. For a set of N lines, the CM current and voltage, when defined with respect to an arbitrary reference point P as shown in Figure 3-1, are

$$i^{(c)} \triangleq \sum_{n=1}^{N} i_n \tag{3.3}$$

$$V^{(c)} \triangleq \frac{1}{N}\sum_{n=1}^{N} V_{nP} \tag{3.4}$$

The voltage and current definitions result in $N-1$ DM expressions and one CM expression for the set of N lines. These definitions can be expanded to a $N \times N$ matrix with linear transforms that go from Mixed-Mode (MM) quantities to decomposed DM and CM quantities. These linear voltage and current transformations are expressed as,

$$\mathbf{i}^{(dc)} \triangleq \mathbf{T}^{i}_{N}\mathbf{i}_n \tag{3.5}$$

$$\mathbf{V}^{(dc)} \triangleq \mathbf{T}^{v}_{N}\mathbf{V}_{nP} \tag{3.6}$$

where $\mathbf{i}_n$ and $\mathbf{V}_{nP}$ are the vectors of the MM line currents and voltages, and $\mathbf{i}^{(dc)}$ and $\mathbf{V}^{(dc)}$ are the vectors of decomposed DM/CM currents and voltages, respectively. If we were to expand the vector expression seen in Equation 3.5 we would have,

$$\begin{bmatrix} i_{n(n+1)} \\ \vdots \\ \vdots \\ \vdots \\ i_{(N-1)N} \\ i^{(c)} \end{bmatrix} \triangleq \begin{bmatrix} \frac{1}{N_i} & -\frac{1}{N_i} & 0 & 0 & \dots & 0 \\ 0 & \frac{1}{N_i} & -\frac{1}{N_i} & 0 & \dots & 0 \\ \vdots & \ddots & \ddots & \ddots & \ddots & \vdots \\ \vdots & \ddots & 0 & \frac{1}{N_i} & -\frac{1}{N_i} & 0 \\ 0 & \dots & \dots & 0 & \frac{1}{N_i} & -\frac{1}{N_i} \\ 1 & 1 & \dots & \dots & 1 & 1 \end{bmatrix} \begin{bmatrix} i_n \\ \vdots \\ \vdots \\ \vdots \\ \vdots \\ i_N \end{bmatrix} \tag{3.7}$$

Again, N_i is a specified normalization factor and the choice of N_i is not unique. For example, one may define $N_i \triangleq \sqrt[N-1]{N}$ in order to achieve $\left|\mathbf{T}_n^i\right| = 1$, which is a unimodular matrix. A unimodular matrix is a integer matrix that guarantees that its inverse exists, is an integer matrix, and it itself is unimodular. They are highly desirable for transformations, since a unimodular matrix $\mathbf{A}$ represents a one-to-one mapping, and has the property that $\mathbf{xA}$ is an integer vector if and only if $\mathbf{x}$ is an integer vector.

Present work utilizes $N_i \triangleq 2$ since it yields DM circuit elements that are simple series combinations of their respective MM constituents for symmetric lines. Such that,

$$\underbrace{\begin{bmatrix} i_{n(n+1)} \\ \vdots \\ \vdots \\ \vdots \\ i_{(N-1)N} \\ i^{(c)} \end{bmatrix}}_{\mathbf{i}^{(dc)}} \triangleq \underbrace{\begin{bmatrix} \frac{1}{2} & -\frac{1}{2} & 0 & 0 & \dots & 0 \\ 0 & \frac{1}{2} & -\frac{1}{2} & 0 & \dots & 0 \\ \vdots & \ddots & \ddots & \ddots & \ddots & \vdots \\ \vdots & \ddots & 0 & \frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \dots & \dots & 0 & \frac{1}{2} & -\frac{1}{2} \\ 1 & 1 & \dots & \dots & 1 & 1 \end{bmatrix}}_{\mathbf{T}_N^i} \underbrace{\begin{bmatrix} i_n \\ \vdots \\ \vdots \\ \vdots \\ \vdots \\ i_N \end{bmatrix}}_{\mathbf{i}_n} \tag{3.8}$$

$$\underbrace{\begin{bmatrix} V_{n(n+1)} \\ \vdots \\ \vdots \\ \vdots \\ V_{(N-1)N} \\ V^{(c)} \end{bmatrix}}_{\mathbf{V}^{(dc)}} \triangleq \underbrace{\begin{bmatrix} 1 & -1 & 0 & 0 & \dots & 0 \\ 0 & 1 & -1 & 0 & \dots & 0 \\ \vdots & \ddots & \ddots & \ddots & \ddots & \vdots \\ \vdots & \ddots & 0 & 1 & -1 & 0 \\ 0 & \dots & \dots & 0 & 1 & -1 \\ \frac{1}{N} & \frac{1}{N} & \dots & \dots & \frac{1}{N} & \frac{1}{N} \end{bmatrix}}_{\mathbf{T}_N^v} \underbrace{\begin{bmatrix} V_{nP} \\ \vdots \\ \vdots \\ \vdots \\ \vdots \\ V_{NP} \end{bmatrix}}_{\mathbf{V}_{nP}} \tag{3.9}$$

It should be noted that although $\mathbf{T}_N^i \mathbf{i}_n$ and $\mathbf{T}_N^v \mathbf{V}_{nP}$ are not unique, they specify an in-

dependent set of modes. In mathematics, a uniqueness theorem asserts the uniqueness of an object satisfying certain conditions. So, there are multiple solutions to these transformations but once the conditions are set (i.e. N_i, voltage vector, and current vector), then there is only one solution based on these conditions.

3.1.2 Derivation of Voltage and Current Matrices

Applying Kirchhoff's Voltage Law (KVL) to the transmission line model example in Figure 3-1, a matrix equation can be written for line-to-ground voltages in terms of an arbitrary reference point, P, as

$$\mathbf{V}_{nP} + V_{Pg}\left[1\ 1\ \cdots\ 1\right]^{\mathrm{T}} = \left(\mathbf{R} + \hat{p}\mathbf{L}\right)\mathbf{i}_n + \frac{1}{\hat{p}}\mathbf{S}\left(\mathbf{i}_n - \mathbf{i}'_n\right) \tag{3.10}$$

where $\mathbf{R}$, $\mathbf{L}$, and $\mathbf{S}$ are the resistance, inductance, and elastance (inverse of capacitance) matrices, respectively. These impedance's relate the line current, $\mathbf{i}_n$, to the line-to-ground voltages, $\mathbf{V}_{nP} + V_{Pg}$, where $\hat{p}$ is the heavyside operator (d/dt). We can start decomposing the MM equations into a system of DM and CM equations by first left-multiplying by the voltage transformation matrix, $\mathbf{T}_N^v$, resulting in

$$\mathbf{T}_N^v\mathbf{V}_{nP} + \mathbf{T}_N^v V_{Pg}\left[1\ 1\ \cdots\ 1\right]^{\mathrm{T}} = \mathbf{T}_N^v\left(\mathbf{R} + \hat{p}\mathbf{L}\right)\mathbf{i}_n + \frac{1}{\hat{p}}\mathbf{T}_N^v\mathbf{S}\left(\mathbf{i}_n - \mathbf{i}'_n\right) \tag{3.11}$$

There is a very subtle yet important thing to notice about Equation 3.11, and that is the operation with $\mathbf{T}_N^v$ on $V_{Pg}\left[1\ \cdots\ 1\right]^{\mathrm{T}}$. To make this apparent, let us consider a scenario where we have a 3 line model

$$\mathbf{T}_3^v\ V_{Pg}\left[1\ 1\ 1\right]^{\mathrm{T}} = \left[0\ 0\ V_{Pg}\right]^{\mathrm{T}} \tag{3.12}$$

In matrix representation, we have

$$\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} V_{Pg} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} = V_{Pg} \begin{bmatrix} 1-1+0 \\ 0+1-1 \\ \frac{1}{3}+\frac{1}{3}+\frac{1}{3} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ V_{Pg} \end{bmatrix} \tag{3.13}$$

The importance is that V_{Pg} vanishes from all but the CM equation, which indicates the independence of the differential modes from the ground and the CM reference. We can thus represent Equation 3.11 as

$$\mathbf{V}^{(dc)} + V_{Pg}\left[0\ 0\cdots 1\right]^{\mathrm{T}} = \mathbf{T}_N^v\left(\mathbf{R} + \hat{p}\mathbf{L}\right)\mathbf{i}_n + \frac{1}{\hat{p}}\mathbf{T}_N^v\mathbf{S}\left(\mathbf{i}_n - \mathbf{i}_n'\right) \tag{3.14}$$

With the voltage transformations in place we now need to apply the current transformations, but it is not as simple as just applying our current transformation to the MM currents because we still need to operate on our impedance matrices. So we provide a little math manipulation through the use of the transformation inverse, noted below

$$\begin{aligned}\left(\mathbf{T}_N^i\right)^{-1}\mathbf{i}^{(dc)} &= \mathbf{T}_N^i\mathbf{i}_n\left(\mathbf{T}_N^i\right)^{-1}\\ \left(\mathbf{T}_N^i\right)^{-1}\mathbf{i}^{(dc)} &= \mathbf{i}_n\end{aligned} \tag{3.15}$$

Now substituting Equations 3.15 into Equation 3.14,

$$\mathbf{V}^{(dc)} + V_{Pg}\left[0\ 0\cdots 1\right]^{\mathrm{T}} = \mathbf{T}_N^v\left(\mathbf{R} + \hat{p}\mathbf{L}\right)\left(\mathbf{T}_N^i\right)^{-1}\mathbf{i}^{(dc)} + \frac{1}{\hat{p}}\mathbf{T}_N^v\mathbf{S}\left(\mathbf{T}_N^i\right)^{-1}\left(\mathbf{i}^{(dc)} - \mathbf{i}'^{(dc)}\right) \tag{3.16}$$

Further insight can be obtained by inspecting the impedance matrices of the transmission line example that are soon to be operated on. Continuing with our 3 line example ($N = 3$),

$$\mathbf{R} = R\begin{bmatrix}1 & 0 & 0\\ 0 & 1 & 0\\ 0 & 0 & 1\end{bmatrix},\quad \mathbf{L} = L\begin{bmatrix}1 & k_M & k_M\\ k_M & 1 & k_M\\ k_M & k_M & 1\end{bmatrix},\quad \mathbf{S} = \frac{1}{C}\begin{bmatrix}1 & 0 & 0\\ 0 & 1 & 0\\ 0 & 0 & \frac{1}{k}\end{bmatrix} \tag{3.17}$$

From this we see that the line resistances are symmetric, the inductances are balanced but they have a common linkage factor between all lines that can be seen in the upper and lower triangles, and the capacitance is asymmetric. This provides an example of all possible scenarios that may present themselves when working with this methodical approach (other than asymmetric coupling in inductors), and that is why this example is so great at understanding the methodology. Continuing with the example, by looking at Equation 3.16

we have,

$$\text{RHS} = \mathbf{T}_3^v \left(\mathbf{R} + \hat{p}\mathbf{L}\right) \left(\mathbf{T}_3^i\right)^{-1} \mathbf{i}^{(dc)} + \frac{1}{\hat{p}} \mathbf{T}_3^v \mathbf{S} \left(\mathbf{T}_3^i\right)^{-1} \left(\mathbf{i}^{(dc)} - \mathbf{i}'^{(dc)}\right) \tag{3.18}$$

At this point the LHS side of Equation 3.16 is in the form we want and needs no further computation. While the RHS still needs to go through voltage and current transformations before we can extract DM or CM equivalent expressions. With a 3-line example we need to be aware that there are two DM expressions due to the two different pairs of lines ($V_{12}^{(d)}$, $V_{23}^{(d)}$), and one CM expression. In this example we are more interested in the CM expression, but before we start doing the appropriate operations, let us define the transformation matrices that will need to be used to do so. And they are,

$$\mathbf{T}_3^v = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix}, \qquad \left(\mathbf{T}_3^v\right)^{-1} = \begin{bmatrix} \frac{2}{3} & \frac{1}{3} & 1 \\ -\frac{1}{3} & \frac{1}{3} & 1 \\ -\frac{1}{3} & -\frac{2}{3} & 1 \end{bmatrix} \tag{3.19}$$

$$\mathbf{T}_3^i = \begin{bmatrix} \frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{1}{2} & -\frac{1}{2} \\ 1 & 1 & 1 \end{bmatrix}, \qquad \left(\mathbf{T}_3^i\right)^{-1} = \begin{bmatrix} \frac{4}{3} & \frac{2}{3} & \frac{1}{3} \\ -\frac{2}{3} & \frac{2}{3} & \frac{1}{3} \\ -\frac{2}{3} & -\frac{4}{3} & \frac{1}{3} \end{bmatrix} \tag{3.20}$$

With these transformation matrices we are now in the position to start operating on the impedances for the derivation of the CM expression for the transmission line model. Note that I have included the inverse voltage transformation, it will not be used right now but we will see how it will be used in a future operation.

$$\text{RHS} = \mathbf{T}_3^v \mathbf{R} \left(\mathbf{T}_3^i\right)^{-1} \mathbf{i}^{(dc)} + \hat{p}\ \mathbf{T}_3^v \mathbf{L} \left(\mathbf{T}_3^i\right)^{-1} \mathbf{i}^{(dc)} + \frac{1}{\hat{p}} \mathbf{T}_3^v \mathbf{S} \left(\mathbf{T}_3^i\right)^{-1} \left(\mathbf{i}^{(dc)} - \mathbf{i}'^{(dc)}\right) \tag{3.21}$$

The expression is broke into parts so that we can analyze and operate on each impedance separately. These operations can be seen as follows

$$\mathbf{T}_3^v\mathbf{R}\left(\mathbf{T}_3^i\right)^{-1} = R\begin{bmatrix}1 & -1 & 0\\ 0 & 1 & -1\\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3}\end{bmatrix}\begin{bmatrix}1 & 0 & 0\\ 0 & 1 & 0\\ 0 & 0 & 1\end{bmatrix}\begin{bmatrix}\frac{4}{3} & \frac{2}{3} & \frac{1}{3}\\ -\frac{2}{3} & \frac{2}{3} & \frac{1}{3}\\ -\frac{2}{3} & -\frac{4}{3} & \frac{1}{3}\end{bmatrix}$$
$$= R\begin{bmatrix}2 & 0 & 0\\ 0 & 2 & 0\\ 0 & 0 & \frac{1}{3}\end{bmatrix} \tag{3.22}$$
$$\mathbf{T}_3^v\mathbf{L}\left(\mathbf{T}_3^i\right)^{-1} = L\begin{bmatrix}1 & -1 & 0\\ 0 & 1 & -1\\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3}\end{bmatrix}\begin{bmatrix}1 & k_M & k_M\\ k_M & 1 & k_M\\ k_M & k_M & 1\end{bmatrix}\begin{bmatrix}\frac{4}{3} & \frac{2}{3} & \frac{1}{3}\\ -\frac{2}{3} & \frac{2}{3} & \frac{1}{3}\\ -\frac{2}{3} & -\frac{4}{3} & \frac{1}{3}\end{bmatrix}$$
$$= L\begin{bmatrix}2-2k_M & 0 & 0\\ 0 & 2-2k_M & 0\\ 0 & 0 & \frac{2}{3}k_M+\frac{1}{3}\end{bmatrix} \tag{3.23}$$
$$\mathbf{T}_3^v\mathbf{S}\left(\mathbf{T}_3^i\right)^{-1} = \frac{1}{C}\begin{bmatrix}1 & -1 & 0\\ 0 & 1 & -1\\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3}\end{bmatrix}\begin{bmatrix}1 & 0 & 0\\ 0 & 1 & 0\\ 0 & 0 & \frac{1}{k}\end{bmatrix}\begin{bmatrix}\frac{4}{3} & \frac{2}{3} & \frac{1}{3}\\ -\frac{2}{3} & \frac{2}{3} & \frac{1}{3}\\ -\frac{2}{3} & -\frac{4}{3} & \frac{1}{3}\end{bmatrix}$$
$$= \frac{1}{C}\begin{bmatrix}2 & 0 & 0\\ \frac{2}{3}(k-1) & \frac{2}{3}(2k+1) & \frac{1}{3}(1-k)\\ \frac{2}{9}(1-k) & \frac{4}{9}(1-k) & \frac{1}{9}(k+2)\end{bmatrix} \tag{3.24}$$

With these operations now complete we are able to start putting it all together in order to extract the CM expression and eventually construct our CM equivalent model. If we look back at Equation 3.21, instead of using $\left(\mathbf{i}^{(dc)} - \mathbf{i}'^{(dc)}\right)$ as the currents flowing through the capacitors let's rewrite it as $\mathbf{i}''^{(dc)}$, this is more for simplicity's sake to reduce the amount of current terms floating around. Thus, our new expression is

$$\mathbf{V}^{(dc)} + V_{Pg}\left[0\ 0\cdots 1\right]^{\mathrm{T}} = \mathbf{T}_3^v\mathbf{R}\left(\mathbf{T}_3^i\right)^{-1}\mathbf{i}^{(dc)} + \hat{p}\ \mathbf{T}_3^v\mathbf{L}\left(\mathbf{T}_3^i\right)^{-1}\mathbf{i}^{(dc)} + \frac{1}{\hat{p}}\mathbf{T}_3^v\mathbf{S}\left(\mathbf{T}_3^i\right)^{-1}\mathbf{i}''^{(dc)} \tag{3.25}$$

where in matrix representation, we have

$$\begin{bmatrix} V_{12}^{(d)} \\ V_{23}^{(d)} \\ V^{(c)} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ V_{Pg} \end{bmatrix} = R \begin{bmatrix} 2 & 0 & 0 \\ 0 & 2 & 0 \\ 0 & 0 & \frac{1}{3} \end{bmatrix} \begin{bmatrix} i_{12}^{(d)} \\ i_{23}^{(d)} \\ i^{(c)} \end{bmatrix} + \hat{p}L \begin{bmatrix} 2-2k_M & 0 & 0 \\ 0 & 2-2k_M & 0 \\ 0 & 0 & \frac{2}{3}k_M + \frac{1}{3} \end{bmatrix} \begin{bmatrix} i_{12}^{(d)} \\ i_{23}^{(d)} \\ i^{(c)} \end{bmatrix} \cdots$$
$$+ \frac{1}{\hat{p}C} \begin{bmatrix} 2 & 0 & 0 \\ \frac{2}{3}(k-1) & \frac{2}{3}(2k+1) & \frac{1}{3}(1-k) \\ \frac{2}{9}(1-k) & \frac{4}{9}(1-k) & \frac{1}{9}(k+2) \end{bmatrix} \begin{bmatrix} i_{12}^{\prime\prime(d)} \\ i_{23}^{\prime\prime(d)} \\ i^{\prime\prime(c)} \end{bmatrix} \quad (3.26)$$

With the matrix Equation 3.26, we have derived and constructed two DM equations, one that is a representation of line pairs 1 and 2, and the other representing line pairs 2 and 3. A CM equation has also been constructed, in which we are interested in extracting. The extracted CM expression is,

$$V^{(c)} + V_{Pg} = \frac{1}{3}Ri^{(c)} + \hat{p}L\left(\frac{2}{3}k_M + \frac{1}{3}\right)i^{(c)} + \underbrace{\frac{1}{\hat{p}C}\left[\frac{2}{9}(1-k)\left(i_{12}^{\prime\prime(d)} + 2i_{23}^{\prime\prime(d)}\right) + \frac{1}{9}(k+2)\,i^{\prime\prime(c)}\right]}_{V_{c_p}^{(c)}} \quad (3.27)$$

using the following definitions

$$V^{(c)} = \frac{1}{3}\left(V_{1P} + V_{2P} + V_{3P}\right) \quad (3.28)$$

$$i^{(c)} = i_1 + i_2 + i_3,\ i^{\prime(c)} = i_1^{\prime} + i_2^{\prime} + i_3^{\prime},\ i^{\prime\prime(c)} = (i_1 + i_2 + i_3) - \left(i_1^{\prime} + i_2^{\prime} + i_3^{\prime}\right) \quad (3.29)$$

$$i_{12}^{\prime\prime(d)} = \frac{1}{2}\left[(i_1 - i_2) - \left(i_1^{\prime} - i_2^{\prime}\right)\right],\ i_{23}^{\prime\prime(d)} = \frac{1}{2}\left[(i_2 - i_3) - \left(i_2^{\prime} - i_3^{\prime}\right)\right] \quad (3.30)$$

Taking a closer look at Equation 3.27, we see that the first term of the LHS of the equation represents the CM input voltage with reference to our arbitrary point P, and the second term represents the overall voltage potential from our arbitrary point P to the ground. The RHS of the equation represents the various voltage drops from each component of the transmission line. The first term is the voltage drop due to the resistance, the second term is the voltage drop due to the induced flux by the inductance, and the third term highlighted as $V_{c_p}^{(c)}$, which is the voltage drop from the CM parasitic capacitance. In medium or long transmission lines inductance plays a greater role than the resistance, because the current flow in the transmission lines interacts with the surrounding lines. We are aware that when current flows within a conductor, a magnetic flux is present. With a variation of current in

conductors the amount of flux changes and induces an emf in the lines, due to Faraday's Law. This induced emf is present in the inductance parameter. The voltage drop can be seen as a flux linkage within the conductor, namely, the internal flux and the external flux. The internal flux is induced due to the current flowing through the conductor, this is seen as the second term of the inductance voltage drop in Equation 3.27. While the external flux produced around the conductor is due to its own current and the current of other conductors placed around it, and this is seen in the first term of the voltage drop for the inductance including the linkage factor, k_M. The total inductance voltage drop is then determined by the calculation of the internal and external flux. When looking back at our inductance matrix in 3.17, we have a linkage factor k_M which is the same between all three lines, that means we have assumed a symmetrical or equilateral spacing between the conductors of the three-phase line. Which greatly simplifies the voltage drop from the inductance, now we will see what happens when we introduce non-symmetrical distributions of components by looking at the voltage drop from the CM parasitic capacitance. The first term of the CM parasitic capacitance voltage represents a DM-dependent voltage source, which is the DM to CM coupling due to the asymmetric layout of the parasitic capacitance from the transmission line. The second term is the voltage drop which is induced by the CM current flowing through the parasitic capacitance. The only problem is that the DM-dependent voltage source is in terms of the differential currents $i_{12}^{\prime\prime(d)}$ and $i_{23}^{\prime\prime(d)}$ which lack clear analytic descriptions. We cannot accurately predict or synthesis the currents because there are many factors that drive the system currents, and it is often a bit difficult to measure these currents directly if we want to feed the CM model that way. So in order to gain greater insight, we reformulate the dependent voltage sources in terms of parasitic capacitor DM voltages. To begin with we have,

$$\mathbf{C} = C \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & k \end{bmatrix}, \quad \mathbf{V}_{c_p} = \begin{bmatrix} V_{c_p,1} \\ V_{c_p,2} \\ V_{c_p,3} \end{bmatrix} \tag{3.31}$$

which is the capacitance matrix and defined capacitor voltages, receptively. To reformulate the dependent voltage sources we start by looking at the current flowing through the ca-

pacitors, this allows us to gain access to DM voltage sources for the parasitic capacitance. We know that capacitor current is defined as,

$$\mathbf{i}_n = \hat{p}\mathbf{C}\mathbf{V}_{c_p} \tag{3.32}$$

and in matrix representation it is,

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \hat{p}C \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & k \end{bmatrix} \begin{bmatrix} V_{c_p,1} \\ V_{c_p,2} \\ V_{c_p,3} \end{bmatrix} \tag{3.33}$$

Now to achieve MM quantities we apply transformation matrices that we already established in 3.19 and 3.20, thus resulting in

$$\begin{aligned}
\mathbf{T}_3^i \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} &= \hat{p}C\mathbf{T}_3^i \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & k \end{bmatrix} (\mathbf{T}_3^v)^{-1} \begin{bmatrix} V_{c_p,12}^{(d)} \\ V_{c_p,23}^{(d)} \\ V_{c_p}^{(c)} \end{bmatrix} \\
\begin{bmatrix} \frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{1}{2} & -\frac{1}{2} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} &= \hat{p}C \begin{bmatrix} \frac{1}{2} & -\frac{1}{2} & 0 \\ 0 & \frac{1}{2} & -\frac{1}{2} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & k \end{bmatrix} \begin{bmatrix} \frac{2}{3} & \frac{1}{3} & 1 \\ -\frac{1}{3} & \frac{1}{3} & 1 \\ -\frac{1}{3} & -\frac{2}{3} & 1 \end{bmatrix} \begin{bmatrix} V_{c_p,12}^{(d)} \\ V_{c_p,23}^{(d)} \\ V_{c_p}^{(c)} \end{bmatrix} \\
\begin{bmatrix} i_{12}^{(d)} \\ i_{23}^{(d)} \\ i^{(c)} \end{bmatrix} &= \hat{p}C \begin{bmatrix} \frac{1}{2} & 0 & 0 \\ \frac{1}{6}(k-1) & \frac{1}{6}(2k+1) & \frac{1}{2}(1-k) \\ \frac{1}{3}(1-k) & \frac{2}{3}(1-k) & (k+2) \end{bmatrix} \begin{bmatrix} V_{c_p,12}^{(d)} \\ V_{c_p,23}^{(d)} \\ V_{c_p}^{(c)} \end{bmatrix}
\end{aligned} \tag{3.34}$$

Extracting the CM expression for the parasitic capacitance from matrix Equation 3.34

$$i^{(c)} = \hat{p}C \left[\frac{1}{3}(1-k) V_{c_p,12}^{(d)} + \frac{2}{3}(1-k) V_{c_p,23}^{(d)} + (k+2) V_{c_p}^{(c)} \right] \tag{3.35}$$

Then solving this expression for the CM parasitic capacitance voltage, $V_{c_p}^{(c)}$, instead of the CM current

$$V_{c_p}^{(c)} = \frac{1}{\hat{p}C(k+2)} i^{(c)} + \frac{(k-1)}{3(k+2)} V_{c_p,12}^{(d)} + \frac{2(k-1)}{3(k+2)} V_{c_p,23}^{(d)} \tag{3.36}$$

Now the CM voltage of the capacitance is in a form which provides great analytic descrip-

tion, it is in terms of our CM current, $i^{(c)}$, and two dependent DM voltage sources, $V^{(d)}_{c_p,12}$ and $V^{(d)}_{c_p,23}$. The term that includes our CM current is just the voltage drop for the equivalent capacitance of the transmission line, which can be easily understood. When others derive CM models, they usually stop here without introducing the dependent DM voltage sources because they believe the effect they have is negligent or only looking for a close approximation and then dismiss them. But these DM sources gives us a more accurate representation of the CM current paths to ground, and it also provides us with knowledge on the impact of non symmetrical distribution of components in a circuit. The last two terms from the CM expression in Equation 3.36 are these dependent DM voltage sources coupling into the CM system, and are the direct impact of having non symmetrical layout of parasitic capacitance. If we treat the capacitance as symmetrical, by saying $k = 1$, we can see that these voltage sources drop out of the CM expression completely and it is just left with the equivalent capacitance of the model. These two dependent voltage sources are defined as,

$$V^{(d)}_{c_p,12} = V_{c_p,1} - V_{c_p,2} = V_{12}, \qquad V^{(d)}_{c_p,23} = V_{c_p,2} - V_{c_p,3} = V_{23} \tag{3.37}$$

The DM capacitor voltage sources, by definition, is the voltage drop differences between the pair of capacitors. But we must remember that they are parasitic capacitors, which means that they are not physical capacitors within the circuit, so it is physically impossible to measure the voltage across them. If we go back to the transmission line model in Figure 3-1 and create a small KVL loop between the capacitors, the ground, and the nodes that connect them we can simply modify the voltage as the potential across these nodes. The voltage between the nodes is physically possible to measure and provides us with great analytic description for modeling and validating the CM circuits.

There are two specific methods that these dependent DM voltages can be used, one is through a direct measurement in a hardware setup and the other is through a voltage synthesis. If we want to validate a lab setup for some Device-Under-Test (DUT) we can do so by measuring these nodal voltages and plug it directly into our CM equivalent model to validate and understand the CM emissions. Let's now say we don't have a lab setup

for some converter but we want to gain insight on the CM emissions, we can use voltage synthesis as another method that works very well with these analytic descriptions of the CM capacitor voltages. Being that they are voltage sources and we know the system with its control structure, we can accurately synthesize these voltages and plug them into the circuit directly. These are two methods that can be used, and provides reasoning to why DM voltages provide us with greater analytic description that we can't get with DM currents.

Ok, now that we have the CM parasitic capacitor voltages in the form that we want we are now able to take Equation 3.36 and replace it with the previous expression we have in Equation 3.27. Thus, resulting with our CM expression for the transmission line model that looks like,

$$V^{(c)} + V_{Pg} = \frac{1}{3}Ri^{(c)} + \hat{p}L\left(\frac{2}{3}k_M + \frac{1}{3}\right)i^{(c)} + \frac{1}{\hat{p}C\,(k+2)}i''^{(c)} \;\cdots \\ + \frac{(k-1)}{3\,(k+2)}V^{(d)}_{c_p,12} + \frac{2\,(k-1)}{3\,(k+2)}V^{(d)}_{c_p,23} \tag{3.38}$$

This provides us with a full CM derivation that can be used to analyze the high frequency CM behavior for a transmission line model. In the next section we will take this expression and construct a Common-Mode Equivalent (CEM) model that can be implemented in some simulation software for analyzing and validating CM emissions.

3.1.3 Common-Mode Equivalent Circuit Model

Deriving the CM expressions for the model is the difficult and tedious part, but constructing the CEM from the CM expression is very straight forward. To get started, let's first separate the line-to-ground voltage, V_{Pg}, to the LHS of Equation 3.38 and bring the rest of the expression to the RHS.

$$V_{Pg} = -V^{(c)} + \frac{1}{3}Ri^{(c)} + \hat{p}L\left(\frac{2}{3}k_M + \frac{1}{3}\right)i^{(c)} + \frac{1}{\hat{p}C\,(k+2)}i''^{(c)} \;\cdots \\ + \frac{(k-1)}{3\,(k+2)}V^{(d)}_{c_p,12} + \frac{2\,(k-1)}{3\,(k+2)}V^{(d)}_{c_p,23} \tag{3.39}$$

This is the preferred form for constructing the CEM because the LHS is the total voltage potential that connects our arbitrary point P to ground and the the RHS consists of the

voltage drops for each of the equivalent impedances, the CM input voltage source, and two dependent DM voltage sources. Thus, the constructed CEM takes this form,

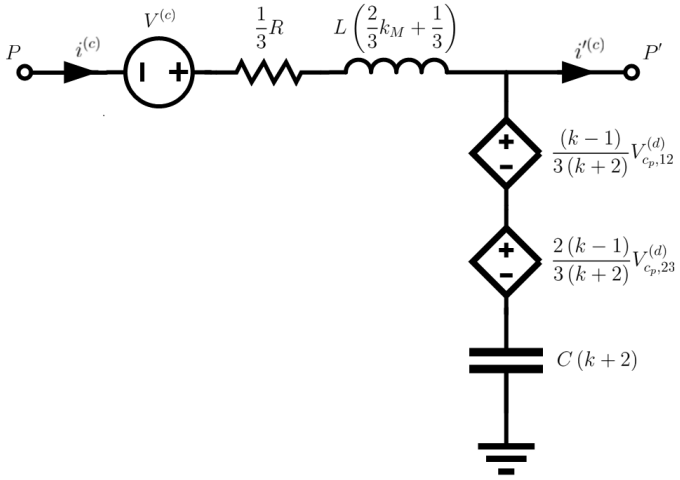


Figure 3-2: Common-Mode Equivalent Model for a 3-Line Transformer Model

Although this is the complete CM equivalent circuit model for our transmission line model there is a few things to note. You will rarely ever just be analyzing this circuit alone, it will be connected to other CM systems like a input power source or some power electronic converter, which is typically the main driver for conducted CM currents. With the goal of connecting this CM circuit up to other CM models for a full system CM model, we have intentionally left our arbitrary P points the way that they are. These P interconnection points gives us freedom of selecting reasonable points within our main circuit, mainly for probable points within a lab setup or for a known synthesized voltage source. If we were to chose a point that is not within our main circuit we might complicate our synthesized voltage or even prohibit us from even being able to probe the circuit for a correct voltage stimulus. It is also important to note that our CM input source is a variable source due to the point P that we chose, this source is the stimulus that initializes our CM circuit to the correct system voltage at that point. If you look at the CM equivalent circuit model, the output arbitrary point is labeled as P' for the freedom of hooking up this CM circuit on the back end to some power electronic converter. A CM output voltage source is not included but there will most definitely be one there, the reason it is left out was that this voltage source did not show up in our derived voltage expression. And in many cases this

voltage source will be translated as a CM input source on the connecting circuit so there is no real reason to show it here. These things will make more sense when we begin to hook up multiple CM stages for a full CM system for testing and validation in the next few chapters.

3.2 Derivation of Voltages for Asymmetric Parasitic Capacitor Models

As we move away from the CM model of a transmission line model, in which we have primarily used for the methodology of understanding the derivation and construction of Common-Mode equivalent models. We will now begin to look at the impact power electronic converters have on CM models, which tend to be the main driver for CM conducted emissions due to there high voltage transition rates (dv/dt) and higher switching frequencies, especially in high power SiC-based systems. These converters usually consist of a single module or multiple modules per leg depending on what converter topology you are using. The SiC power modules consist of two Silicon Carbide semiconductor MOSFETs used as power switches. The SiC power modules allows for higher switching frequencies and can be operated at higher temperatures and higher voltages compared to traditional Si semiconductors. Here is a simplified look at these SiC power modules,

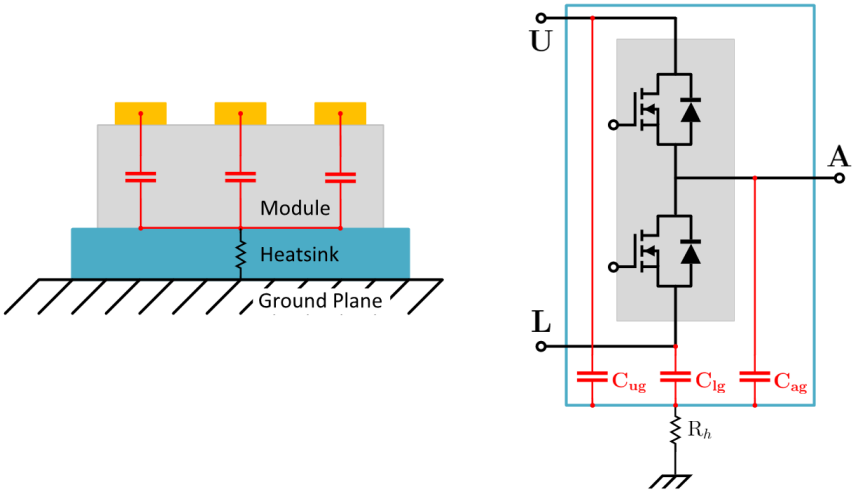


Figure 3-3: SiC Power Module with Parasitic Capacitance

For single module legs, the modules are connected between a dc bus voltage and has a single phase output. One of the most critical parameters in determining the CM currents in many converters is the parasitic capacitance of the power modules. These parasitic capacitances are formed by the modules geometrical configuration from each terminal to the substrate. Due to the higher frequencies these power modules are often operating at higher temperatures, so we set them on heatsinks to dissipate this generated heat. When operating at higher frequencies, these parasitic capacitances allow displacement currents to flow from the substrate into the baseplate of the module that is sitting on the heatsink, which is usually connected to the system ground. Essentially, when a converter switch within the module receives a gate pulse to turn on/off, it can't switch instantaneously, instead it turns on/off with some slew rate. This slew rate or commonly referred to as its switch transition rate (dv/dt) and is the main factor that drives CM displacement current into the heatsink. We know that the current through a capacitor is $i_c = C\,(dv/dt)$, so we begin to see the impact that switch transitions rates have on displacement current. The faster the switching frequency with higher voltages mixed with parasitic capacitance is identified as one of the primary drivers for CM currents in converters, and should be analyzed in great detail. Figure 3-3 illustrates the parasitic capacitance for a SiC power module: C_{ug}, C_{lg}, and C_{ag}. We have defined these capacitances and trapezoidal waveforms as the dominant EMI sources, and for our modeling methodology we measure these parameters in hardware. The rest of the modeling procedure consists of developing a CM model for the power electronics and then importing these dominant EMI sources into our CM equivalent model for predicting conducted emissions.

During the CM equivalent modeling stage for power electronic converters, in which the methodology was discussed in the previous section, we are subject to a wide range of topological structures. When analyzing different converter structures we are usually confronted with single module legs or multiple module legs, but we always assume each module within the converter will have the same substrate design. This allows us to use the same module characterization across the whole converter topology, and it usually doesn't make sense to use a bunch of different modules for the same converter.

The procedure for deriving CM models for power electronic converters can be performed

in six simple steps. Step one, is to break up the circuit and assign super-nodes that are within close proximity and make sense. These are typically seen as input and output nodes, or nodes that are symmetrically distributed throughout the converter. You have to keep in mind that these super-nodes will have an input CM source, so if you spread the super-nodes across the converter this source will be the combination of many switch voltages. So gather super-nodes close in proximity and keep it simple. Step two, calculate the total capacitance seen by each node. The power modules have a parasitic capacitance for every node it is attached to, so simply look at any node within the converter and add all of the capacitance attached to that node. Step three, construct a parasitic capacitance model for each of the super-nodes that have been created within the converter. These parasitic capacitance models illustrate the CM conduction paths through the parasitic capacitors that connect the nodes to the heatsink and then into the ground potential. Step four, derive a CM expression using the mathematical modeling procedure explained in the previous section for each of the parasitic capacitor models created. Step five, construct a CM equivalent model for each of the CM expressions. Step six, connect all of the CM equivalent models together at some common point, which will typically be the arbitrary P point, for a full converter CM equivalent model.

The CM modeling procedure seems very simple, and it is but the process is very tedious and there is a lot of room for error, especially if you are doing the math by hand. From experience, most of the mathematical errors happened with complex converters and to save time and headaches you should try to avoid these as much as possible. I want to briefly explain a few errors I made when deriving CM models for power electronic converters. Firstly, keep your capacitance matrix as simple as possible because this matrix will be going through multiple transformations and the more complex you make it, you will tend to make sign errors or end up with very complex looking expressions. Secondly, the expressions you get are not unique, there are multiple solutions to this procedure based on the order in which you lay out the nodes and their corresponding capacitance. There is an independent solution based on the arrangement of nodes you chose and it is very easy to rearrange nodes and come up with a completely different expression. If you are trying to replicate my work but come up with a different CM expression, look back at how you arranged your nodes and

that may be why. It doesn't mean you are wrong though, because as stated earlier there are multiple solutions for a CM expression that will model the system in the same way, just keep that in mind. The best way for the arrangement of nodes should be determined prior based on the direction you want to probe the voltages.

Over time I wised up and began using a MATLAB script, with use of the symbolic math toolbox, to help myself derive these CM expressions to avoid simple mathematical errors and save myself an incredible amount of time. A generic procedure that developed a generic CM expression can be used for almost every parasitic capacitor model. When gathering super-nodes and constructing parasitic capacitor models, I was almost always confronted with two different capacitor models, and they are the 2- and 3-line capacitor models. Figure 3-4 shows a generic setup for parasitic capacitor models with two or three nodes. With all of the modeling I have done, I have yet to extend this to a 4-line capacitor model, but it doesn't mean that it isn't possible. This generic procedure will be used so that we can reference them in the future when deriving CM models for power electronic converters, instead of rederiving the CM capacitor voltages each time. So, let us derive it once and then take these generic expressions and plug in values, which then will be used in the total CM expression for the converters.

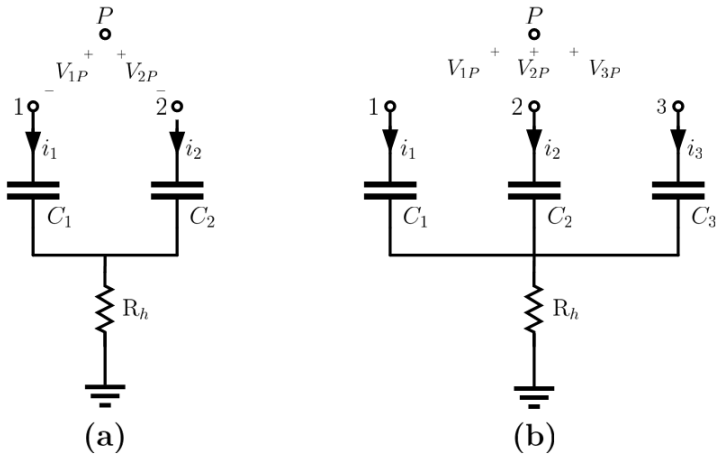


Figure 3-4: (a) 2-Line, (b) 3-Line Parasitic Capacitor Models

These parasitic capacitance models can be modified in a few different ways. Even though there will always be a heatsink resistance, unless for some reason you don't use a heatsink,

there might be some insulation that separates the heatsink from the chassis. This would then be modeled by some capacitance in series with the resistance, to make these changes simply model the resistance as some impedance Z_h instead. All of the CM current flows through this series path so the procedure will still remain the same and you will not see any DM coupling in this path.

2-line equations

Applying KVL to the two line capacitor model in Figure 3-4(a)

$$V_{Pg} = -V_{1P} + \frac{1}{\hat{p}C_1} i_1 + R_h \left(i_1 + i_2\right) \tag{3.40}$$

$$V_{Pg} = -V_{2P} + \frac{1}{\hat{p}C_2} i_2 + R_h \left(i_1 + i_2\right) \tag{3.41}$$

In matrix form

$$\begin{bmatrix} V_{Pg} \\ V_{Pg} \end{bmatrix} = - \begin{bmatrix} V_{1P} \\ V_{2P} \end{bmatrix} + \frac{1}{\hat{p}} \begin{bmatrix} \frac{1}{C_1} & 0 \\ 0 & \frac{1}{C_2} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} + \begin{bmatrix} R_h & R_h \\ R_h & R_h \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{3.42}$$

Applying transformation matrices

$$\begin{aligned} \mathbf{T}_2^v \begin{bmatrix} V_{Pg} \\ V_{Pg} \end{bmatrix} &= - \mathbf{T}_2^v \begin{bmatrix} V_{1P} \\ V_{2P} \end{bmatrix} + \frac{1}{\hat{p}} \mathbf{T}_2^v \begin{bmatrix} \frac{1}{C_1} & 0 \\ 0 & \frac{1}{C_2} \end{bmatrix} \left(\mathbf{T}_2^i\right)^{-1} \begin{bmatrix} i_{12}^{(d)} \\ i^{(c)} \end{bmatrix} + \mathbf{T}_2^v \begin{bmatrix} R_h & R_h \\ R_h & R_h \end{bmatrix} \left(\mathbf{T}_2^i\right)^{-1} \begin{bmatrix} i_{12}^{(d)} \\ i^{(c)} \end{bmatrix} \\ \begin{bmatrix} 0 \\ V_{Pg} \end{bmatrix} &= - \begin{bmatrix} V_{12,P}^{(d)} \\ V^{(c)} \end{bmatrix} + \underbrace{\frac{1}{\hat{p}} \begin{bmatrix} \frac{1}{C_1+C_2} & \frac{1}{2(C_1-C_2)} \\ \frac{1}{2(C_1-C_2)} & \frac{1}{4(C_1+C_2)} \end{bmatrix} \begin{bmatrix} i_{12}^{(d)} \\ i^{(c)} \end{bmatrix}}_{V_{cp}^{(c)}} + \begin{bmatrix} 0 & 0 \\ 0 & R_h \end{bmatrix} \begin{bmatrix} i_{12}^{(d)} \\ i^{(c)} \end{bmatrix} \end{aligned} \tag{3.43}$$

We don't want our CM capacitor voltages to be in terms of DM currents. So to get the capacitor voltages in the form we want, we must rearrange the equations in a different manner which will allow for differential voltages. The rearrangement looks like this

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \hat{p} \begin{bmatrix} C_1 & 0 \\ 0 & C_2 \end{bmatrix} \begin{bmatrix} V_{c_p,1} \\ V_{c_p,2} \end{bmatrix}$$

Applying transformation matrices

$$\mathbf{T}_2^i \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \hat{p}\ \mathbf{T}_2^i \begin{bmatrix} C_1 & 0 \\ 0 & C_2 \end{bmatrix} (\mathbf{T}_2^v)^{-1} \begin{bmatrix} V_{c_p,1} \\ V_{c_p,2} \end{bmatrix}$$
$$\begin{bmatrix} i_{12}^{(d)} \\ i^{(c)} \end{bmatrix} = \hat{p} \begin{bmatrix} \frac{1}{4}(C_1+C_2) & \frac{1}{2}(C_1-C_2) \\ \frac{1}{2}(C_1-C_2) & (C_1+C_2) \end{bmatrix} \begin{bmatrix} V_{c_p,12}^{(d)} \\ V_{c_p}^{(c)} \end{bmatrix}$$

Extracting the CM voltage equation for the capacitors in the form that we want (1 DM capacitor voltages and 1 CM current). This gives us

$$V_{c_p}^{(c)} = \frac{i^{(c)}}{\hat{p}(C_1+C_2)} + \frac{C_2-C_1}{2(C_1+C_2)} V_{c_p,12}^{(d)} \tag{3.44}$$

Resulting in a CM equation for a KVL of a 2 line capacitor model.

$$V_{Pg} = -V^{(c)} + \frac{C_2-C_1}{2(C_1+C_2)} V_{c_p,12}^{(d)} + \frac{i^{(c)}}{\hat{p}(C_1+C_2)} + R_h i^{(c)} \tag{3.45}$$

3-line equations

Applying KVL to the 3 line capacitor model in Figure 3-4(b)

$$V_{Pg} = -V_{1P} + \frac{1}{\hat{p}C_1} i_1 + R_h(i_1+i_2+i_3) \tag{3.46}$$
$$V_{Pg} = -V_{2P} + \frac{1}{\hat{p}C_2} i_2 + R_h(i_1+i_2+i_3) \tag{3.47}$$
$$V_{Pg} = -V_{3P} + \frac{1}{\hat{p}C_3} i_3 + R_h(i_1+i_2+i_3) \tag{3.48}$$

In matrix form

$$\begin{bmatrix} V_{Pg} \\ V_{Pg} \\ V_{Pg} \end{bmatrix} = -\begin{bmatrix} V_{1P} \\ V_{2P} \\ V_{3P} \end{bmatrix} + \frac{1}{\hat{p}} \begin{bmatrix} \frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 \\ 0 & 0 & \frac{1}{C_3} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} + \begin{bmatrix} R_h & R_h & R_h \\ R_h & R_h & R_h \\ R_h & R_h & R_h \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{3.49}$$

Applying transformation matrices

$$\mathbf{T}_3^v \begin{bmatrix} V_{Pg} \\ V_{Pg} \\ V_{Pg} \end{bmatrix} = - \mathbf{T}_3^v \begin{bmatrix} V_{1P} \\ V_{2P} \\ V_{3P} \end{bmatrix} + \frac{1}{\hat{p}} \mathbf{T}_3^v \begin{bmatrix} \frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 \\ 0 & 0 & \frac{1}{C_3} \end{bmatrix} \left(\mathbf{T}_3^i\right)^{-1} \begin{bmatrix} i_{12}^{(d)} \\ i_{23}^{(d)} \\ i^{(c)} \end{bmatrix} \cdots$$
$$+ \mathbf{T}_3^v \begin{bmatrix} R_h & R_h & R_h \\ R_h & R_h & R_h \\ R_h & R_h & R_h \end{bmatrix} \left(\mathbf{T}_3^i\right)^{-1} \begin{bmatrix} i_{12}^{(d)} \\ i_{23}^{(d)} \\ i^{(c)} \end{bmatrix}$$

After transformation

$$\begin{bmatrix} 0 \\ 0 \\ V_{Pg} \end{bmatrix} = - \begin{bmatrix} V_{12,p}^{(d)} \\ V_{23,p}^{(d)} \\ V^{(c)} \end{bmatrix} \cdots$$
$$+ \frac{1}{\hat{p}} \begin{bmatrix} \frac{2}{3}\left(\frac{2}{C_1} + \frac{1}{C_2}\right) & \frac{2}{3}\left(\frac{1}{C_1} - \frac{1}{C_2}\right) & \frac{1}{3}\left(\frac{1}{C_1} - \frac{1}{C_2}\right) \\ \frac{2}{3}\left(\frac{1}{C_3} - \frac{1}{C_2}\right) & \frac{2}{3}\left(\frac{1}{C_2} + \frac{2}{C_3}\right) & \frac{1}{3}\left(\frac{1}{C_2} - \frac{1}{C_3}\right) \\ \frac{2}{9}\left(\frac{2}{C_1} - \frac{1}{C_2} - \frac{1}{C_3}\right) & \frac{2}{9}\left(\frac{1}{C_1} + \frac{1}{C_2} - \frac{2}{C_3}\right) & \frac{1}{9}\left(\frac{1}{C1} + \frac{1}{C_2} + \frac{1}{C_3}\right) \end{bmatrix} \begin{bmatrix} i_{12}^{(d)} \\ i_{23}^{(d)} \\ i^{(c)} \end{bmatrix} \cdots$$
$$+ \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & R_h \end{bmatrix} \begin{bmatrix} i_{12}^{(d)} \\ i_{23}^{(d)} \\ i^{(c)} \end{bmatrix} \quad (3.50)$$

Rearranging the capacitor voltage equations to avoid having DM currents

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \hat{p} \begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & C_3 \end{bmatrix} \begin{bmatrix} V_{c_p,1} \\ V_{c_p,2} \\ V_{c_p,3} \end{bmatrix}$$

Applying transformation matrices

$$\mathbf{T}_3^i \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \hat{p}\ \mathbf{T}_3^i \begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & C_3 \end{bmatrix} \left(\mathbf{T}_3^v\right)^{-1} \begin{bmatrix} V_{c_p,1} \\ V_{c_p,2} \\ V_{c_p,3} \end{bmatrix}$$
$$\begin{bmatrix} i_{12}^{(d)} \\ i_{23}^{(d)} \\ i^{(c)} \end{bmatrix} = \hat{p} \begin{bmatrix} \frac{1}{6}\left(2C_1 + C_2\right) & \frac{1}{6}\left(C_1 - C_2\right) & \frac{1}{2}\left(C_1 - C_2\right) \\ \frac{1}{6}\left(C_3 - C_2\right) & \frac{1}{6}\left(C_2 + 2C_3\right) & \frac{1}{2}\left(C_2 - C_3\right) \\ \frac{1}{3}\left(2C_1 - C_2 - C_3\right) & \frac{1}{3}\left(C_1 + C_2 - 2C_3\right) & \left(C_1 + C_2 + C_3\right) \end{bmatrix} \begin{bmatrix} V_{c_p,12}^{(d)} \\ V_{c_p,23}^{(d)} \\ V_{c_p}^{(c)} \end{bmatrix}$$

Extracting the CM voltage equation for the capacitors in the form that we want (in terms of 2 DM capacitor voltages and 1 CM current). This gives us

$$V_{c_p}^{(c)} = \frac{i^{(c)}}{\hat{p}\,(C_1+C_2+C_3)} + \frac{C_2+C_3-2C_1}{3\,(C_1+C_2+C_3)}V_{c_p,12}^{(d)} + \frac{2C_3-C_1-C_2}{3\,(C_1+C_2+C_3)}V_{c_p,23}^{(d)} \tag{3.51}$$

Resulting in a CM equation for a KVL of a 3 line capacitor model.

$$V_{Pg} = -V^{(c)} + \frac{C_2+C_3-2C_1}{3\,(C_1+C_2+C_3)}V_{c_p,12}^{(d)} + \frac{2C_3-C_1-C_2}{3\,(C_1+C_2+C_3)}V_{c_p,23}^{(d)} + \frac{i^{(c)}}{\hat{p}\,(C_1+C_2+C_3)} + R_h i^{(c)} \tag{3.52}$$

3.3 Full-Bridge CM Modeling

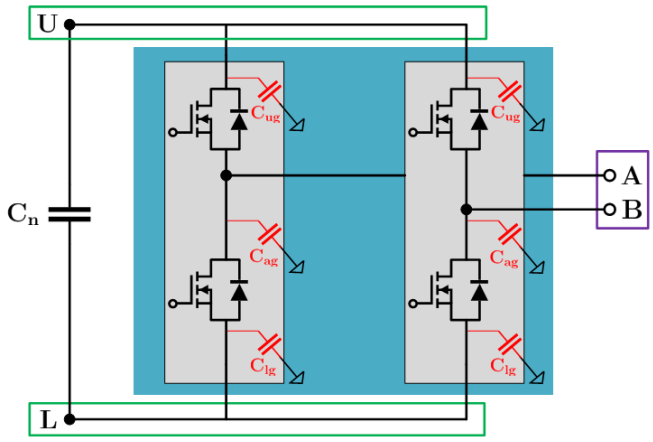


Figure 3-5: Full-Bridge Circuit with Parasitic Capacitance

Figure 3-5 illustrates a Full-Bridge circuit using two SiC power modules that are placed on top of a heat sink, with a top-down view. The converter has input nodes (U,L) with a dc-link capacitor between them, and has output phase nodes (A,B). The full-bridge converter can be separated into two sections; a DC side with the input nodes, and an AC side with the output nodes. Using this analysis we can begin to derive CM expressions for both sides which will result in a Common-mode equivalent model for the converter.

3.3.1 Derivation of the DC-side CM expression

Considering only the DC-side of Figure 3-5, we note that the circuit simply consists of the parallel combinations of the two parasitic capacitances, C_{ug}, w.r.t. the positive rail (U)

and the two parasitic capacitances, C_{lg}, w.r.t. the negative rail (L). Thus, resulting in the parasitic capacitance model below

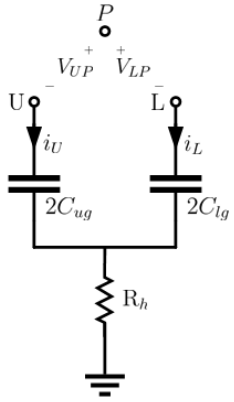


Figure 3-6: Full-Bridge, DC Parasitic Capacitance Model

Now we use Equation 3.45, which is our previously derived expression for a 2-line capacitor model, and then plug in values from the capacitance model in Figure 3-6. This results in a CM expression for the DC side of the full-bridge, shown below

$$V_{Pg} = -V_{UL}^{(c)} + \frac{C_{lg} - C_{ug}}{2\left(C_{lg} + C_{ug}\right)} V_{c_p,UL}^{(d)} + \frac{i^{(c)}}{\hat{p}\left(C_{lg} + C_{ug}\right)} + R_h i^{(c)} \tag{3.53}$$

Then extending this CM expression into an equivalent circuit model,

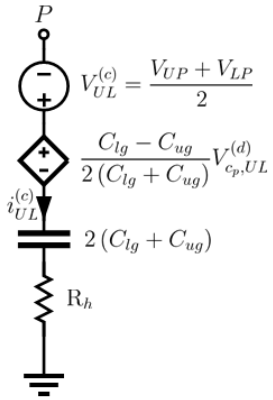


Figure 3-7: Full-Bridge, DC Side CEM

3.3.2 Derivation of the AC-side CM expression

Considering the AC-side of Figure 3-5, we see that the circuit simply consists of one parasitic capacitance, C_{ag}, w.r.t. phase A and one parasitic capacitance, C_{ag}, w.r.t. phase B. This means that the AC-side has a symmetric distribution of parasitic capacitance, significantly simplifying the CM expression. The parasitic capacitance model of the AC-side can be seen below

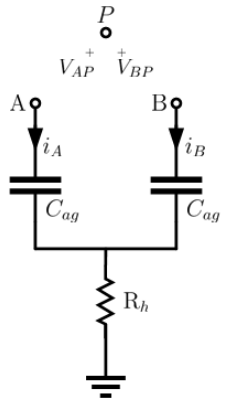


Figure 3-8: Full-Bridge, AC Parasitic Capacitance Model

Relating Equation 3.45 to the parasitic capacitance model in Figure 3-8 results in a CM expression for the AC-side of the full-bridge, shown below

$$V_{Pg} = -V_{AB}^{(c)} + \frac{i^{(c)}}{\hat{p}\,(2C_{ag})} + R_h i^{(c)} \tag{3.54}$$

Due to the symmetric distribution of parasitic capacitance we see that there is not a DM coupling term into the CM expression. The CEM is shown below

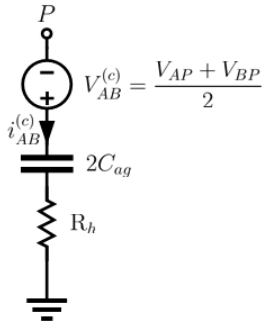


Figure 3-9: Full-Bridge, AC Side CEM

3.3.3 Full-Bridge Common-Mode Equivalent Circuit

In order to obtain the common-mode equivalent circuit for the full-bridge system, we simply combine the DC and AC side equivalent circuits at the common-mode reference point chosen. Thus, combining the two models at the point P, we have the following CEM

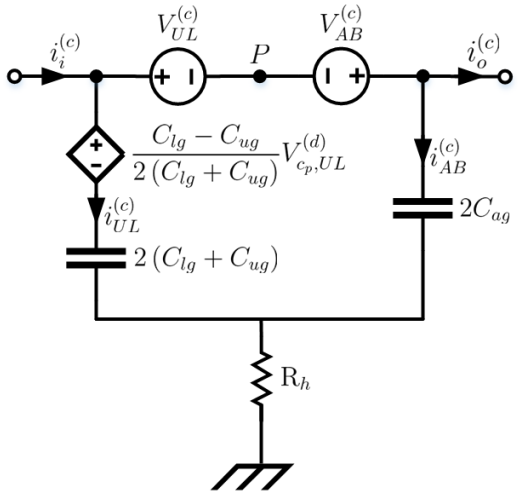


Figure 3-10: Full-Bridge Common-Mode Equivalent Model

3.4 Three Phase Inverter CM Modeling

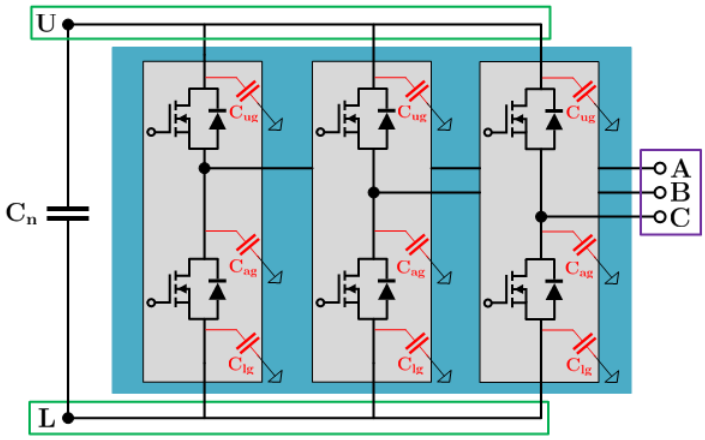


Figure 3-11: 3-Phase Inverter Circuit with Parasitic Capacitance

The 3-Phase Inverter can be separated into two sections; a DC side with input nodes (U,L), and an AC side with output nodes (A,B,C). Using this analysis we will derive CM expressions for both sides.

3.4.1 Derivation of the DC-side CM expression

Considering only the DC-side of Figure 3-11, we note that the circuit simply consists of the parallel combinations of the three parasitic capacitances, C_{ug}, w.r.t. the positive rail (U) and the three parasitic capacitances, C_{lg}, w.r.t. the negative rail (L). Thus, resulting in the parasitic capacitance model below

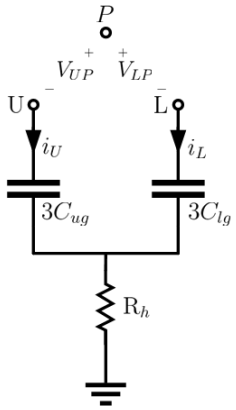


Figure 3-12: 3-Phase Inverter, DC Parasitic Capacitance Model

Relating Equation 3.45 to the parasitic capacitance model in Figure 3-12 results in a CM expression for the DC-side of the 3-Phase Inverter, shown below

$$V_{Pg} = -V_{UL}^{(c)} + \frac{C_{lg} - C_{ug}}{2\left(C_{lg} + C_{ug}\right)} V_{c_p,UL}^{(d)} + \frac{i^{(c)}}{\hat{p}\ 3\left(C_{lg} + C_{ug}\right)} + R_h i^{(c)} \tag{3.55}$$

Then extending this CM expression into an equivalent circuit model,

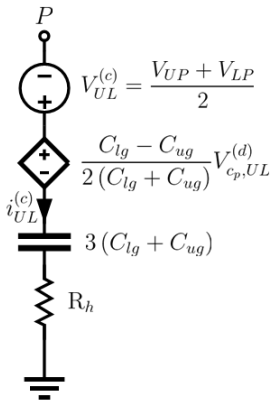


Figure 3-13: 3-Phase Inverter, DC Side CEM

3.4.2 Derivation of the AC-side CM expression

Considering the AC-side of Figure 3-11, we see that the circuit simply consists of a symmetric distribution of capacitance. There is one parasitic capacitance, C_{ag}, w.r.t. phase A, one parasitic capacitance, C_{ag}, w.r.t. phase B, and one parasitic capacitance, C_{ag}, w.r.t. phase C. The parasitic capacitance model of the AC-side can be seen below

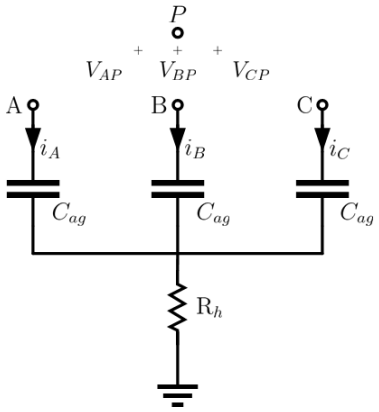


Figure 3-14: 3-Phase Inverter, AC Parasitic Capacitance Model

Relating Equation 3.52 to the parasitic capacitance model in Figure 3-14 results in a CM expression for the AC-side of the inverter, shown below

$$V_{Pg} = -V_{ABC}^{(c)} + \frac{i^{(c)}}{\hat{p}\,(3C_{ag})} + R_h i^{(c)} \tag{3.56}$$

Based on the symmetrical distribution of parastic capacitance on the AC terminals, the DM coupling term has been eliminated. The CEM is shown below

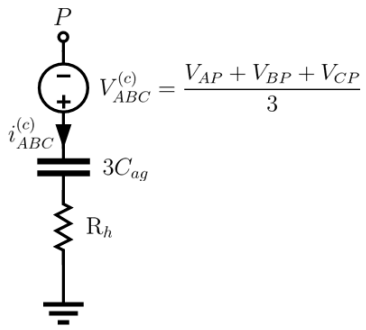


Figure 3-15: 3-Phase Inverter, AC Side CEM

3.4.3 3-Phase Inverter Common-Mode Equivalent Circuit

To obtain the common-mode equivalent circuit for the inverter system, we simply combine the DC and AC side equivalent circuits at the common-mode reference point P. Thus, the CEM for the entire 3-phase inverter is

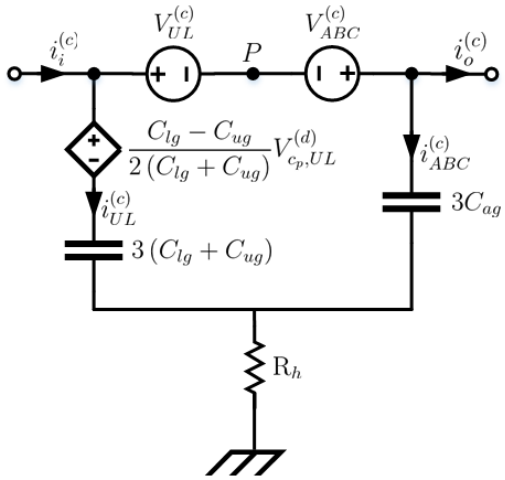


Figure 3-16: 3-Phase Inverter Common-Mode Equivalent Model

3.5 Neutral Point Clamped Full-Bridge CM Modeling

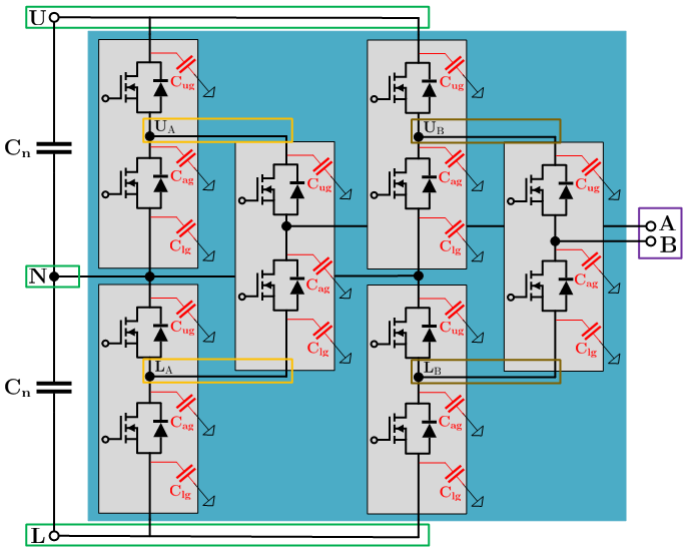


Figure 3-17: NPC Full-Bridge Circuit with Parasitic Capacitance

The derivation of the Neutral Point Clamped (NPC) Full-Bridge converter follows the same

basic procedure that is followed in the previous CM derivations, but due to the complexity of this converter it takes a little more work and a different look at nodes. When looking at Figure 3-17 we break the circuit up and assign super-nodes that are close in proximity and make sense, these super-nodes are represented with corresponding colors. Labeled in green is super-node (U,L,N), labeled in yellow is the super-node (U_A,L_A), labeled in brown is super-node (U_B,L_B), and labeled in purple is the super-node (A,B), which is also our output node. At this point we will analyze each super-node independently by constructing a parasitic capacitance model and then determine a CM expression and equivalent circuit for each.

3.5.1 Derivation of Super-Node (U,L,N) CM expression

From Figure 3-17 we can calculate the total capacitance seen by each node. These nodal capacitances are,

$$\text{Node U}: \; C = 2C_{ug}, \quad \text{Node L}: \; C = 2C_{lg}, \quad \text{Node N}: \; C = 2C_{ug} + 2C_{lg}$$

Then constructing a parasitic capacitor model based on these nodal capacitances

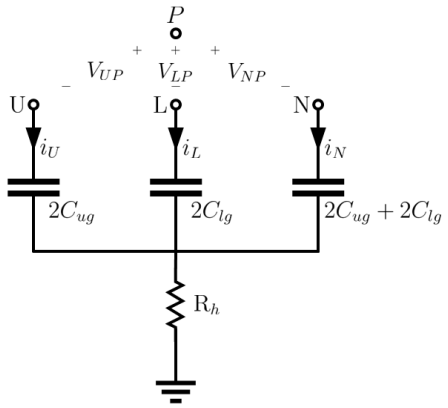


Figure 3-18: NPC Full-Bridge, Super-Node (U,L,N) Capacitance Model

Using Equation 3.52 to come up with a CM expression for this capacitance model

$$V_{Pg} = -V_{ULN}^{(c)} + \frac{2C_{lg} - C_{ug}}{6\,(C_{lg} + C_{ug})} V_{c_p,UL}^{(d)} + \frac{1}{6} V_{c_p,LN}^{(d)} + \frac{i^{(c)}}{\hat{p}\;4\,(C_{lg} + C_{ug})} + R_h i^{(c)} \tag{3.57}$$

The CEM for this CM expression is shown below

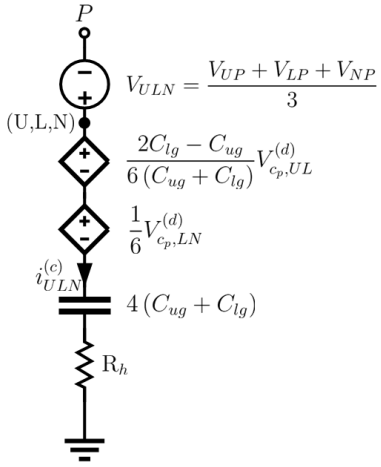


Figure 3-19: NPC Full-Bridge, Super-Node (U,L,N) CEM

3.5.2 Derivation of Super-Nodes (U_A,L_A) and (U_B,L_B) CM expressions

From Figure 3-17 we can calculate the total capacitance seen by each node

$$\text{Node U}_\text{A}: \; C = C_{ag} + C_{ug}, \quad \text{Node L}_\text{A}: \; C = C_{ag} + C_{lg}$$

$$\text{Node U}_\text{B}: \; C = C_{ag} + C_{ug}, \quad \text{Node L}_\text{B}: \; C = C_{ag} + C_{lg}$$

This results in two constructed parasitic models for each super-node

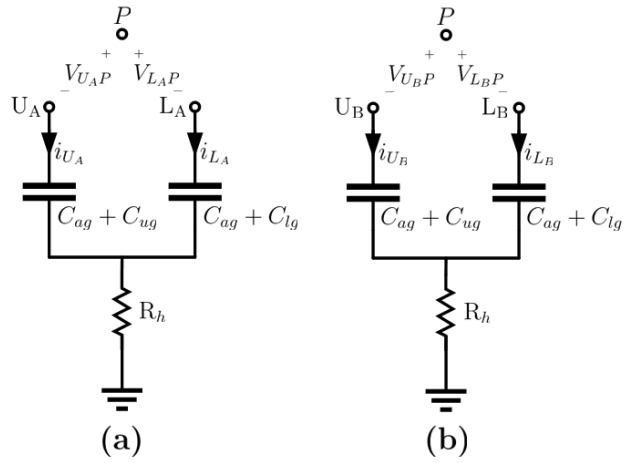


Figure 3-20: NPC Full-Bridge: (a) Super-Node (U_A,L_A) Capacitance Model, (b) Super-Node (U_B,L_B) Capacitance Model

Using the super-node (U_A,L_A) capacitance model and Equation 3.45, the resulting super-node CM expression is

$$V_{Pg} = -V^{(c)}_{U_A L_A} + \frac{C_{lg} - C_{ug}}{2\left(C_{lg} + C_{ug} + 2C_{ag}\right)} V^{(d)}_{c_p, U_A L_A} + \frac{i^{(c)}}{\hat{p}\left(C_{lg} + C_{ug} + 2C_{ag}\right)} + R_h i^{(c)} \quad (3.58)$$

and the CM expression for super-node (U_B,L_B) is

$$V_{Pg} = -V^{(c)}_{U_B L_B} + \frac{C_{lg} - C_{ug}}{2\left(C_{lg} + C_{ug} + 2C_{ag}\right)} V^{(d)}_{c_p, U_B L_B} + \frac{i^{(c)}}{\hat{p}\left(C_{lg} + C_{ug} + 2C_{ag}\right)} + R_h i^{(c)} \quad (3.59)$$

Looking at Equations 3.58 and 3.59 we see how similar they truly are, the constants remain the same between the two while the CM/DM voltages and the CM current are different. Constructing a CEM for both expressions below

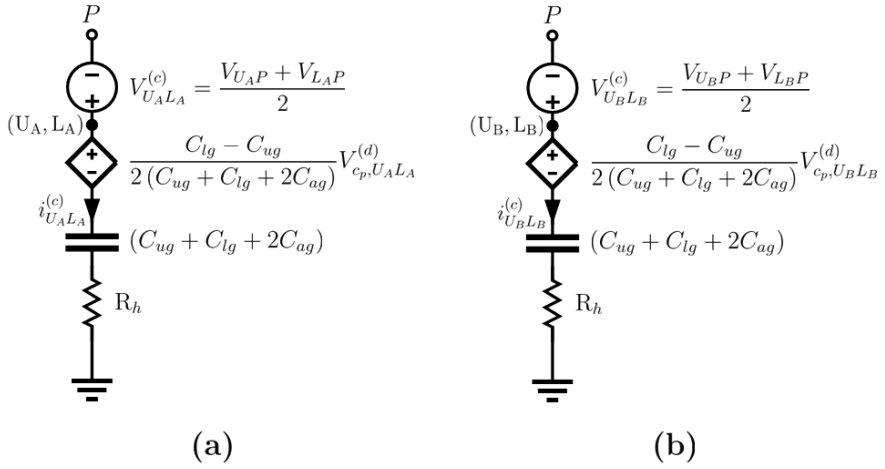


Figure 3-21: NPC Full-Bridge: (a) Super-Node (U_A,L_A) Capacitance Model, (b) Super-Node (U_B,L_B) CEM

3.5.3 Derivation of Super-Node (A,B) CM expression

From Figure 3-17 the total capacitance seen by each node is

$$\text{Node A}: \; C = C_{ag}, \quad \text{Node B}: \; C = C_{ag}$$

The constructed parasitic capacitance model is as follows

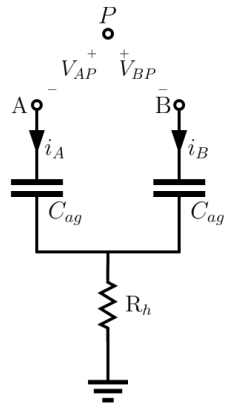


Figure 3-22: NPC Full-Bridge, Super-Node (AB) Capacitance Model

Once again we are confronted with a symmetrical distribution of capacitance seen at the AC terminals, which tends to be a common occurrence when analyzing the phase outputs because of where they are connected to power modules. Using Equation 3.45 and plugging in values from our capacitance model above, we result in the CM expression below

$$V_{Pg} = -V_{AB}^{(c)} + \frac{i^{(c)}}{\hat{p}\,(2C_{ag})} + R_h i^{(c)} \tag{3.60}$$

The CEM resulting from this CM expression is as follows

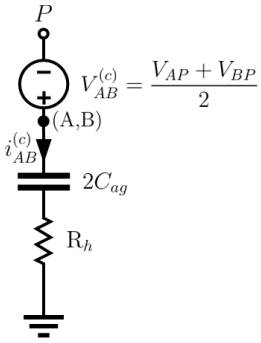


Figure 3-23: NPC Full-Bridge, Super-Node (A,B) CEM

Conveniently our super-node (A,B) is also our output node of the circuit, so we are able to tap into this node within the CEM for connecting this model to external CM circuits. But we can't say the same about our input node (U,L), so there is one more step that needs to be taken before we complete a full CEM for the NPC full-bridge converter.

3.5.4 Derivation of Input Node (U,L) CM expression

When looking back at the CEM we constructed for the super-node (U,L,N) in Figure 3-19 we see that there is not a convenient place for us to tap into the input node (U,L). We have a super-node (U,L,N) not a super-node (U,L), so we need to construct a CEM for the input node that only consists of a CM input voltage and nothing else so there is a way for us to connect the full CM circuit to some input source or front end converter. We can do this because the parasitic capacitance has already been included in our analysis of the super-node (U,L,N) and would lead to errors if we included them again for our input node. Therefore, we can simply look at this input node in this manner below

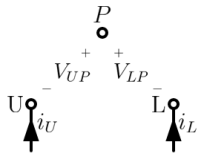


Figure 3-24: NPC Full-Bridge, Input Node (U,L)

From this figure it is a fairly trivial method in deriving a CEM for the input node of the converter. Essentially it is just a CM voltage term that relates the two input notes to the arbitrary reference point P. The CM equivalent circuit for the input node is as follows

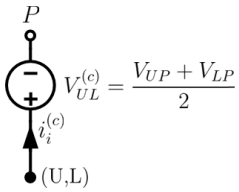


Figure 3-25: NPC Full-Bridge, Input Node (U,L) CEM

With this CEM we now have access to the input node of the converter.

3.5.5 NPC Full-Bridge Common-Mode Equivalent Circuit

To obtain the CEM for the NPC Full-Bridge system, we simply combine all super-node and input node equivalent circuits at the common-mode reference point P.

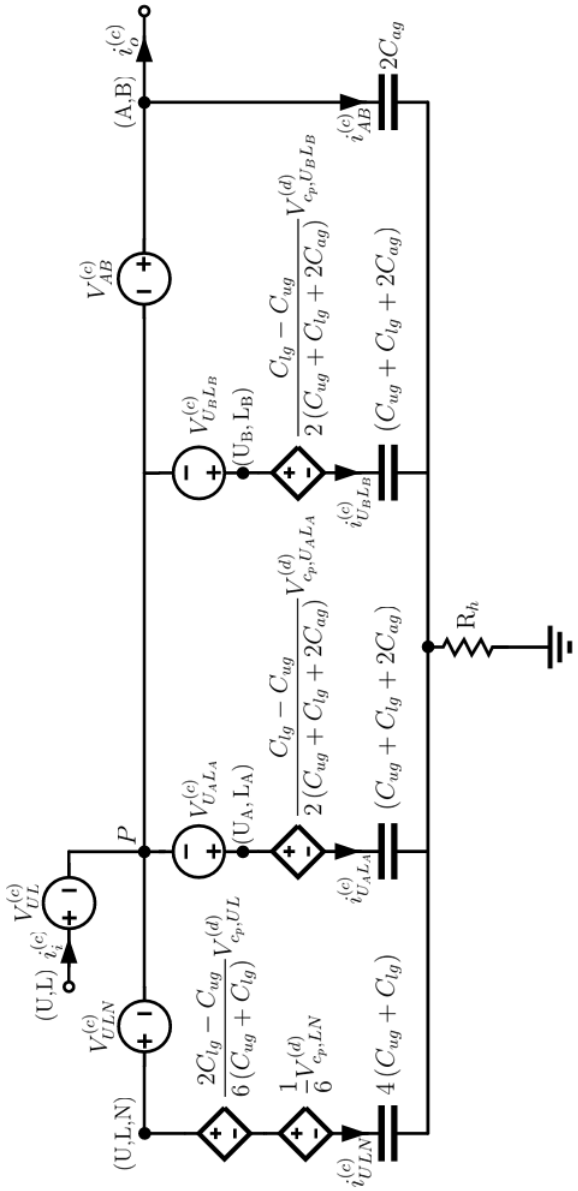


Figure 3-26: NPC Full-Bridge Common-Mode Equivalent Model

3.6 3-Phase Neutral Point Clamped Inverter CM Modeling

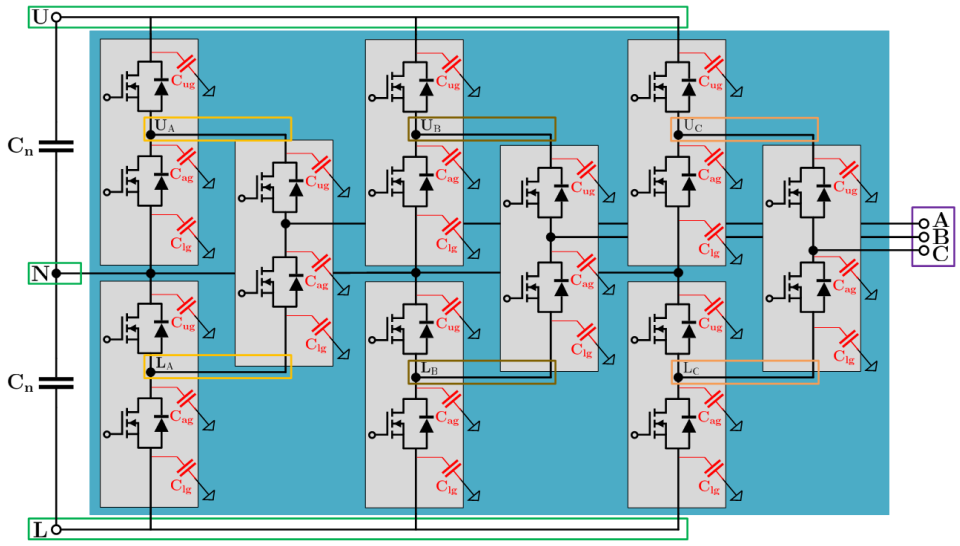


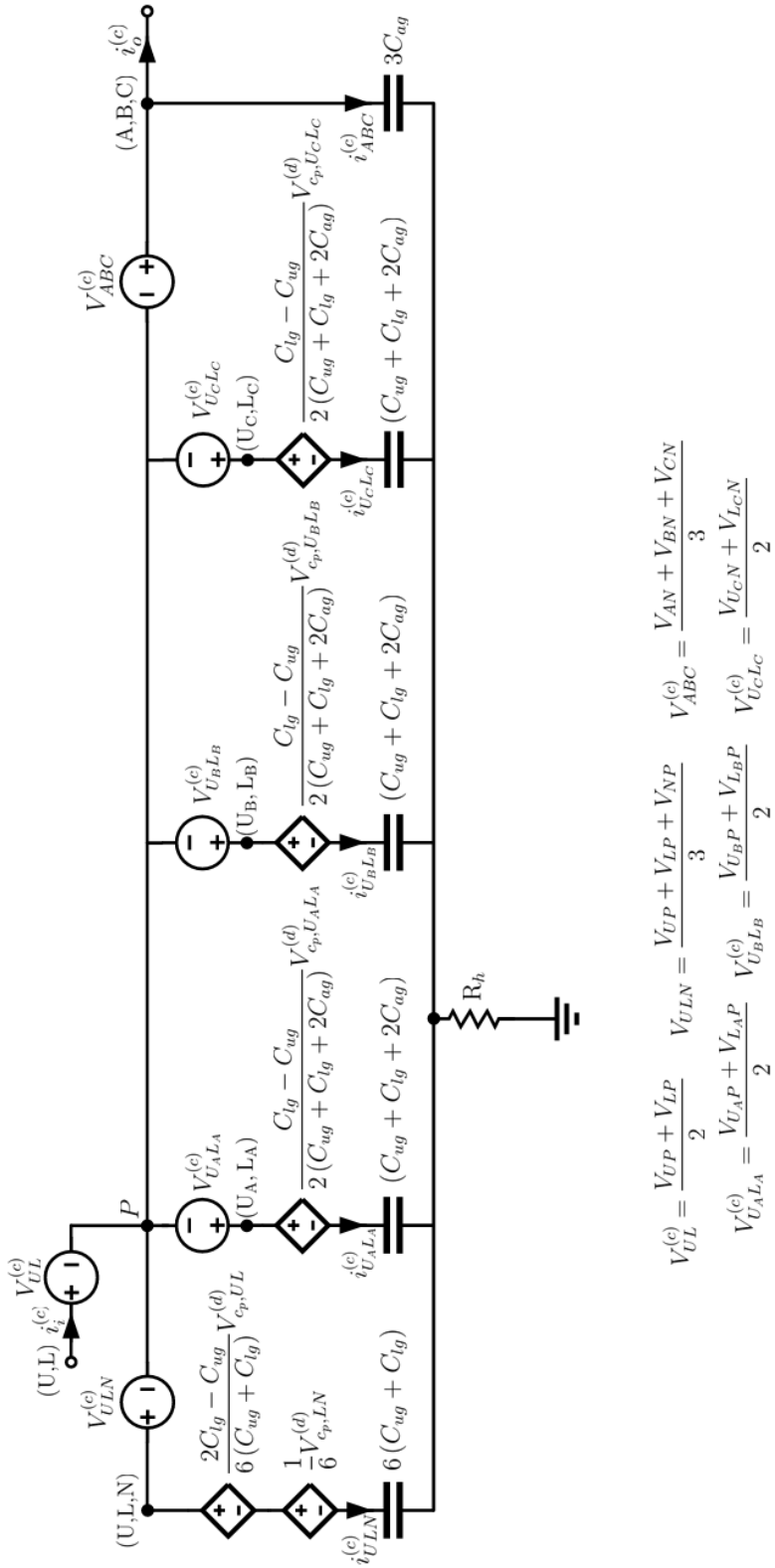
Figure 3-27: NPC Inverter Circuit with Parasitic Capacitance

The derivation of the Neutral Point Clamped Inverter is just an extension from the previous derivation of the NPC Full-Bridge. We have added one more converter leg to allow for a 3-phase AC to DC converter. We still keep most of the same super-nodes; where we have super-node (U,L,N) labeled in green, super-node (U_A,L_A) labeled in yellow, and super-node (U_B,L_B) labeled in brown. But with the addition of the third leg we now have a super-node (U_C,L_C) labeled in orange and a super-node (A,B,C) labeled in purple. We still follow the same procedure as before, where we analyze each super-node independently by constructing a parasitic capacitance model and then determine a CM expression and equivalent circuit for each, then piece them all together for a full system CEM. To avoid repeated work, I will calculate the total capacitance seen by each node and then supply you with the final common-mode equivalent model for the system.

$$\text{Nodes A, B, C}: \; C = C_{ag}$$

$$\text{Node U}: \; C = 3C_{ug}, \quad \text{Node L}: \; C = 3C_{lg} \quad \text{Node N}: \; C = 3C_{ug} + 3C_{lg}$$

$$\text{Nodes } U_A, U_B, U_C: \; C = C_{ag} + C_{ug}, \quad \text{Nodes } L_A, L_B, L_C: \; C = C_{ag} + C_{ug}$$



$$V_{UL}^{(c)} = \frac{V_{UP}+V_{LP}}{2} \quad V_{ULN} = \frac{V_{UP}+V_{LP}+V_{NP}}{3} \quad V_{ABC}^{(c)} = \frac{V_{AN}+V_{BN}+V_{CN}}{3}$$

$$V_{U_AL_A}^{(c)} = \frac{V_{U_AP}+V_{L_AP}}{2} \quad V_{U_BL_B}^{(c)} = \frac{V_{U_BP}+V_{L_BP}}{2} \quad V_{U_CL_C}^{(c)} = \frac{V_{U_CN}+V_{L_CN}}{2}$$

Figure 3-28: NPC Inverter Common-Mode Equivalent Model

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Chapter 4

Medium-Frequency Transformer

A transformer is a key asset component of any electrical distribution system and plays a vital role in energy conversion by transferring power from the primary winding to other windings with no energy storage or loss. Medium-frequency transformers operate using the same basic principles as standard transformers. The main difference is that they operate at much higher frequencies, while most standard transformers operate at 50 or 60 Hz, these medium-frequency transformers operate at frequencies from 20 kHz to over 1 MHz. Operating at higher frequencies offer many benefits, the first of which is its size, allowing for the building of smaller, less expensive, and compact portable electric devices. Secondly, because the transformer is smaller, less copper wire is needed, thus reducing the losses and helping to make the transformer more efficient. Therefore, medium-frequency transformers are preferred over traditional transformers in the power electronic field, such as switching power supplies; converters; and medium voltage inverters. Although we gain benefits from light weight, small size, and high power dense devices, it also poses a number of challenges. Minimizing issues such as skin effects, proximity effects, and electromagnetic interference are a serious concern when designing high-frequency transformers.

Skin effect is where alternating current tends to avoid travel through the center of a solid conductor, limiting itself to conduction near the surface. This effectively limits the cross-sectional conductor area available to carry alternating current flow, increasing the resistance of that conductor above what it normally would be for direct current. The losses due to the skin effect can be reduced through the use of Litz wire. Litz wire is constructed

by weaving multiple smaller conductors together to make an equivalent larger wire gauge. The size of each individual strand is determined by the intended operating frequency, where smaller strands are used for higher frequencies.

Proximity effects, or eddy current losses, are caused by the magnetic fields from adjacent conductors either in adjacent windings or in adjacent turns which cause current to flow in unintended patterns, or in eddy currents. This effect creates unintentional power loss, and it should also be noted that core gaps result in these losses as well. There are a number of techniques that minimize proximity effects, which include selecting a core allowing an increased number of turns or layers and using tape as a physical barrier to keep the winding away from core gaps.

As medium-frequency transformers become more power dense, and regardless of this higher efficiency, heat dissipation becomes a major design consideration. In many situations active cooling is needed through use of a fan, liquid cooling, by mounting the transformer on a cooling plate, or potting in a thermally conductive material.

As all of these things are major concerns in designing medium-frequency transformers, but the EMI characteristics, mainly parasitic capacitance is an under studied design impact that needs an in depth study on.

4.1 Parasitic Effects

A transformer has two main jobs, one is to transform voltage by stepping up or down the voltage to a desired level. The other is to provide galvanic isolation between system ground potentials. Galvanic isolation can be extremely effective for improving noise immunity between circuits. Galvanic isolation is a principle of isolating functional sections of electrical systems to prevent current flow, where no direct conduction paths are permitted. It is an effective method for breaking ground loops by preventing unwanted current from flowing between units sharing a ground conductor. Galvanic isolation works very well for breaking CM conducted ground loops for low frequency systems, but at higher frequencies the galvanic isolation of the transformer has some unique side effects of increasing CM coupling between the isolated circuits through parasitic capacitance.

Higher frequency designs require more care in specifying the winding configuration. This is because the physical orientation and spacing of the windings determine its leakage inductance and winding capacitance, where each are actually distributed throughout the winding of the transformer. Transformers designed for power conversion are driven with trapezoidal waves with fast rise and fall times, and these parasitic effects are typically seen on the rising edge of the current and voltage waveforms.

Transformer leakage inductance and capacitance have an inverse relationship, that is if you decrease one you increase the other. These are trade-offs that the power conversion engineer must account for when producing the best transformer design for a specific application.

4.1.1 Leakage Inductance

Leakage inductance is distributed throughout the windings of the transformer based off the flux created in the primary winding, which does not link to the secondary side. This gives rise to leakage inductance in both windings which do not contribute to the mutual flux. The effects of leakage inductance is primarily observed on the leading edge of voltage waveforms in the form of voltage spikes. These voltage spikes are caused by the stored energy in the leakage flux and tend to increase with load.

To minimize leakage inductance there are a few things that can be taken into consideration. The magnetic core geometry plays a big role in leakage inductance. To minimize leakage inductance, the primary winding should be wound on a long bobbin with the secondary winding wound as close to the primary as possible with a minimum amount of insulation. If layers must be used, the interleaved structure of primary and secondary windings can reduce leakage inductance. To do this you would want to break the primary windings into sections and the place the secondary windings between them. This also poses a problem when worried about electrical stresses, creepage distance, and the minimum insulation requirements between the primary and secondary windings, so careful consideration is necessary.

4.1.2 Parasitic Capacitance

Parasitic capacitance of a transformer have a significant impact on converter operation and play a vital role in the mitigation of CM noise currents created by fast voltage transients. Transformer winding capacitance has a negative impact to the transformer in multiple ways: winding capacitance can lead to harmonic distortion and drive premature resonance; winding capacitance can produce large primary current spikes when operating with square wave sources; and winding capacitance can produce coupling to other circuits.

Windings within magnetic components have conductor materials separated by insulation, so there is capacitance associated with the windings. Keeping turns within the transformer as low as possible will keep the parasitic capacitance to a minimum. The parasitic capacitance in magnetic components can be observed in five different ways: turn-to-turn capacitance; layer-to-layer capacitance; intra-winding capacitance; inter-winding capacitance; and leakage capacitance. These capacitance's can be combined to generate an effective capacitance at the component level. For a transformer, the net effect of the parasitic capacitances are used to model conduction paths for common-mode currents. These common-mode currents can generate EMI noise, and paired with the system inductance (leakage and magnetizing inductance) can result in resonance which can cause ringing in the component voltage and currents.

The intra-winding capacitance, or lumped turn-to-turn capacitance, can result in parallel resonances with magnetizing and leakage inductance and therefore should be kept as low as possible. The intra-capacitance of a winding can be reduced by increasing the distance between layers, by lowering the number of turns per layer, or by having a low value for the relative permittivity.

The inter-winding capacitance is highly undesirable, as it can couple CM currents from primary to secondary sides. In order to estimate the inter capacitance for multiple layered windings, only the outermost layer of the winding is considered since it acts as a screen for the other layers. The most effective method in order to reduce the effect of the inter-winding capacitance is to arrange the windings in such a way that the voltage between adjacent turns of the high- or low-voltage windings are the same.

Both intra and inter-winding capacitances can be influenced by potential screens or shields between the windings, the way windings are grounded, and whether or not the core is grounded. Where grounding the core greatly increases the inter capacitance.

But remember that the cost of reducing parasitic capacitance comes with the increase of leakage inductance and therefore a decrease in power throughput. So we should focus on the dominating parasitics and reduce them with a balancing effect on the leakage inductance.

4.2 Common-Mode Modeling: Method 1

Our intention in CM modeling has primarily been focused on the modeling of the parasitic capacitance, although leakage inductance is important, we are more interested in the conduction paths of high-frequency currents. So to model these high-frequency currents we begin with a simplified transformer parasitic model below

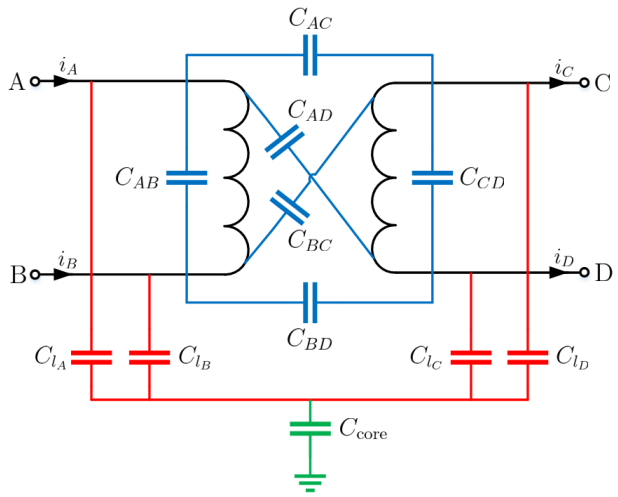


Figure 4-1: Simplified Transformer Parasitic Model

These lumped parasitic capacitances from the simplified transformer parasitic model are used to model conduction paths for the high-frequency currents in the simplest way. The lumped capacitances of the intra-windings of the primary and secondary windings are denoted as C_{AB} and C_{CD}, respectfully. The inter-winding capacitances are C_{AC}, C_{AD}, C_{BC}, and C_{BD}. These inter- and intra-winding capacitances are labeled in blue. Each winding also has leakage capacitance due to the core, these leakage capacitances are denoted as C_{l_A},

C_{l_B}, C_{l_C}, and C_{l_D}, which are labeled in red. Then the core capacitance should be included, in some cases the core is grounded, but for our case we have modeled a floating core with some standoff capacitance, labeled in green. When grounding the core you increase the voltage stresses on the transformer and increase the winding capacitance, so for this reason we model a floating core.

By looking at this simplified transformer parasitic model in Figure 4-1, we notice that the CM modeling procedure for the parasitic capacitance can be broken into two different parts. First, separate the primary and secondary sides and model the leakage capacitance paths on each side. Then model of the winding capacitance, which provides the coupling paths from primary to secondary sides. So let's look at these individually and construct a common-mode equivalent model to accurately represent the high-frequency characteristics of the transformer.

4.2.1 Leakage (Stray) Capacitance

Minimizing leakage capacitance is very important because it can cause asymmetric currents and can lead to high common-mode noise. Each of the windings have leakage capacitance due to it surrounding materials, in our case the core.

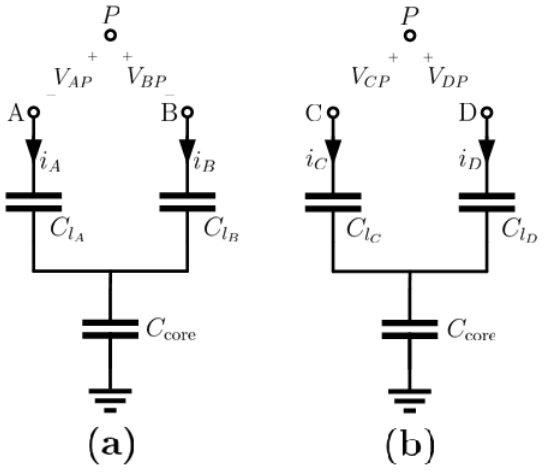


Figure 4-2: HF Transformer: (a) Input Node (A,B) Leakage Capacitance Model, (b) Output Node (C,D) Leakage Capacitance Model

By looking at the simplified transformer parastic model in Figure 4-1 we see that we can separate both leakage paths on the primary and secondary sides, further simplifying the

modeling procedure. Both CM leakage paths on each side of the transformer can be seen as a 2-line capacitor model and the constructed parasitic capacitance model for both leakage paths can be seen in Figure 4-2. Using the input node (A,B) leakage capacitance model and Equation 3.45, the resulting CM expression is

$$V_{Pg} = -V_{AB}^{(c)} + \frac{C_{l_B} - C_{l_A}}{2\left(C_{l_A} + C_{l_B}\right)} V_{c_p,AB}^{(d)} + \frac{i^{(c)}}{\hat{p}\left(C_{l_A} + C_{l_B}\right)} + R_h i^{(c)} \tag{4.1}$$

and the CM leakage path expression for the output node (C,D) is

$$V_{Pg} = -V_{CD}^{(c)} + \frac{C_{l_D} - C_{l_C}}{2\left(C_{l_C} + C_{l_D}\right)} V_{c_p,CD}^{(d)} + \frac{i^{(c)}}{\hat{p}\left(C_{l_C} + C_{l_D}\right)} + R_h i^{(c)} \tag{4.2}$$

Constructing two CEMs for the leakage paths on the primary and secondary sides of the transformer from the expressions above, results in

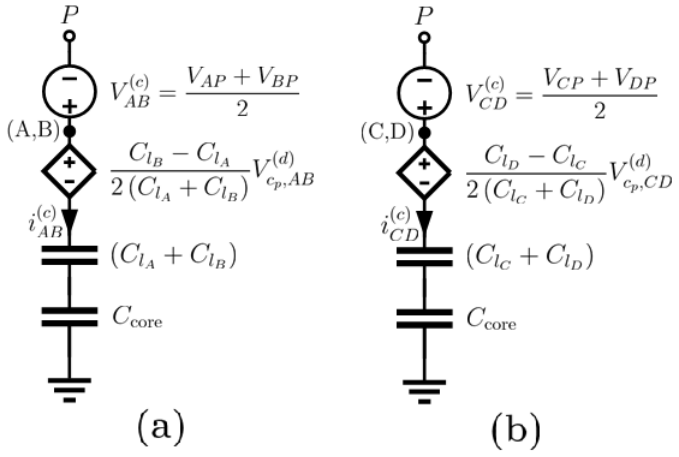


Figure 4-3: HF Transformer: (a) Input Nodes (A,B) Leakage CEM, (b) Output Nodes (C,D) Leakage CEM

It should be noted that although both CM equivalent circuits include the arbitrary point P, they are not going to be connected to the same point. We should be aware that the transformer itself does not have a common point due to the isolation from primary to secondary sides, and that the transformer itself does not generate CM current. The transformer parasitic capacitance acts as a coupling path from one side to the other, and the converters on either side of the transformer is what is generating the CM noise sources. Therefore we should use the arbitrary reference point P as some point that is contained within each of

the converters on both sides of the transformer and use the parasitic winding capacitance as the coupling path for CM noise to flow from one side of the transformer to the other side.

4.2.2 Intra- and Inter-Winding Capacitance

To produce a CM model of the transformer windings, it should be noted that the resistive and magnetic parts (i.e. leakage and magnetizing inductance) of a transformer circuit contribute to the DM operation alone and should not be included in the CM modeling procedure. For this reason we are only looking at the intra-winding and more importantly the inter-winding capacitances of the transformer. Let us look back at our simplified transformer parasitic model in Figure 4-1 and use our super-node approach to help us derive a CM equivalent model. This results with us gathering a super-node of input nodes (A,B) of the primary side and another super-node of the output nodes (C,D) on the secondary side. By doing this we are essentially shorting the primary and secondary nodes, which causes the intra-winding capacitances to be shorted as well. This causes them to vanish from the CM modeling procedure, which makes sense since they primarily contribute to the DM operation. This leaves us with just the inter-winding capacitances in parallel, where these capacitances can be lumped together as one equivalent capacitance.

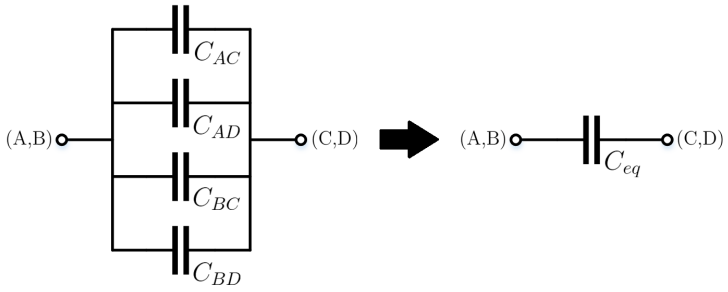


Figure 4-4: HF Transformer: Inter-Winding Capacitance Model and Equivalent Model

The equivalent capacitance is the sum of parallel inter-winding capacitance

$$C_{eq} = C_{AC} + C_{AD} + C_{BC} + C_{BD} \tag{4.3}$$

4.2.3 Medium-Frequency Transformer Common-Mode Equivalent Model

The resulting CEM for the MF transformer is

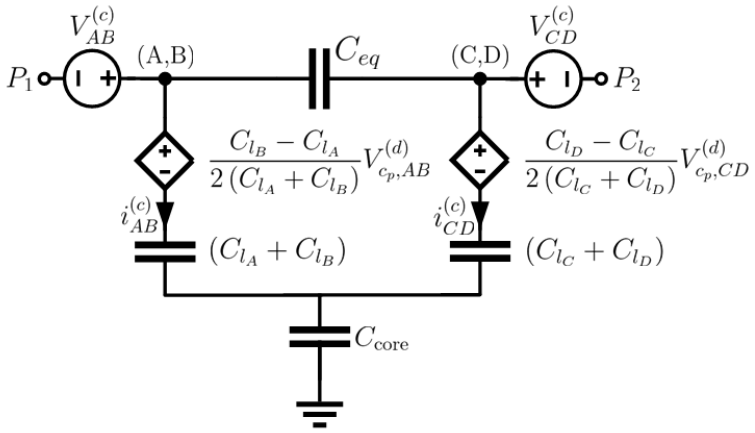


Figure 4-5: HF Transformer CEM

We can now continue the discussion about having two different arbitrary P points. The primary side leakage capacitance CEM circuit has point P_1, which will connect to a common point among the converter on the primary side of the transformer, and the secondary side leakage capacitance CEM circuit has point P_2, which will connect to a common point among the converter on the secondary side of the transformer. Then the inter-winding capacitance CEM will connect between the nodes (A,B) and the nodes (C,D) on the primary side and secondary side leakage capacitance CEM circuit, respectively.

4.3 Common-Mode Modeling: Method 2

In this section, another CM modeling method is derived and serves more as a case study and will not be intended for use in the complete CM model for the NPC DAB. There are many ways of coming up with equivalent circuits, this approach uses methods of superposition and thevenin theories.

As explained earlier, the intra- and inter-winding capacitances are influenced by the way that the windings are grounded. So lets focus in on the winding capacitance for an approach where we explore an example winding ground structure for a flyback converter transformer. The winding structure for a flyback converter has a primary ground connected

to the upper rail of the transformer input and a separate secondary ground on the lower rail of the transformer output.

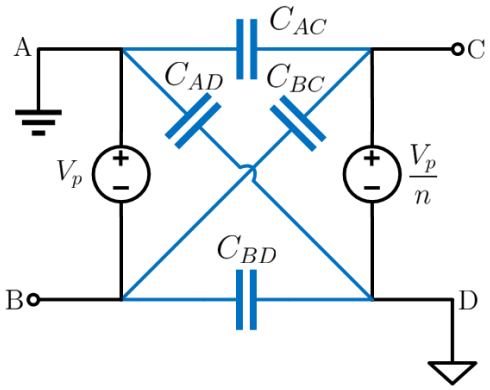


Figure 4-6: Flyback HF Transformer Parasitic Model Example

The modeling procedure used for this transformer model will not follow our traditional mathematical modeling procedure, instead we will use a mix of superposition and thevenin theorems to come up with a CM model. The simplified transformer parasitic model in Figure 4-6 does not include leakage or intra-winding capacitance. When grounding the input or output line to the transformer, in theory, the leakage paths would be eliminated on that line. Our main intent is to understand how the winding parasitics are affected by the grounding structure, so for the time being let us neglect the possible leakage paths that may be present in the transformer. We assume that the intra-winding capacitance is primarily DM operation and would not be included in the CM modeling procedure. The intra-winding capacitance is replaced with voltage sources for the primary and secondary sides, we have pre-determined the CM conduction path from A to D, and all of this allows us to analyze the inter-winding capacitance between both sides of the transformer.

This model can be further simplified by using Thevenin and superposition. We use superposition on the voltage sources to calculate the equivalent voltage and then to find the equivalent capacitance by shorting all the sources. By applying superposition we construct two different circuits, one that has the primary side voltage and the other that consists of the secondary side voltage

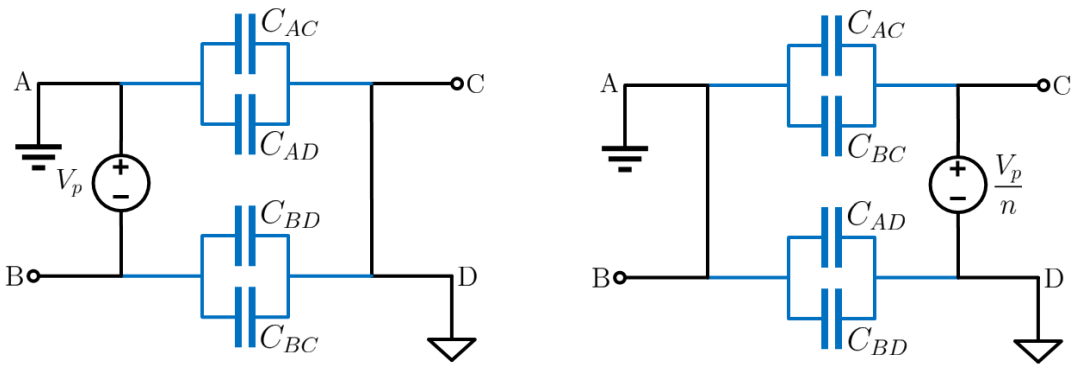
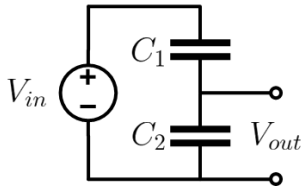


Figure 4-7: Flyback HF Transformer Superposition

With superposition complete we then use a simple voltage divider on each circuit to find the total equivalent voltage drop across the inter-winding capacitance. Here is a simple voltage divider for reference



$$V_{out} = V_{in}\frac{C_1}{C_1 + C_2}$$

Figure 4-8: Capacitor Voltage Divider

With calculations below

$$V_{eq} = \frac{1}{C_{total}}\left[V_p\left(C_{BD} + C_{BC}\right) + \frac{V_p}{n}\left(C_{AC} + C_{BC}\right)\right] \tag{4.4}$$

$$C_{total} = C_{AC} + C_{AD} + C_{BC} + C_{BD} \tag{4.5}$$

$$Z_{eq} = \frac{1}{j\omega C_{total}} \tag{4.6}$$

We know that we have simplified the model as much as possible when the ported networks of the transformer is simplified to one voltage source and two equivalent passive elements. Let's choose the one voltage source as the primary side voltage, and using our determined CM path from A to D, our equivalent capacitors should be the capacitors that connect from our primary side to D. One of the capacitors will be the capacitor between C and D, and then we will lump the rest of the capacitance in the capacitance from B to D. The lumped

equivalent capacitance can be denoted as C'_{BD}.

$$C_{total} = C_{AD} + C'_{BD} \tag{4.7}$$

$$V_{eq} = V_p \frac{C'_{BD}}{C_{total}} \tag{4.8}$$

$$C'_{BD} = (C_{BD} + C_{BC}) + \frac{1}{n}(C_{AC} + C_{BC}) \tag{4.9}$$

Such that our equivalent voltage can be expressed in the following way

$$V_{eq} = \frac{C'_{BD}}{C_{AD} + C'_{BD}} V_p \tag{4.10}$$

We can express this equivalent voltage to a equivalent circuit, resulting in a CM equivalent model that looks like this

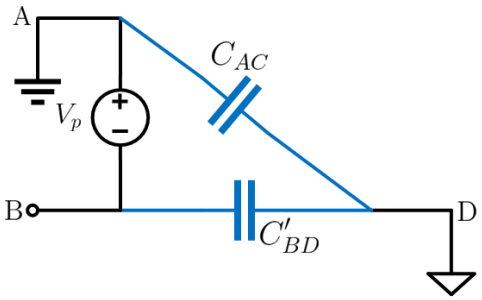


Figure 4-9: Flyback HF Transformer CEM

This modeling approach can be extended to other examples of flyback converters using auxiliary windings or if shielded windings are used.

This CM equivalent model will not be used moving forward because studying flyback converters is not in our area of research and doesn't sync up with our mathematical modeling procedure very well. So moving forward with our research progress for validating and performing sensitivity analysis on the HF transformer, Method 1 CM equivalent circuit model will be the preferred choice.

Chapter 5

EMC Testing and Validation of Models

With the CM equivalent models developed in the previous chapters we now need an efficient and accurate EMI characterization platform and reduction methodology for the support in designing medium voltage power electronic based distribution systems. To form a methodology suited for these challenges we must begin a validation process for our CM mathematical modeling methods and eventually produce measurement hardware for EMC testing.

5.1 Electromagnetic Compatibility (EMC) Testing

EMC testing exists to ensure that our electrical devices don't emit a large amount of electromagnetic interference, through either radiated or conducted emissions, and that our device continues to function in the presence of other electromagnetic phenomena. There are many regulatory agencies that have placed limits on the level of emissions that our electrical devices are allowed to generate, and often times we are mandated to abide to these limits. If you manufacture products with electronics inside, then it is almost definite that you are going to need to care about the EMC testing.

History of EMC Testing

Since we first began to understand and utilize electricity, the effects of EMI have been observed and regulated. This may seem like a modern day problem with the vast amount of electronic devices in our lives, but EMC compliance testing dates back into the 19th century. The use of circuit breakers and lightning rods in homes during the 1870s was in response to the impact of sudden EM radiation pulses. In 1892 the Law of the Telegraph in the German Empire arose because they observed that EMC disturbances have a negative impact on telegraph cables. As the 20th century rolled around with a rapid industrializing society, EM compliance was no longer just an infrastructural problem, as more people were able to afford electronics in their homes the potential for conflict within devices became readily apparent. Founded in 1906, the International Electrotechnical Commission (IEC) became the world's leading advocate for the standardization of EMC testing. CISPR, a branch of the IEC dedicated to the problem of radiated emissions, was founded in 1933. Then the FCC has had limits on transmitter emissions since 1938 and has continued to expand its rules in response to explosion of electric devices over the following decades, until in 1989 when the FCC standardized emission limits for general applications.

The development of power grids, the rise of the automobile, and the consumer market have changed the way we use electricity. Each change has created a market for enhanced EMC testing equipment for the safety of ourselves and the environment. Today, EMC compliance testing is a major part of the development of any electrical product.

Radiated Emissions Testing

Radiated emissions testing is the most common EMC test undertaken around the world. It involves measuring the electromagnetic field strength of the emissions that are unintentionally generated by a product. Electromagnetic waves do not extend out from a product in a nice spherical pattern, they are directional, so a test lab has to vary the height of the receiving antenna. The antenna picks up both the signal directly from your device as well as the signal that bounces off the ground. To increase the measurement accuracy the ground must be flat and covered with an electromagnetically reflective surface. The test lab will then

scan the frequency band of interest and look for emissions that are close to the standard limits. Using a method called 'maximization' the test lab can then quantify the amplitude of the field strength. Maximization is the process used to find the maximum amplitude of the emissions from the device. Maximization can be performed in multiple ways: manipulating cabling; rotating the device within 360 degrees on turntable; moving the antenna height up or down; flipping the polarization of the antenna; and varying equipment modes of operation.

Test labs are usually performed in Anechoic Chambers, which houses the device within a shielded room. This is extremely helpful because it attenuates the ambient radio signals, making it much easier to distinguish what is coming from your device. The inside of a anechoich chamber is lined with some kind of RF absorbent material to keep reflections of signals to a minimum. The distance between the antenna and the device under test is typically meters away to ensure that you are measuring the field strength in the far field opposed to the near field. As you approach the near field, the electric field will not be stable and the measurements will be less accurate. The EMI reciever is a spectrum analyzer and is the backbone of an EMC tests measurement equipment.

The frequency range that a test lab should investigate typically depends on the highest clock rate present in the device. For some industry and product specific standards the frequency range is fixed. The lower frequency range would then be determined by the lowest frequency clock rate present in your device.

Conducted Emissions Testing

Power electronic devices create electromagnetic energy and a portion of it will be conducted in unintentional paths, such as coupling back onto the power supply. To restrict the amount of interference the device couples into undesired locations, test labs measure these emissions, typically between 100 kHz and 30 MHz, and verify that they comply with the standards limits. Doing this ensures that nearby devices won't be affected by your device and that the power supply remains fairly clean.

The typical setup for testing conducted emissions from a Device-Under-Test (DUT) requires the following things: an EMI receiver or spectrum analyzer; a Line Impedance

Stabilization Network (LISN); and a ground plane. The DUT, LISN, and EMI receiver are all placed and connected to the ground plane. The LISN is a three-port device connected to the DUT, EMI receiver, and power supply. The LISN is a low-pass filter and provides a standardized impedance at RF across the DUT measurement point. We need a known impedance otherwise our measurements would not be able to be repeatable. The impedance of AC power supplies vary between different sources, so the LISN standardizes this impedance between lab setups. The LISN couples the measurement point of the DUT to the EMI reciever and filters unwanted interference signals coming from the power supply, which is helpful by minimizing the noise from the power supply and allowing us to measure only the noise from the DUT. The EMI receiver with correct cables and transducers are used to measure the conducted emissions emanating from the device. Unlike oscilloscopes, the EMI receiver looks at signals in the frequency domain. The spectrum analyzer will display the amplitude of the RF signal on the vertical scale and the frequency on the horizontal scale. The vertical axis is calibrated in amplitude, although there is possibility of choosing a linear or logarithmic scale, a logarithmic scale is chosen for most measurements. This enables signals over a much wider range to be seen on the measuring receiver and limits are specified in decibels.

Here is a typical circuit for a LISN

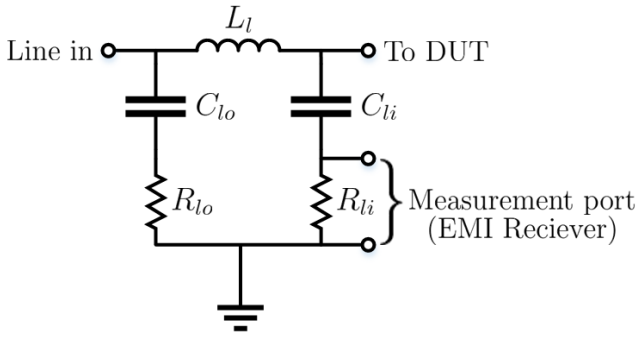


Figure 5-1: Line Impedance Stabilization Network (LISN)

The circuit inside a LISN is fairly simple. It consists of some filtering, an 'outboard' side (line in) that connects to the power supply, an 'inboard' side that connects to the DUT, and a port that connects to the spectrum analyzer. The component values used are determined from MIL-STD-461 CE102, which is a military test standard that pertains to RF potentials

for conducted emissions testing. The LISN inductor, L_l, is 50 μH, which models a long cable ran to the power supply. On the outboard side there is a capacitor, C_{lo}, which is 8 μF and the resistor, R_{lo}, is a value of 5 Ω. On the inboard side there is a capacitor, C_{li}, which is 0.25 μF and the resistor, R_{li}, is a value of 1 kΩ. The measurement port is across R_{li} and typically has a 50 Ω resistor across it for impedance matching the EMI receiver.

5.1.1 EMC Testing Lab Setup

Our research has been directed towards an accurate EMI characterization and reduction methodologies to support our design of the NPC DAB as a sub module for much larger system applications.

A simplified look at our proposed lab setup can be seen in Figure 5-2.

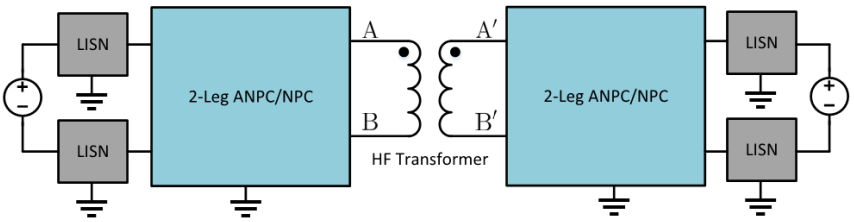


Figure 5-2: Lab Validation of ANPC Dual Active Bridge

The LISNs are designed in accordance to MIL-STD-461 CE102 and can be seen in Figure 5-1, a full-bridge NPC is placed on both sides of the transformer, and then the HF transformer provides the interface between both converters. This comprises our full DUT that we intend to do both radiated and conducted emissions testing on. The custom designed EMI characterization platform presented here uses a unusual configuration of the LISNs on both the input and output of the converter. This configuration allows us to observe the conducted emissions generated by the converter, which is often times difficult to decipher when connected to a larger system. By taking the difference of the input and output CM currents, it is possible to directly relate and determine the displacement current that the converter is generating. By moving the LISNs around, for instance, moving the output LISNs to the other side of the primary converter we can directly see what that converter is emitting without the influence of any other component within the assembly. This provides

us with an in depth understanding of the conducted emissions of each converter and the whole system.

Due to limited resources, we are not currently able to develop a hardware setup for this sub system. The initial project was designed for a 13 kV primary side voltage and a 7.2 kV secondary side voltage, which means we would need 10 kV rated power modules for our converters. But the manufacturing of 10 kV rated devices is an active area of research and not yet developed for commercial use, plus they are very expensive devices. So to make an affordable and practical NPC DAB we need to scale down the voltage, but how much do we need to scale down the voltage. Well that depends on the information provided and our choice of the medium-voltage SiC MOSFET modules. To my knowledge there is only a select few rated voltage levels we can choose from, these are 1.2 kV, 1.7 kV, 3.3 kV, and 6.5 kV, which are all manufactured by Cree/Wolfspeed. The modules will be chosen by system application and current capacity as well its pricing and availability. Aside from just the modules there are many other factors we should address before producing the lab testbed. We must design a gate drive circuit, buswork layout, neutral forming capacitors, and controller implementation. All of this is just for the NPC converter, we also need to design and build a transformer, which is another ongoing project within the research team. Once all of this is put together we will need to design LISNs for the input and output terminations and provide an input power supply. Then all of this will be mounted on a lab testbed that has a ground plane.

When we have finally put all of this together we will be ready to conduct EMC testing for radiated and conducted emissions. We currently have a lab testbed with a ground plane and custom LISNs that is being used for EMC testing. We are also in the process of building an anechoich chamber which will be our main hub for EMC testing. These things are all very exciting but it must be saved for future work.

Even though we are not yet capable of performing hardware implementation for EMC testing, there is still many things that we can do in the simulation world. This brings us back to CM modeling and validation.

5.2 Common-Mode Modeling and Validation

Since a hardware setup is currently not an option for us, we must impose a white-box modeling approach for the validation of our CM equivalent models. For simulation of our NPC Dual Active Bridge depicted in Figure 5-2 we are using MATLAB Simulink which is a graphical programming environment for modeling, simulating and analyzing mulitdomain dynamical systems. We use a PLECS Blockset integrated into MATLAB Simulink, where the controls are created in Simulink and the electrical circuits are modeled in PLECS. PLECS gives us advantages that can't be done in Simulink alone; we are able to model switch characteristics more accurately, it allows us to build an accurate model of parasitics within a mixed-mode environment, and it allows us to speed up the simulation considerably without sacrificing accuracy. Thus the integration of the PLECS software is ideally suited for modeling and simulation of modular multilevel converters.

We have developed a phase shifted modulation control scheme in Simulink, which directs power flow by shifting the leading edges of both high- and low-voltage side switches. For simplicity sake we have developed a single phase shift modulation scheme, where we predetermine the switching frequency and duty cycles for high- and low-voltage sides and then apply closed loop controls to determine the phase shift needed to achieve a desired power level. The modulated gate pulses are then routed to our PLECS Blockset where we model the NPC Dual Active Bridge circuit.

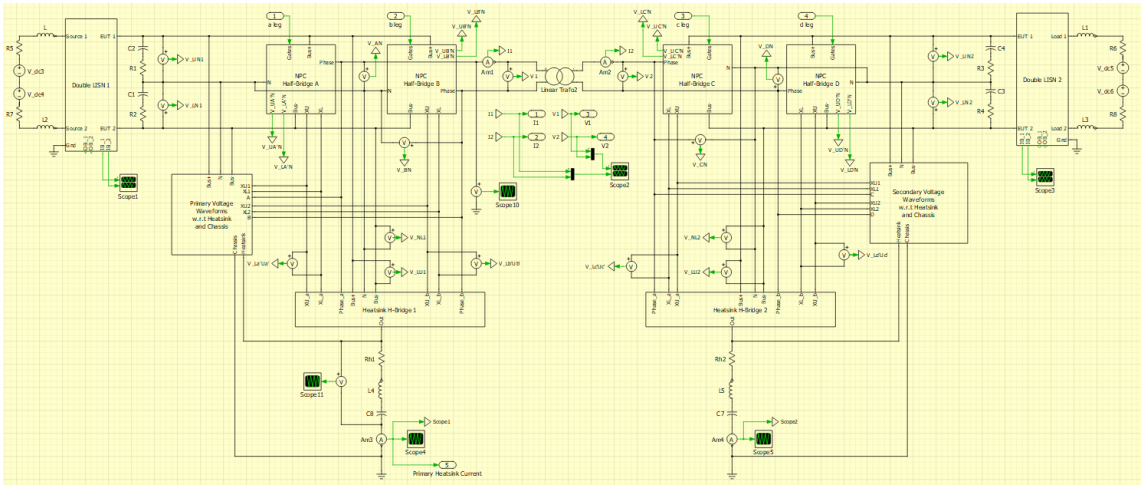


Figure 5-3: PLECS MM Circuit of ANPC Dual Active Bridge

This MM circuit models a floating NPC Dual Active Bridge. The MM circuit contains DC voltage sources on both sides of the Dual Active bridge. The initial voltage for the system was 13 kV to 7 kV, using 10 kV power modules. But due to lack of knowledge of device characteristics and parasitics for the 10 kV modules, we needed to scale down the voltage. Based on what we had in the lab, the availability of spec sheets, and measured parasitics forced the decision to use 1.2 kV power modules. So the voltage was scaled down linearly to approximately ten percent the initial voltage, meaning the system is now a 1.5 kV to 850 V Dual Active Bridge. The converter topology for both the high- and low-voltage sides is an NPC full-bridge as seen in Figure 3-17, using CREE CAS300M12BM2 SiC Modules [45]. We have measured the parasitic capacitance of the modules as

$$C_{ug} = 203\text{pF}, \quad C_{lg} = 47\text{pF}, \quad C_{ag} = 227\text{pF}$$

The modules are then routed to a floated heatsink through these parasitic capacitors. The floated heatsink is modeled as a simple series RLC circuit to a ground reference. Then there are LISNs, following MIL-STD-461 CE102 standards, connected between the sources and converters on the input and output sides that are also connected to reference ground, this allows for CM current circulation with known ground loops and provides a standardized impedance for the input and output of the system.

The interfacing between the converters is the MF transformer which is modeled as a two winding linear transformer. The hardware design of the MF transformer has been an iterative process and is still an ongoing project, but we do have some preliminary results that can be put in the model. These can be seen in the table below.

Table 5.1: HF Transformer Parameters

		Value
Leakage Inductance	Primary Side	28.15 μH
	Secondary Side	16.91 μH
Winding Resistance	Primary Side	28.93 mΩ
	Secondary Side	2.67 mΩ
Magnetizing Inductance		1.92 H
Winding Ratio		1.8

Although the FEM simulation of the transformer has provided us parasitic values, they will not be included in this analysis. That is because, to my knowledge, it is nearly impossible to model the parasitic capacitance in PLECS without changing system dynamics. There would need to be a custom transformer block that includes winding capacitance, has port access to the core to connect leakage capacitance, and necessitates the need to ground or float the core. All which is not possible with current PLECS blocks, so a temporary placeholder will be done by using this linear transformer block until we find a way to accurately model the parasitics of the transformer.

Below is a table that shows a summary of system specifications.

Table 5.2: System Specifications

		Value
Topology		ANPC DAB
Switching Frequency		20 kHz
Power		80 kW
Primary Side	Voltage	1.5 kV
	Current	53 A
Secondary Side	Voltage	850 V
	Current	94 A

With the development of a full simulation model for the NPC DAB, we have ran and analyzed the system at steady state operating conditions. The plots in Figure 5-4 show the operating conditions at the interface between both NPC converters in steady state. The first plot shows the 5-step voltage waveforms for the high- and low-voltage sides of the transformer, with the corresponding currents in the second plot, and the final plot shows the power on the secondary side of the transformer. For the power plot, the blue line is the actual power, this power is then filtered and shown by the green line, and then we have a commanded power in red. In steady state we see that our filtered power is equal to our commanded power, so we know that the system is operating as intended.

With an accurate simulation, we are able to analyze CM operation. We could perform EMC testing on the device using the measurement ports within the LISNs, but without hardware it isn't much of a priority right now. Instead we want to look at the CM displacement current through the heatsink generated by the converters, and validate these with our CEM derivations.

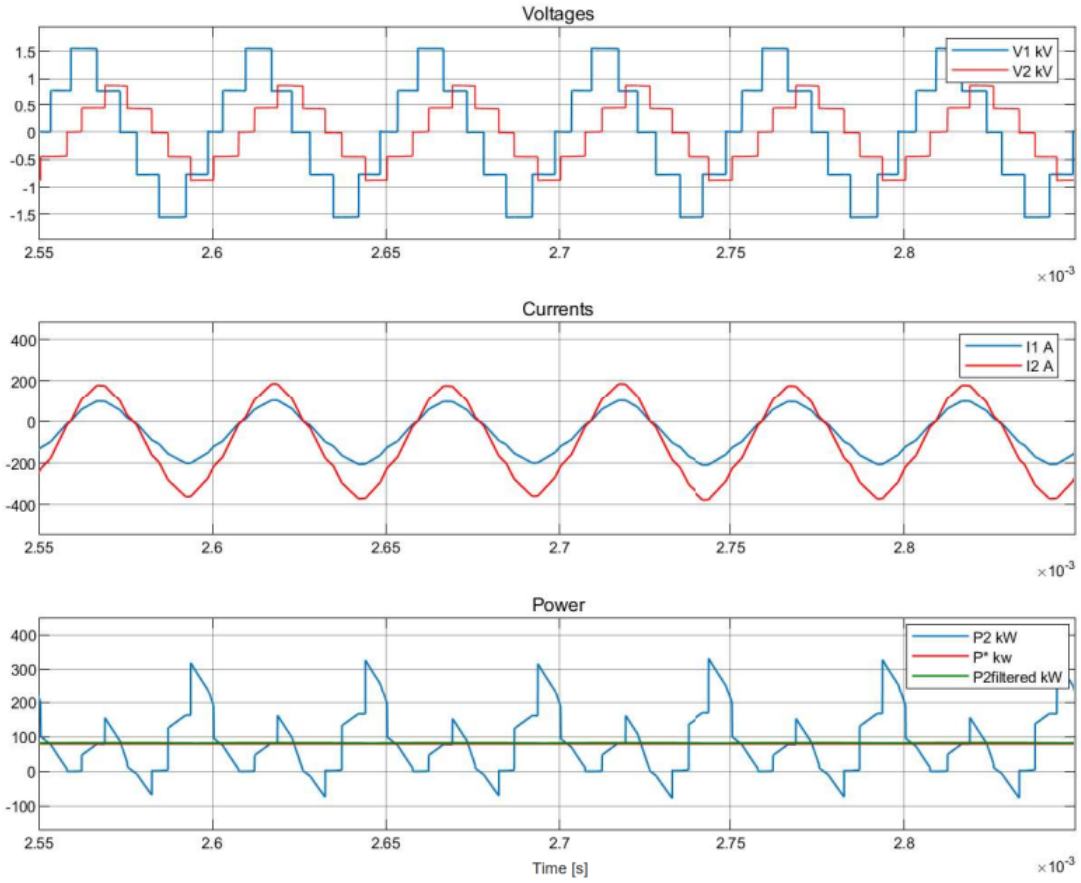


Figure 5-4: Steady State Operating Conditions for NPC DAB

5.2.1 CM Displacement Current

As explained in Section 3.2, we know the main driver for CM conducted emissions is due to the power modules higher switching frequencies and high voltage transition rates (dv/dt). When a converter switch receives its gate pulse, it can't turn on instantaneously and instead turns on with some slew rate. Figure 5-5 shows a plot for a typical voltage transition rate for one of the MOSFETS within the converter on the high-voltage side. The switch has a similar turn off rate, so we tend to see trapezoidal voltage waveforms across switches and as we increase the switching frequency we see more of these trapezoidal waveforms over a given time period, this greatly affects the CM displacement current. When these switches turn on within these power modules, these (dv/dt) rates drive current through the modules parasitic capacitance into the systems heatsink towards the ground potential. By looking at the transition rate in Figure 5-5, the approximate the time it takes for the switch to

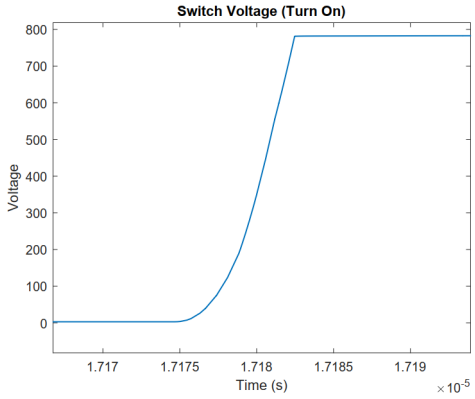


Figure 5-5: MOSFET (dv/dt) during Turn On

turn on fully is roughly 10 ns, and the change in voltage is 800 V. Then on average we have a parasitic capacitance around 100 pF, therefore we would expect the current through these parasitic capacitors to be around a few amps. So, we should expect to see spikes in displacement current through the heatsink as each of the switches turn on inside the converter to be on the order of amps.

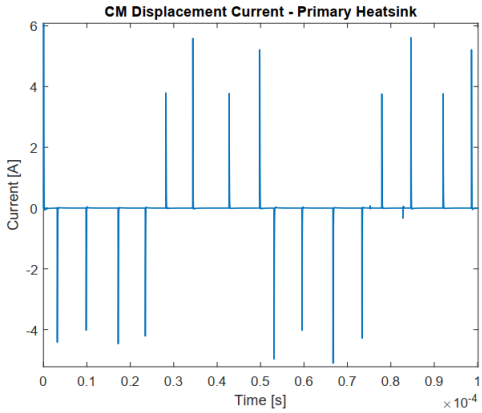


Figure 5-6: CM Displacement Current - Primary Heatsink

Measuring the current through the heatsink, with a plot shown in Figure 5-6 we see spikes in current on the order or amps in the positive and negative directions, just as expected. So at this point we have successfully modeled and simulated the MM circuit and verified conducted CM current through the heatsink generated by the converter.

The only downside to solely using simulation to predict CM conducted emissions is that it starts to pose a computational burden as systems get more complex. Just this simulation model that runs for a few milliseconds of real time takes more than a half hour to complete.

This circuit is relatively small consisting of only a DC/DC converter using a MF transformer interface which provides isolation from both full-bridge converters on either side. So why does it take so long? It is the switch commutation and undesirable current paths that is eating up much of its computing power, where the solver has to go through many small transient circuits analysis's every few microseconds. Now lets think about scaling this system up to a modular multi-level converter or any other larger system application, this could pose a serious computation burden if we are only looking at predicting CM emissions for the system. Is there other ways we can predict CM emissions without doing a full system analysis? The answer is yes, we can do it through our CM equivalent circuits that we have developed.

The MM models, like the one we have just simulated, produces results for the full system operation and CM emissions through the CM conduction paths. But, the CM equivalent models we have developed can isolate the CM behavior without the need of a full operational system and extra switch commutations. Producing a full system model for simulation can take a lot of time because you need to create controls, build the circuit, enter parameters, and then after you complete that you still need to wait for the simulation to run before you see results. So these CM equivalent models seem like the preferred option for predicting CM currents without the computation burden of simulating a full system, saving precious time. Before we can use these CM to their full potential we must first construct a CEM for the full system that we are analyzing and then validate the CEM using our MM model in PLECS.

In the next section, the full system CEM will be constructed, a validation process for the CEM will be performed, and then an explanation on how we can begin to use these CEM circuits for predicting CM emissions generated by the converters.

5.2.2 Construction and Validation of CEM

With the completion of the derived CEMs for converters in Chapter 3 and the derived CEM for the HF transformer in Chapter 4, we can begin constructing the full system CEM for the NPC DAB, and using Figure 5-2 as reference. When constructing these CEMs in the previous chapters we left the arbitrary P points as they were, but as we begin to piece the

CEMs together we must now chose a common point that is actually within the circuit and is distinguishable from ground potential. Since the circuit seen in Figure 5-2 is symmetric about the transformer, I will begin constructing the total system CEM starting on the outside and going in. That is I will begin from the DC source, then the LISN, then the NPC full-bridge converter, and finally the MF transformer. Based on symmetry, everything on the secondary side of the transformer will just be mirrored from the primary side. To distinguish the secondary side from the primary side, I will be using a prime ($\prime$) notation.

LISNs CEM

The DC sources contribute to the DM operation only and are not included in the CM models. Next to the DC source are two LISNs, one connected to the upper rail and the other connected to the lower rail. Since both LISNs are the same they can be treated as symmetrical impedance, therefore the CM equivalent model for the LISNs is just a parallel combination of the impedance.

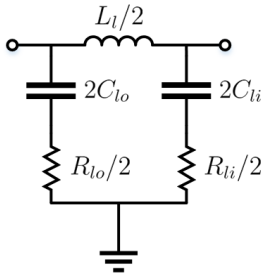


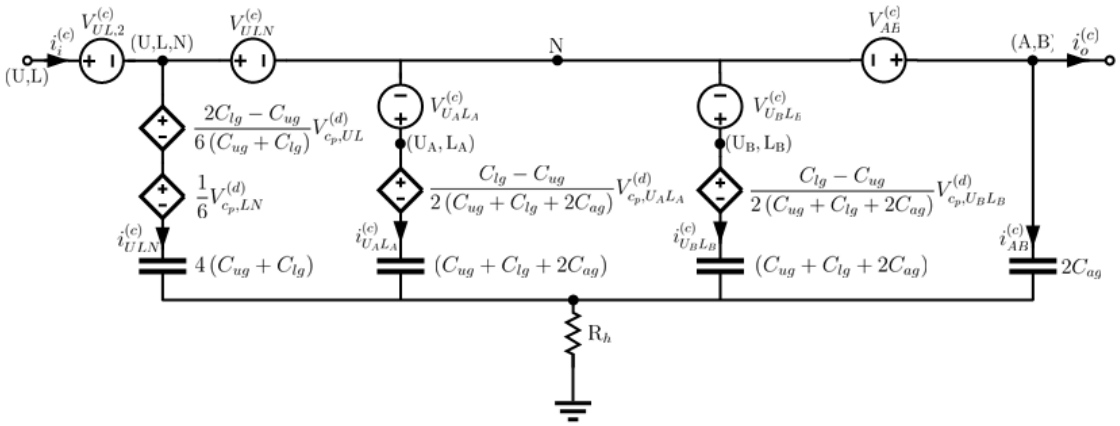
Figure 5-7: 2-Line LISN CEM

The CM derivation of the LISNs is trivial, so there is no need to show the derivation. The inboard side of this CEM will be connected to the node (U,L) and the outboard side will not be connected to anything since the DC source is not part of the CM model.

NPC Full-Bridge CEM

We previously derived the CEM for the NPC full-bridge converter in Chapter 3, for reference it can be seen in Figure 3-26. The arbitrary point P is often chosen by picking a common point among most CM branches. I believe that choosing the neutral point N is a wise choice since it splits the DC link and it is shared between all branches. The resulting CEM for the

NPC Full-Bridge converter choosing P=N can be seen below



$$V^{(c)}_{UL,2} = \frac{V_{UN} + V_{LN}}{6} \qquad V^{(c)}_{ULN} = \frac{V_{UN} + V_{LN}}{3} \qquad V^{(c)}_{AB} = \frac{V_{AN} + V_{BN}}{2}$$

$$V^{(c)}_{U_AL_A} = \frac{V_{U_AN} + V_{L_AN}}{2} \qquad V^{(c)}_{U_BL_B} = \frac{V_{U_BN} + V_{L_BN}}{2}$$

Figure 5-8: NPC Full-Bridge CEM w/ P = N

Although U and L are shared common points, choosing these points make the middle branches CM voltage sources, $V^{(c)}_{U_AL_A}$ and $V^{(c)}_{U_BL_B}$, to be more complex. If we think about choosing U or L for the arbitrary point instead of N, these voltage sources will no longer be across one switch but multiple switches. For this reason, we want to veer away from choosing these points even though they are possible choices. We can also pose this argument when analyzing the CM voltage source, $V^{(c)}_{AB}$. But choosing U, L, or N nodes will mean that this CM voltage will always be across multiple switches, so having N as the arbitrary point still is the most viable common node. The only difficultly that might be encountered when probing these CM or DM voltage sources is that there might be limited access to these nodes. But for our lab setup we are motivated to keep access to the nodes.

MF Transformer CEM

For the complete construction of the CEM for the MF transformer, with reference to the original CEM in Figure 4-5, we choose the arbitrary point as the same point we used for the NPC full-bridge on each corresponding side. That means for the primary side we choose P_1=N and for the secondary side we chose P_2=N′, resulting in the CEM below.

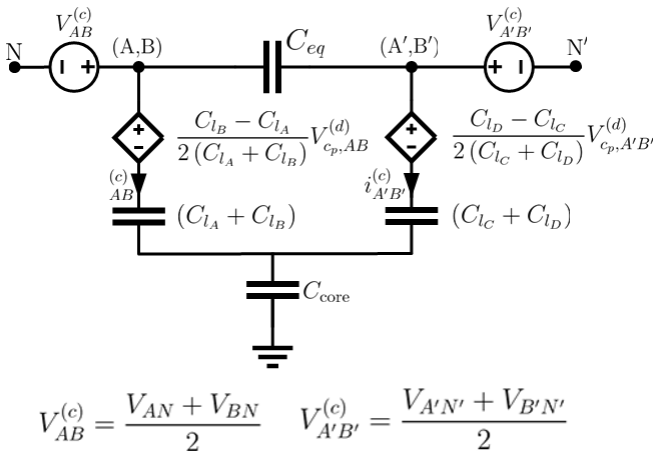


Figure 5-9: HF Transformer CEM

Doing this easily allows us to connect the MF transformer CEM to the NPC full-bridge CEM. They both also conveniently share the CM voltage, $V_{AB}^{(c)}$, so we don't need an extra CM voltage source to sync them together. This intuitively makes sense too, because the MF transformer does not generate CM noise since it doesn't contain switching elements. Instead the MF transformer provides coupling paths for the CM currents to pass through the MF transformer from primary to secondary sides and vice versa. The MF transformer also provides CM current paths from the terminals to the core through leakage paths and then into the ground potential. So as long as we provide a CM input voltage from the converters that is all we need, other than the DM voltage coupling from the terminals that show up in our leakage paths, of course.

Full System CEM

A systematic approach has been gone through for setting up the CEM for the LISN and NPC full-bridge on the primary side as well as setting up the CEM for the HF transformer itself. For the secondary side, we will just mirror everything we did on the primary side and denote everything with prime notation. The full system CEM can be seen on the next page, since the CM circuit is so large it needs to be broken into a couple parts so everything is readable. The nodes are labeled, so the full system will then just be a connection of the each of these parts at the labeled nodes.

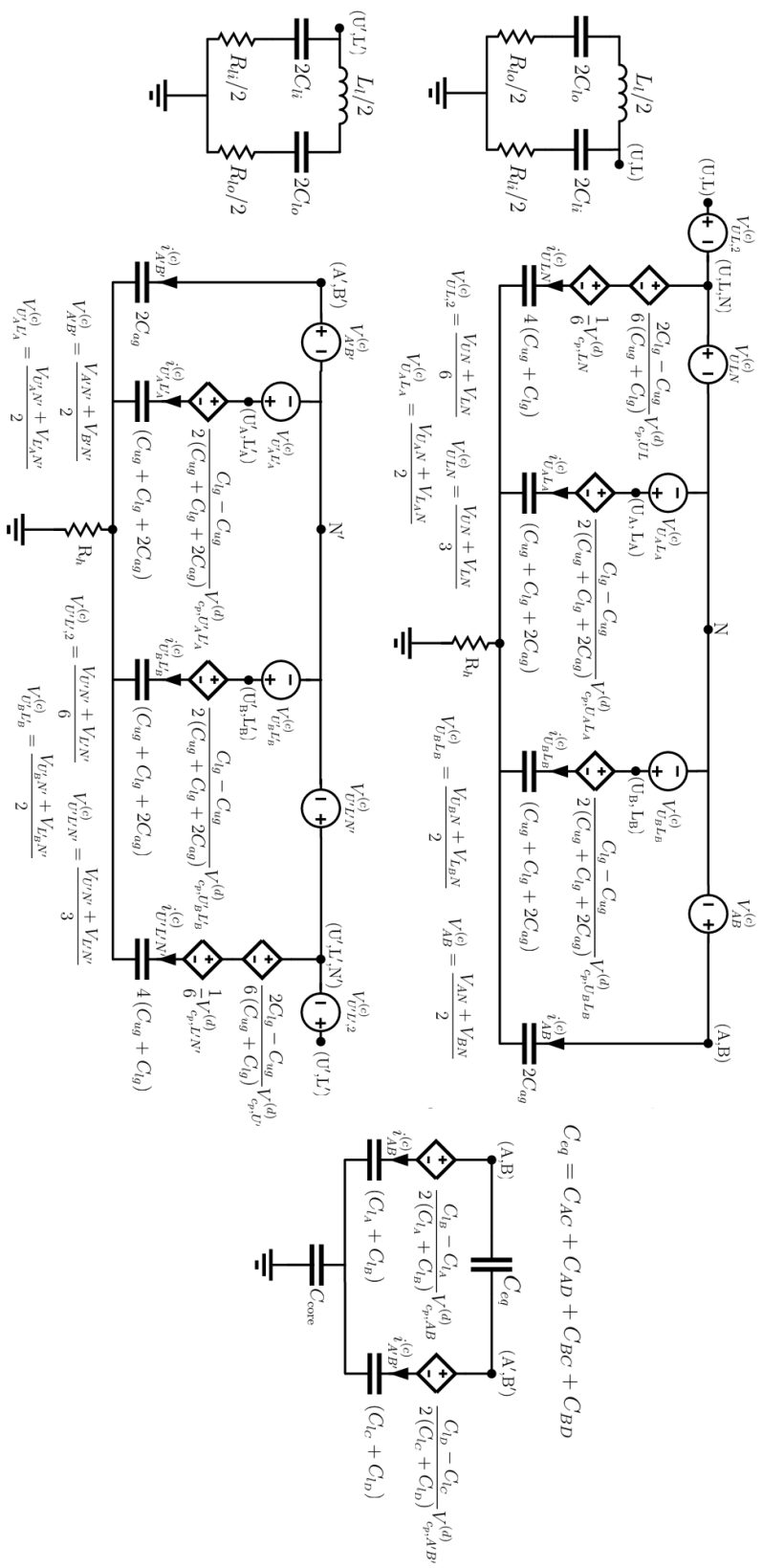


Figure 5-10: Full System CEM - NPC DAB CEM

Validation of Full System CEM

Now that the full system CEM has been constructed, we can now begin the validation process. To validate our CM equivalent model, we are going to bring the constructed model in Figure 5-10 into our PLECS model. Here is the built up model inside PLECS.

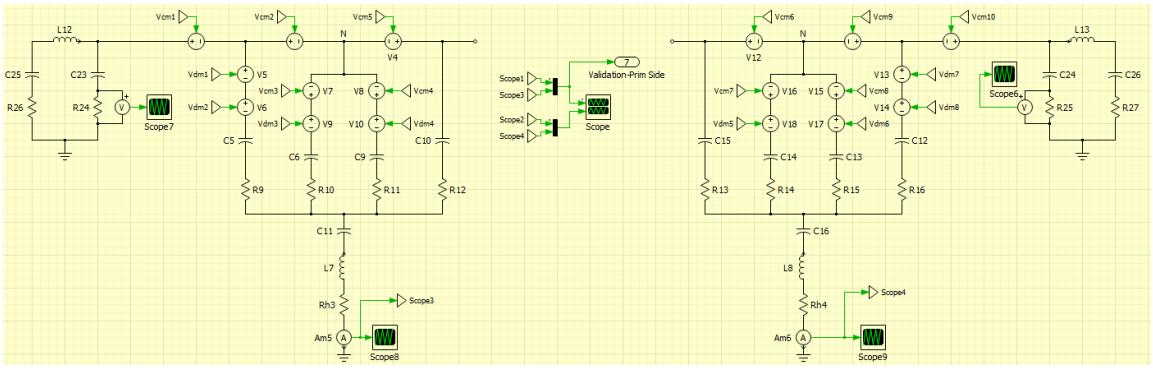


Figure 5-11: CEM PLECS Circuit used for Validation

You may have noticed that the CEM for the HF transformer is not included, this is because we can't accurately model the transformer parasitics inside the MM circuit. Technically we could add in the CEM for the HF transformer to predict the CM currents displaced through the transformer, but the intent of this section is to validate our CM equivalent models. Since we were able to simulate the CM conducted paths from the converter, the only CEM we can validate at the moment is the NPC full-bridge converter. The CEM consists of controlled voltage sources in which we probe our mixed mode circuit and then plug them into these controlled voltage sources. If we look at the CM voltage V_{UN}, the probed voltage is from node U to node L, this should be intuitive. The DM voltage sources is a little different, if we look at the DM voltage source $V^{(d)}_{c_p,UL}$ presented below,

$$V^{(d)}_{c_p,UL} = V_{c_p,U} - V_{c_p,L}$$

we cannot physically probe the parasitic capacitance in a hardware setup, so we need to probe this DM voltage in a different way. If we look at the KVL loop created in these parasitic loops, we can actually probe across the nodes between the parasitic capacitance. This means we can probe from node U to node L and this will provide us the same DM voltage needed to excite the DM coupling term into the CM model. With all of this explained

we can now run the simulation and provide results needed to validate the CM equivalent models. Here is the conducted CM current from both the MM circuit and CM circuit.

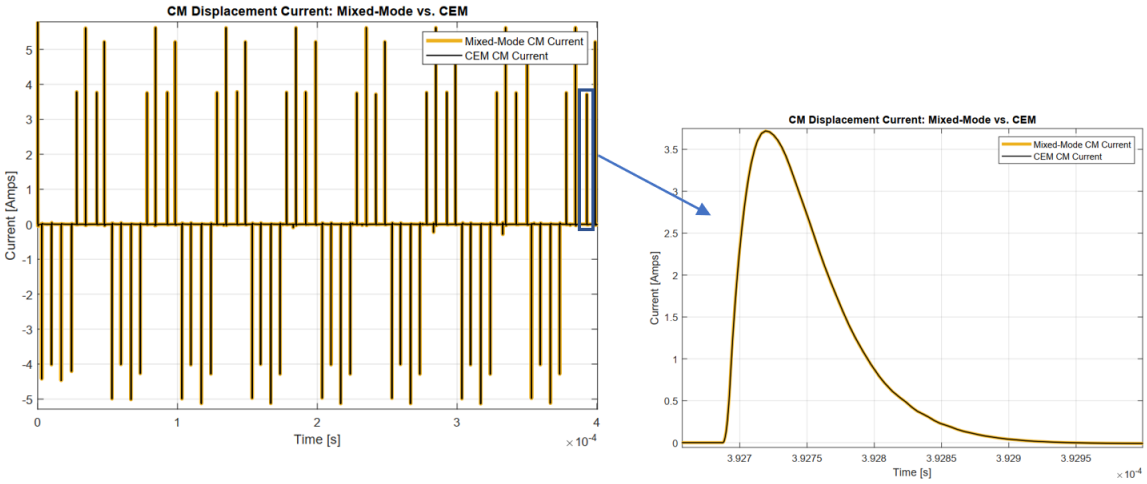


Figure 5-12: CM Currents used for Validation of CEM

On the main plot to the left we have measured the CM displacement current through the heatsink from both the MM model and the CM model. We see that both models pretty much produce the same results. Zooming in on one of the current spikes, it looks like we have an exact match. This means we have a very accurate modeling approach for predicting CM conducted currents. The amount of error in the time-domain simulation is determined between both CM currents.

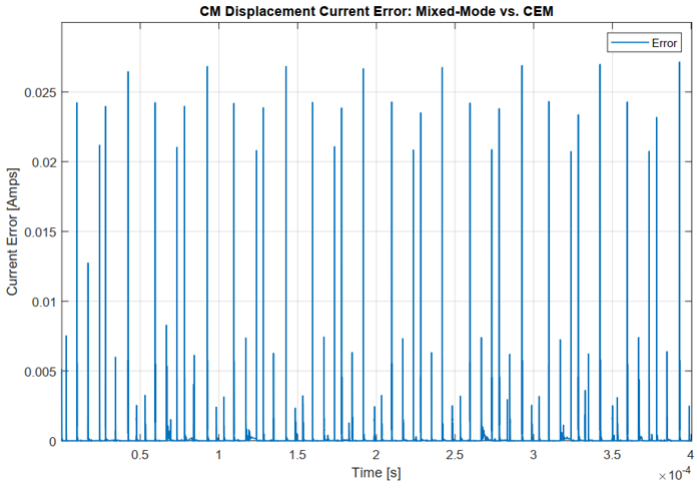


Figure 5-13: CM Validation Current Error: MM vs. CEM

The error is determined using the absolute value of the difference between both plots. We

are experiencing error in the range of tens of mA, which is an overall error of less than one percent. This error could be caused from a small delay or offset between both models, but without further insight we can not pin point the exact reason. With these results we have a very accurate modeling technique for predicting CM conducted emissions, justifying a validation for our CM equivalent model.

Effect of Neglecting DM Coupling in CM Model

In past modeling techniques, others have mentioned that the DM coupling term into the CM circuit is negligible and doesn't need to be added in the CM model for an accurate modeling of CM conducted current, which is often true for non-WBG devices or symmetrical systems. Effectively, they are saying all you need to accurately model the CM conducted current is the CM input voltages and the equivalent CM impedance, but we have learned that the asymmetric coupling factor plays a significant role in understanding conducted emissions. So lets go back to our CM model and remove the DM coupling terms and see the effect it has on our predicted CM displacement current.

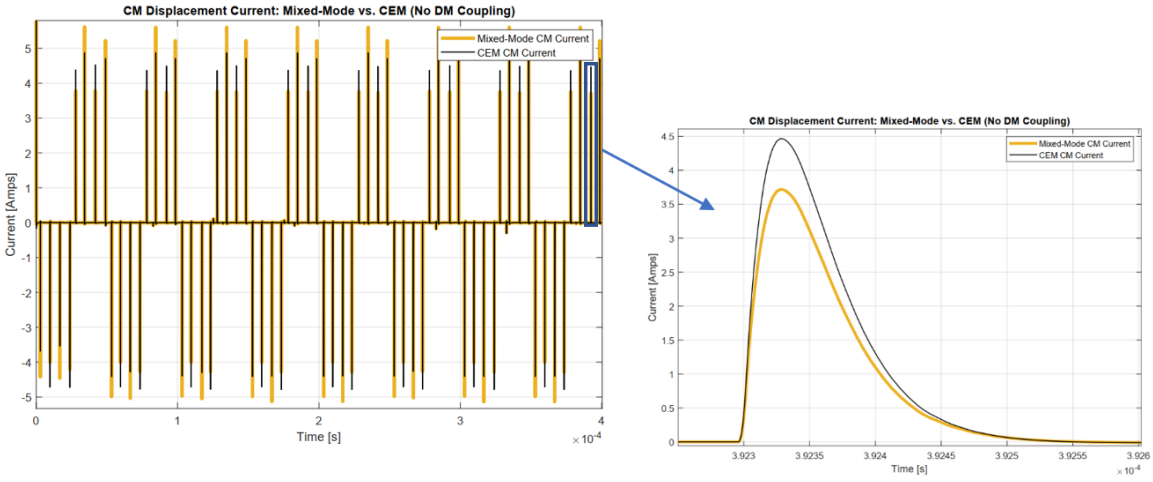


Figure 5-14: CM Currents: MM vs. CEM(No DM Coupling)

From these results I would say that this is a semi-accurate model, but is not as accurate as the CM model if you were to include the DM coupling. Maybe you could justify using this method if you want to save time or unaware of the mathematical modeling procedure used to compute the DM coupling. But there is still a significant amount of error involved

in not using the coupling term.

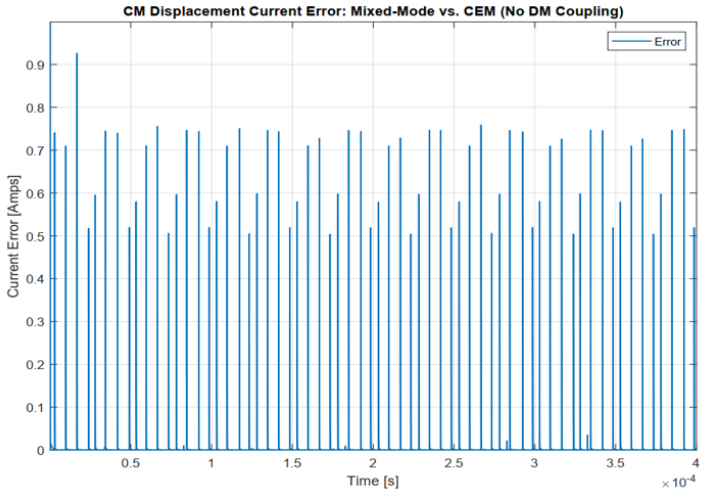


Figure 5-15: CM Validation Current Error: MM vs. CEM(No DM Coupling)

Without the use of the DM coupling terms we are experiencing error in the range of hundreds of mA, which is an overall error of upwards of twenty percent. This is a significant amount of error and really drives the point home that DM coupling is not negligible when trying to produce an accurate CM model to predict CM emissions.

Effective Use of CEM

With the validation of CM equivalent models, we should define effective use cases for them. Even though we used PLECS to simultaneously run both models together for validation, it doesn't make sense to do this apart from that because the MM model can do it on its own. But running a MM model can take a long time to run, which is why we initially created these CM equivalent models. We wanted to isolate the CM emissions by only extracting the dominant EMI sources and allow us to run these models without the use of a full system model.

So how do we efficiently use the CEMs after validation? There are two methods, method 1 is with the use of a hardware setup and method 2 is through the use of synthesized voltage sources. Method 1 will be conducted in a similar manner in which we use our MM model to validate the CM model, we will probe the hardware and input these voltages into the CM model and be able to predict the amount of CM emissions that our device is producing.

Method 2 will be used in the case that we don't have a hardware setup, instead we will gain insight on how the intended system will operate and we will then synthesize these voltage waveforms and plug them into our CM model for prediction of CM emissions. Both are valid use cases for predicting CM emissions without the build up of a simulation, saving us valuable time and providing an accurate method of predicting CM emissions for a given system.

5.2.3 Floating Heatsink vs. Nuetral Point Clamped Heatsink

CM current through the transistor baseplate can degrade power semiconductor module insulation, and by floating the heatsink we can limit the insulation stress on these devices. By keeping the heatsink floated we studied ways of changing the circuit layout, and more specifically, ways of connecting the heatsink to our topology to reduce the amount of CM emissions. Since we are dealing with NPC converters, where the converter is clamped to the neutral point, we wanted to know what happens if the heatsink is clamped to this neutral point as well. By doing this we found out that we can significantly decrease the amount of CM displacement current through the heatsink into the ground potential.

If we look back at our CM displacement current through the heatsink, shown in Figure 5-6, we saw that the displacement current was on the order amps. By tying the heatsink to the neutral point of the converter we discovered that there is a CM displacement current reduction down to the order of a fraction of milliamps. A plot of the displacement current implementing this technique can be seen in Figure 5-16. So by tying the neutral point of the converter to the heatsink we not only reduced the CM current but we significantly reduced the CM current by orders of magnitude. By doing this we are able to reduce a large portion of CM parasitic paths. Essentially, we eliminate all parasitic capacitors seen by the neutral point of the NPC modular layout, which makes up for about 25 percent of the total parasitic paths. With this study, it provides insight into how noisy the neutral point of the converter actually is. This justifies an in depth study into ways of providing more voltage balancing techniques and ways of limiting asymmetric currents flowing into the neutral point.

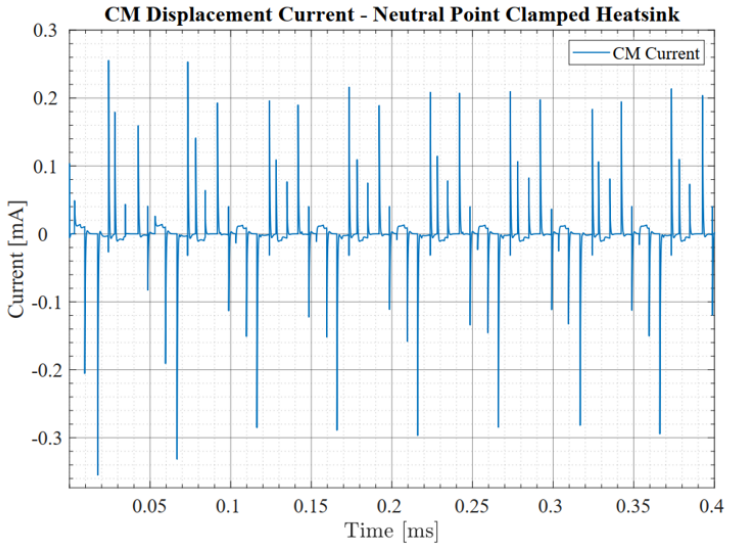


Figure 5-16: CM Displacement Current w/ Neutral Clamped Heatsink

Effect on the CM Equivalent Model

Previously we developed a CM equivalent model for a NPC full-bridge converter that did not have the neutral point tied to heatsink, for reference look at Figure 5-8. For that model we used P = N, but when we develop the new CM equivalent model for this scenario we can no longer use N as the arbitrary point. When tying N to the heatsink, it is no longer distinct from ground, so we chose the arbitrary point to be the lower rail of the DC link. The new constructed CM equivalent model using P = L, is constructed below

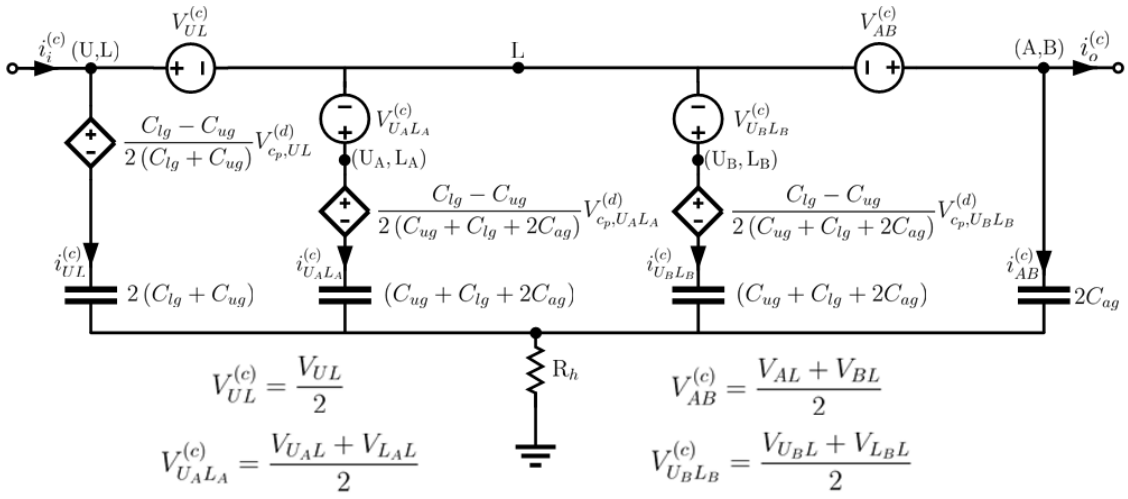


Figure 5-17: NPC Full-Bridge CEM w/ P = L, Neutral Clamped Heatsink

Comparing the two CM equivalent circuits we need to realize that our CM sources have changed a little based on the arbitrary point that is chosen. But more significantly we realize that mathematically we have reduced the total capacitance as well as significantly reducing the DM noise coupling term in the left most branch.

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Chapter 6

Conclusion

6.1 Summary

This section summarizes the work presented in this thesis. The goal was to provide a computationally efficient method of EMI characterization for conducted emissions for power electronic based power distribution systems, in particular the neutral point clamped dual active bridge. With EMI characterization we are able to provide quantified insights into many EMC design challenges. This quantification makes the design of EMI mitigation more efficient by reducing the scale and number of physical experiments, reducing simulation time, and reducing unnecessary design margins. By being able to quantify the EMI with light weight computation, the iteration process is manageable and allows the implementation of automated optimized algorithms.

To begin with, a literature review on current and state of the art major modeling methods for EMI characterization performed by academic scholars was covered. Three different modeling methods was covered; black-box, white-box, and gray-box modeling. The impacts on high-frequency accuracy and computational efficiency was covered for each model, where gray-box modeling was deemed best suited for its balance between analysis accuracy and simulation efficiency. Gray-box modeling establishes a mathematical equivalent circuit modeling technique where the dominate EMI sources are measured in hardware.

A systematic common-mode mathematical modeling method was proposed. The objective of the approach was to define a CM voltage with respect to an arbitrary reference

point which is distinct from ground. This floating point facilitates the transformation of mixed-mode systems into common-mode equivalent systems which are then systematically assembled to form common-mode equivalent models. The methodology for this procedure was thoroughly covered in great detail. A common-mode equivalent circuit for the neutral point clamped converter was derived, as well as an equivalent circuit for the medium-frequency transformer. Both of these provided a full common-mode equivalent circuit for neutral point clamped based dual active bridge.

To support the design methodology, a validation process was performed. To validate the common-mode model for the NPC DAB, a full system simulation for the mixed-mode circuit was developed using MATLAB Simulink with a PLECS blockset. The common-mode model of the NPC converter was then validated along side the mixed-mode model in simulation. The validation was a success and possible conducted emission mitigation efforts were simulated as well.

Electromagnetic compatibility testing was discussed for both radiated and conducted emissions, which will eventually be conducted on a hardware implementation of the NPC DAB.

6.2 Future Work

This section suggests direction for further development of the work presented in this thesis.

First, a prototype of the neutral point clamped converter based dual active bridge needs to be constructed and tested. With a lab hardware setup we will be able to continue the validation process of our common-mode equivalent models, primarily the medium-frequency transformer. A hardware implementation is key to the validation of the medium-frequency transformer since we were unable to model the CM conduction paths in simulation. A process will need to be set forth to make this possible, but looks promising with continued support and collaboration from like minded people in industry and academia.

Once hardware is implemented and the common-mode models are validated, there are many avenues we can take to continue the research for neutral point clamped converter based dual active bridges for electrical distribution systems.

One option is to conduct EMC testing, both radiated and conducted emissions, in our soon to be built anechoic chamber. These testing measurements can be compared to testing standards on the limits of emissions, if the measurements are under the limits we can move on. If our measurements are over the limits we can implement EMI mitigation tools, through filters or other means, to lower the amount of interference that our converter exhibits.

Another option is to extend this modeling procedure from the NPC DAB to much larger system applications for the prediction of CM emissions of these systems. The DAB is a sub module used in so many applications, and with the validation of the DAB it will be really easy to extend this process out to much larger distribution system applications. In the appendix, there are a few CM equivalent models for larger system applications that the NPC DAB can be extended to.

Another option is through the implementation of automated optimized algorithms for the design of power electronic converters. The Virtual Prototype Process (VPP) is an application of this automated optimization process that is already being performed by our research team, but one of the missing links is the EMI characterization. So, there is potential for us to enhance the VPP with one more optimization constraint using these computationally efficient methods of CM modeling.

Honestly, this is only the beginning, there are so many options we can take with these computationally efficient methods of CM modeling. This is just one stepping stone for a long line of research to come. It is truly exciting to be apart of this journey.

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Appendix

A.1 NPC to 2-Level Full-Bridge DAB

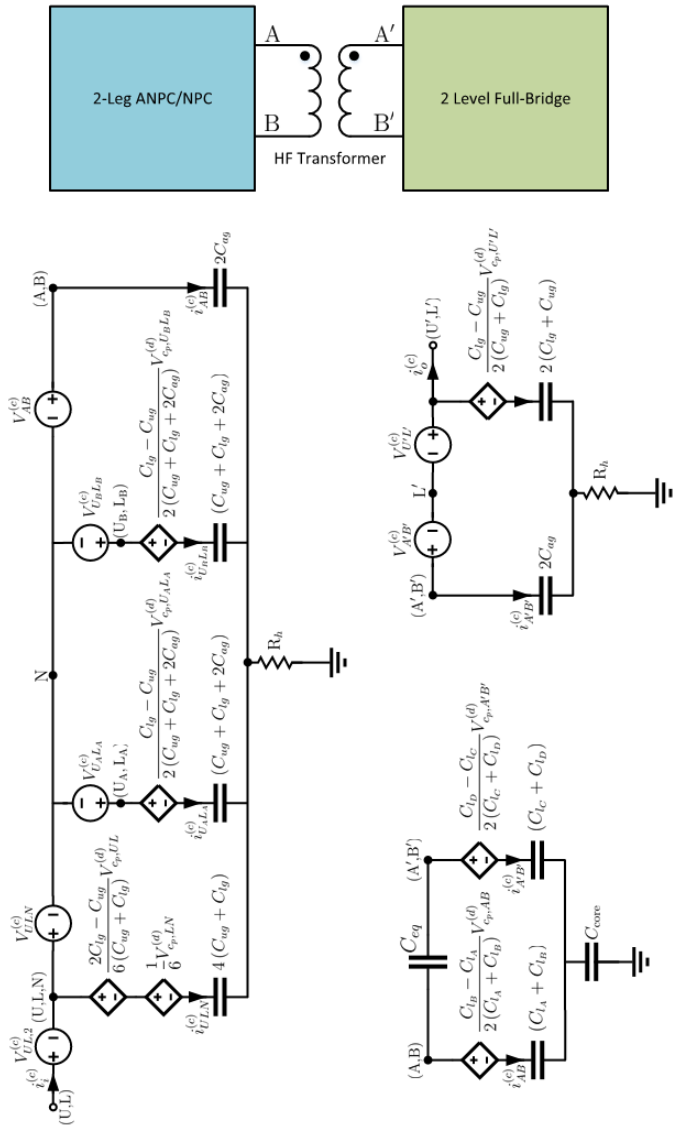

Figure A-1: NPC to Full-Bridge DAB CEM

A.2 AC to AC Converter using 3-Leg ANPC/NPC

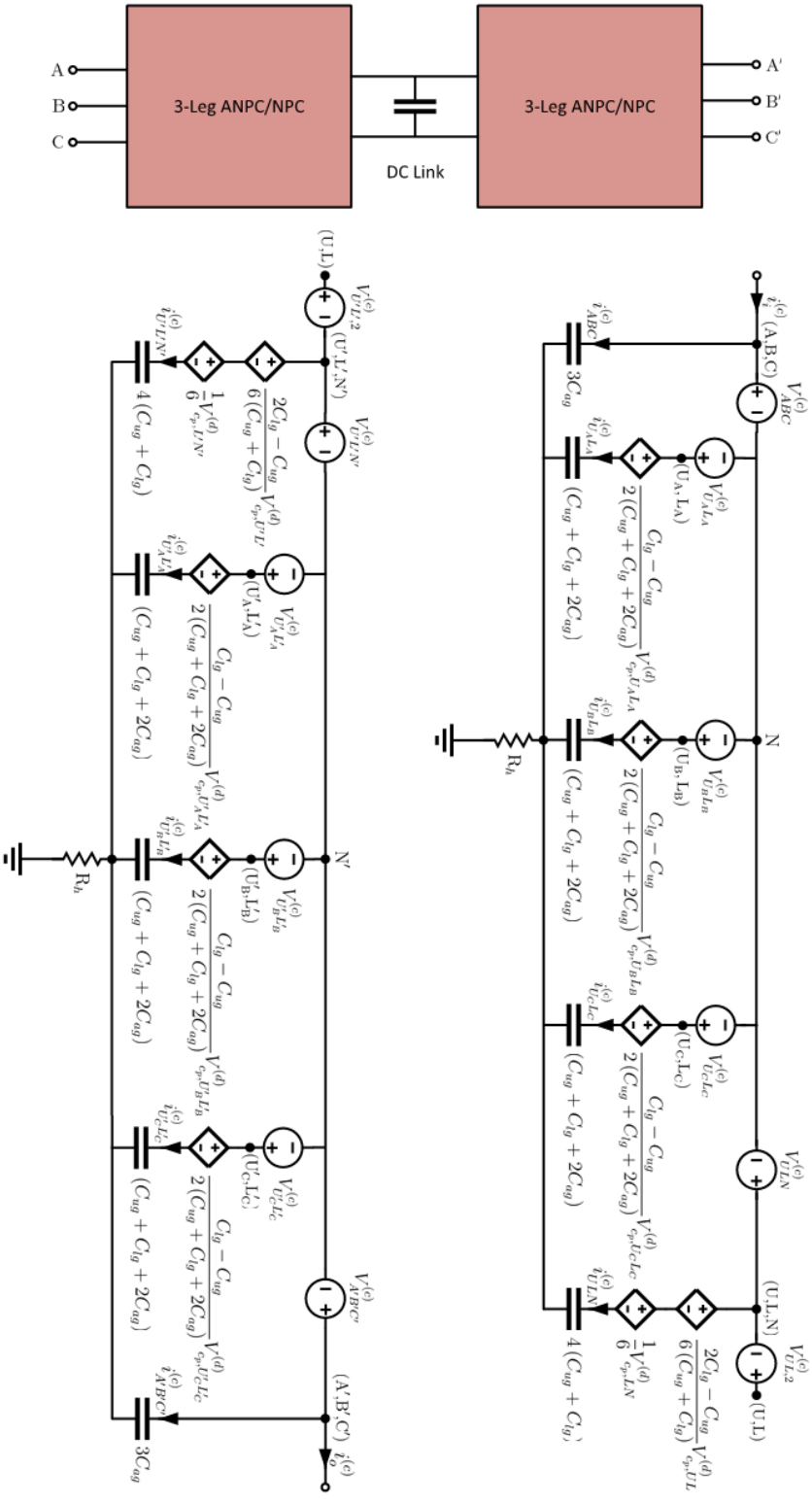

Figure A-2: AC/AC Converter using NPC CEM

A.3 AC to DC Isolated Converter

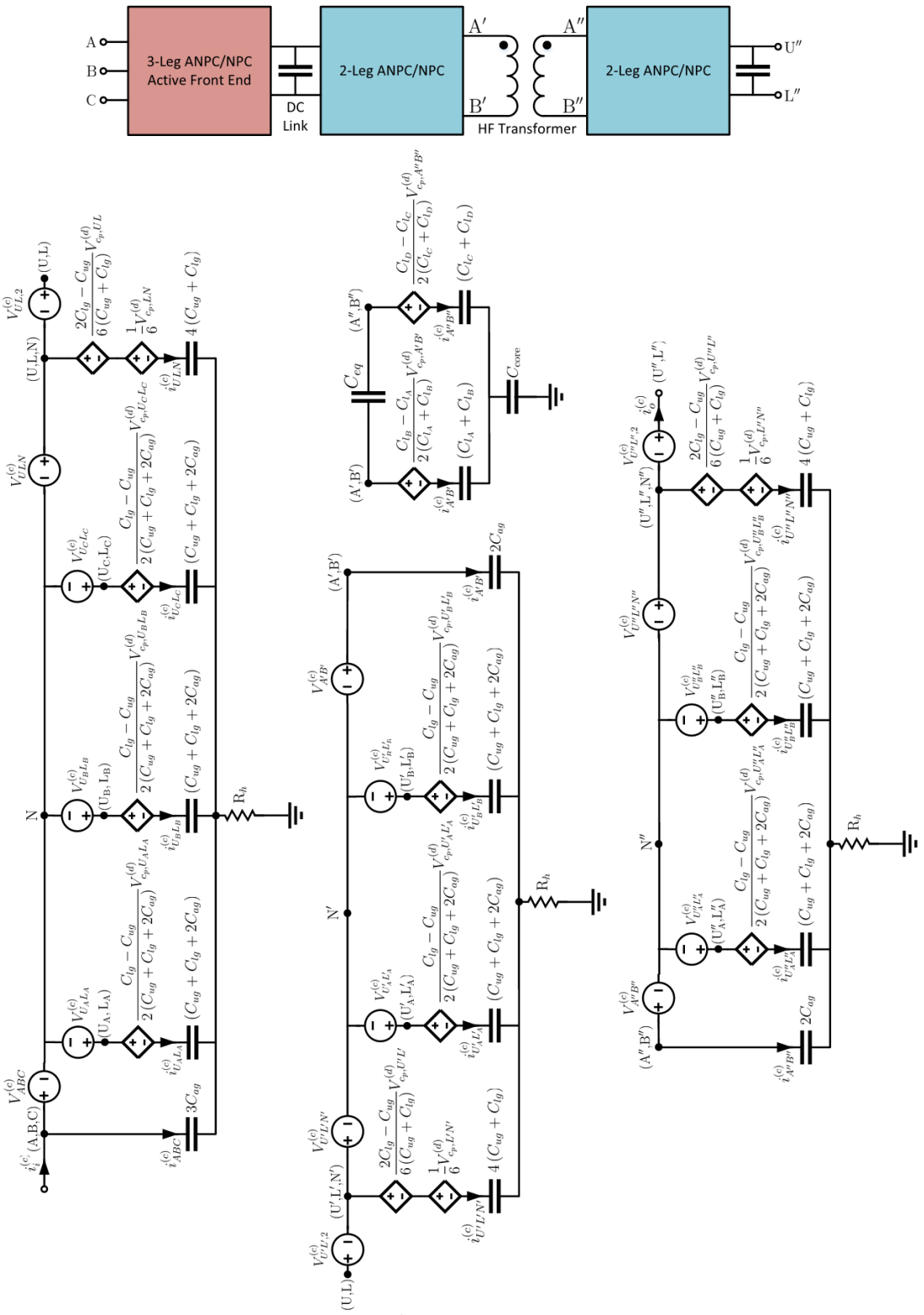

Figure A-3: AC/DC Isolated Converter CEM