Design Considerations and Topology Selection for a 120-kW IGBT Converter for EV Fast Charging

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***Abstract*— Fast charging of electric vehicles (EV's) is a very desirable feature, especially for long-distance travel. For an EV with a battery capacity of 30 kWh, a 15-min charge requires 120-kW charging power. Inductive charging offers a safe and convenient means to accomplish this task. This paper investigates the design criteria of the high-power converter for a 120-kW inductive battery charger. Since insulated gate bipolar transistors (IGBT's) are the devices of choice at this power level, the impact of IGBT losses on the converter design and topology selection is investigated. A comparison between a zero-voltage-switching (ZVS) and zero-current-switching (ZCS) series-resonant converter (SRC) is presented. Based on the comparison results, a ZCS SRC topology is selected for this application, and an experimental 120-kW/75-kHz unit was built and tested in the laboratory to verify the results.**

***Index Terms*— Electric vehicle charging, series-resonant converters, zero-current switching, zero-voltage switching.**

I. Introduction

HIGH-POWER charging is desirable if electric vehicles (EV's) are to be used for long distances. In this case, it is required that battery charging be accomplished in minutes rather than hours. For a battery capacity of 30 kWh, a 15-min charge would require a charging power of 120 kW. For an EV battery voltage of 200–400 Vdc, this corresponds to 300 A at the upper end of the expected battery voltage range.

Inductive charging technology offers a safe and convenient means to accomplish this task, where magnetic induction is used as the interface for energy transfer [1]. No exposed conductors exist which gives a safety advantage over conductive schemes. In addition, the scalability of the interface to high power levels and frequencies fulfills the universal interface requirement, where the same charger port can be used to interface chargers of different ratings and manufacturers.

This paper will examine the converter topology selection, design, and testing at the proposed power level. A major factor in selecting a converter topology is the total loss of the semiconductor switching devices. Since insulated gate bipolar transistors (IGBT's) are the most suitable devices to be used at this power level, a complete characterization of these devices is needed before a final decision is made. Based on the obtained results, a zero-current-switching series-resonant-converter (ZCS SRC) topology was found to be most suitable for this application.

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II. Design Criteria

The main design criteria for the high-power charging converter are first discussed. These criteria are meant to provide selection guidelines for a suitable converter topology.

A. Current-Source High-Frequency Link

The high-frequency transformer link should be current rather than voltage stiff. The current-source link results in a rectifier, which is followed by a capacitive input filter, and, hence, no overvoltage clamping is required for the secondary diodes. This arrangement is less sensitive to the converter operating frequency and power level.

B. Soft Switching for the Main Devices

The converter frequency must be kept as high as possible to minimize the coupling transformer size and on-board filter components. A 75-kHz operating frequency has been proposed for this work. As soft switching allows higher operating frequencies, it becomes a prerequisite.

C. Fixed Operating Frequency

The magnetic design of the transformer can be best optimized if the operating frequency is fixed. However, in order to accommodate load variations, the frequency may be varied. In this case, it is better that higher frequency operation results at part load so as to keep the converter switching loss relatively constant over the switching frequency range and provide full utilization of the magnetic core.

D. Operating Over Wide Load Range

The converter should be capable of operating safely over a wide range of load conditions including open and short circuit. A lead acid battery normally will present a much narrower load

range. It is desirable that the converter be able to operate with a totally discharged battery.

III. Converter Topology Selection

Since the output rectifier should be current sourced, only topologies which connect a significant inductance in series with the transformer primary are considered. These include the single active-bridge (SAB) converters and resonant converters with the transformer in series with the resonant inductor. The SAB has significantly higher peak currents compared with traditional resonant converters [3]. An SRC can be considered as an SAB with a large inductance. The resonant capacitor corrects the converter regulation by canceling the inductor voltage drop. Resonant converters are preferred as a slower grade of rectifier diode can always be used.

Several series resonant topologies have been reported in the literature. These topologies are categorized as either current or voltage fed.

A. Current-Fed Topologies

In these topologies, the converter is fed by a current source. Hence, the device current is well defined, but no limitation on the switch voltage is provided, which is a disadvantage of these topologies since IGBT's have more tolerance to overcurrent than overvoltage. Most of the current-fed converters use reverse-blocking-controlled switches.

B. Voltage-Fed Topologies

In these topologies, the converter is fed by a voltage source. As a result, the device voltage is well defined, but the device can be damaged by a shoot-through fault. These converters are normally classified as series, parallel, or series-parallel resonant types [3]–[5]. The SRC connects the transformer primary in series with the resonant inductor and is the only converter that has a current stiff link.

A disadvantage of the SRC is that output voltage regulation is difficult. The output voltage can be controlled in a number of ways, which include control of the converter frequency, pulse-width modulation (PWM), and combining the outputs of two phase-shifted half-bridge converters. Frequency variation is undesirable since the optimization of the transformer is affected and the converter control complicated. Phase-shift control or PWM may be considered. However, soft switching is normally lost on one of the inverter legs.

IV. Insulated Gate Bipolar Transistor Characterization Under Soft-Switching Conditions

Since power devices are still far from being ideal switches, their switching behavior will directly affect the performance of the converter topology being used. Although a spectrum of zero-voltage-switching (ZVS) and ZCS topologies have been reported in the literature, only a limited number of these topologies will work with a certain power device given the device switching characteristics. IGBT's with relatively low conduction loss and high-frequency capability are increasingly

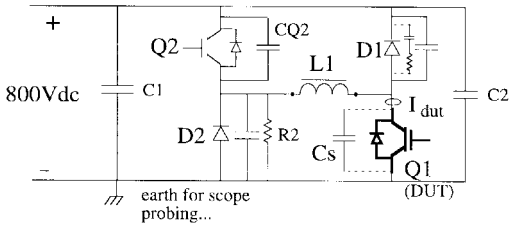


Fig. 1. An IGBT test circuit.

the preferred choice for high-power and high-frequency applications. Yet, their switching losses remain a limiting factor in many converter topologies. Kurnia *et al.* [6], [7] characterized the different loss mechanisms in IGBT's such as the di/dt dependent conduction loss due to conductivity modulation lag and the turn-off tail-current bump with capacitive snubbers. These results show clearly that care should be taken when using IGBT's in ZVS topologies since the turn-off losses could be quite high, especially at high ambient temperatures.

In this section, a complete IGBT characterization under ZVS will be presented. The specification for the dc-bus voltage has been selected to be 800 Vdc to interface a 2:1 inductive coupler turns ratio. Note that the upper limit of the battery voltage is 400 Vdc. Based on the dc-bus-voltage specification, a 1200-V IGBT device can be selected. Since the output battery current is 300 A at the upper limit, a 400-A device rating is selected. Hence, a Powerex CM400HA-24H (1200 V/400 A) and a CM600HA-24H (1200 V/600 A) were selected and completely characterized. Both devices are punchthrough IGBT's.

The test circuit used for loss characterization is shown in Fig. 1. In this figure, $Q1$ is the IGBT under test while $Q2$ is a 1200-V/400-A Powerex IGBT. Both ZVS turn off and turn on in addition to hard-switching losses can be measured using this setup. A hot plate was used to heat up the device case to 125 °C. The circuit operation under turn-off and turn-on conditions is as follows.

A. Turn-Off Test

Both $Q1$ and $Q2$ are turned on and off simultaneously. The inductance value $L1$ and/or the on time of the devices can be varied to vary the turn-off current. The pull-down resistance $R2$ is used to reset the voltage across $Q1$ to zero before the device is turned on again. The value of C_s is varied to test the device under different dv/dt conditions. Typical voltage and current waveforms are shown in Fig. 2(a).

B. Turn-On Test

In this mode, $Q1$ is kept on all the time while $Q2$ is turned on and off. The inductance value L_l and/or the dc-bus voltage can be varied to control the di/dt of the device current. Typical voltage and current waveforms are shown in Fig. 2(b).

The selected IGBT's were thoroughly tested. Both hard-switching (HS) and ZVS-switching tests were performed at 25 and 125 °C. In addition, the device internal package inductances, on-voltage drop, and di/dt dependent conduction drop were all measured. The measured turn-off losses for the 1200-V/400-A IGBT under HS and ZVS with a 200-nF

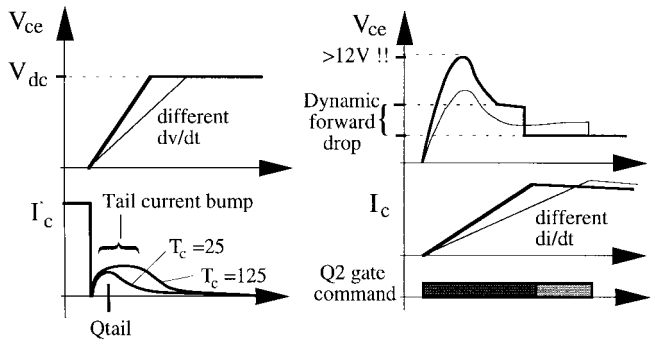


Fig. 2. The IGBT turn-off (a) and turn-on dynamics (b).

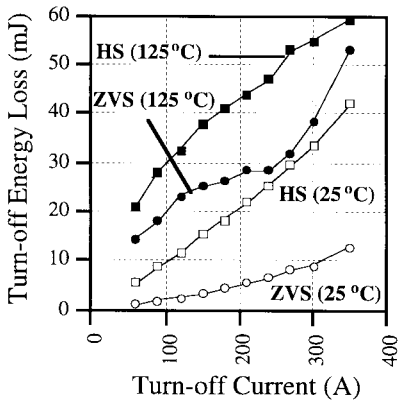


Fig. 3. Measured HS and ZVS ($C_s = 200$ nF) turn-off losses for the 1200-V/400-A IGBT.

snubber capacitor are shown in Fig. 3. As shown in Fig. 3, under ZVS, the turn-off losses at 25 °C can be lower than HS losses by nearly a factor of four (lower two curves). In reality, the actual die temperature is likely to be closer to 125 °C. Hence, the improvement factor with ZVS is limited to 1.5. This will limit the use of IGBT's in ZVS applications.

Based on the experimental results, two turn-off loss mechanisms for IGBT's can be identified. The first is associated with the tail current under HS conditions and with current-tail bump under ZVS conditions $E_{\text{off(tail)}}$. The second turn-off loss mechanism encountered is due to energy trapped in the device internal inductance $E_{\text{off}(L_{\text{int}})}$. Hence

$$E_{\text{off(total)}} = E_{\text{off(tail)}} + E_{\text{off}(L_{\text{int}})}. \tag{1}$$

The turn-off energy loss due to the device internal package inductance can be computed via

$$E_{\text{off}(L_{\text{int}})} = \tfrac{1}{2} L_{\text{int}} I_c^2. \tag{2}$$

The device internal inductance L_{int} is determined by measuring both the package and Kelvin lead voltages as shown in Fig. 4. The emitter terminal internal inductance is found using

$$L_{E\_\text{int}} = \frac{V_{ce\_ex} - V_{ce\_k}}{di/dt}. \tag{3}$$

The collector terminal internal inductance is normally the same as the emitter terminal. Note here that the energy dissipated in the internal package inductance is calculated as a function of

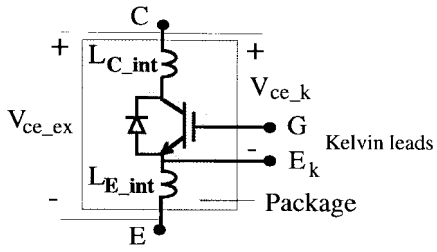


Fig. 4. Measuring the device internal inductance.

the collector current once the value of the package inductance L_{int} is determined. Hence, the tail-current turn-off losses are calculated via

$$E_{\text{off(tail)}} = E_{\text{off(total)}} - E_{\text{off}(L_{\text{int}})}. \tag{4}$$

A curve-fitting approach can be used to estimate tail-current turn-off loss given by (4). For a given value of snubber capacitance, the turn-off energy loss due to tail current is given by

$$E_{\text{off(tail)}} = k_o + k_1 I_c + k_2 I_c^2 \quad (\text{mJ}) \tag{5}$$

where I_c is the device current and k_o, k_1, and k_2 are the constant coefficients resulting from the second-order polynomial curve-fitted equations. Finally, the total average turn-off power loss is given by

$$P_{\text{off}} = f_s E_{\text{off(tail)}} + f_s E_{\text{off}(L_{\text{int}})} \tag{6}$$

where f_s is the switching frequency.

During turn on, a dynamic saturation voltage spike V_{sp} results, which varies with the impressed di/dt condition [Fig. 2(b)]. The dynamic saturation voltage spike is negligible at elevated temperatures. If a snubber capacitor C_s is placed across the device to insure ZVS, energy is stored in the snubber capacitor due to the resultant voltage spike, which is then dissipated within the device. The resultant turn-on energy loss under ZVS conditions is given by

$$E_{\text{on(ZVS)}} = \tfrac{1}{2} C_s V_{sp}^2 \quad (\text{J}). \tag{7}$$

On the other hand, if the device is turned on under ZCS condition, the energy stored in the device output capacitance is dissipated within the device. Hence, turn-on energy loss under ZCS conditions is given by

$$E_{\text{on(ZCS)}} = \tfrac{1}{2} C_{ce} V_{sp}^2 \quad (\text{J}) \tag{8}$$

where C_{ce} is the device output capacitance at V_{sp}. Note here that the device output capacitance is a function of the device voltage as given in the manufacturer's data sheets. As a result, the total average turn-on power loss is given by

$$P_{\text{on}} = f_s E_{\text{on}}. \tag{9}$$

With the IGBT conducting, it has been observed that under di/dt conditions, the device on-voltage drop is higher than the dc values and contribute substantially to the total conduction loss within the device. It can be seen that the voltage drop across the device increases as the applied di/dt increases, which may be due to the internal device stray inductance.

TABLE I
MEASURED DEVICES' DATA

	1200V/400A IGBT		1200V/600A IGBT	
Peak on-voltage drop	2.65 V @ 400 A		2.3 V @ 400 A	
Total package inductance	26.0 nH		41.0 nH	
di/dt effective inductance	12 nH max		15 nH max	
Turn off loss coefficients	HS	C_S =200nF	HS	C_S =200nF
k_2	1.45 x 10^{-3}	1.09 x 10^{-4}	8.36 x 10^{-5}	1.17 x 10^{-4}
k_1	0.135	0.054	0.215	0.108
k_o	-0.365	-0.311	1.35	-0.453

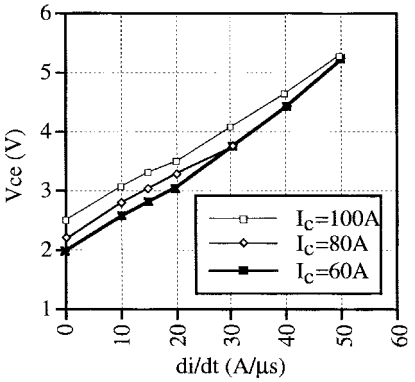


Fig. 5. Measured device on drop as a function of di/dt for the 1200-V/400-A IGBT.

However, it has been verified that the measured internal inductance does not account totally for the measured voltage levels. This suggests that an additional on-voltage drop across the device is induced, which is a function of di/dt and is given by

$$V_{ce} = V_{ce(\mathrm{dc})} + L_{\mathrm{eq}} di/dt \tag{10}$$

$$L_{\mathrm{eq}} = L_{\mathrm{int}} + L_{di/dt}. \tag{11}$$

Note here that the di/dt effective inductance contributes to the overall conduction loss within the device. During the turn-on test, the di/dt is varied and the device terminal voltage is measured (Fig. 5). The dc on-voltage drop is given in the manufacturer's data sheets. In addition, once the device internal inductance is measured, the di/dt effective inductance is given by

$$L_{di/dt} = \frac{V_{ce(\mathrm{measured})} - V_{ce(\mathrm{data\,sheets})}}{di/dt} - L_{\mathrm{int}}. \tag{12}$$

The total conduction loss within the device is computed via

$$P_c = (V_{ce(\mathrm{dc})} + L_{di/dt} \cdot di/dt) \cdot I_c. \tag{13}$$

A summary of the IGBT maximum forward drop, curve-fitted turn-off constant coefficients, di/dt effective inductance, and measured package inductance are listed in Table I. As shown in this table, the 600-A device has lower on-voltage drop and, hence, lower conduction losses. However, the turn-off losses of the 600-A IGBT are higher compared with the 400-A device. In addition, the turn-off and turn-on delay times are also higher. As a result, the 1200-V/400-A IGBT was selected for this application.

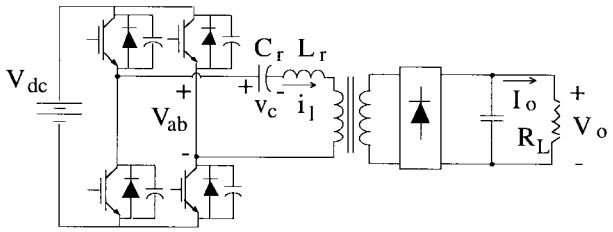


Fig. 6. The ZVS SRC.

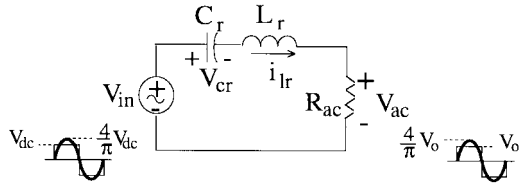


Fig. 7. Fundamental mode equivalent circuit of the ZVS SRC.

V. FIXED-FREQUENCY SRC

The SRC meets all of the earlier defined design criteria. Both ZVS and ZCS schemes will be investigated. A final comparison is then made.

A. The ZVS SRC

The SRC topology meets all of the earlier preset design criteria. As mentioned earlier, the maximum dc-bus voltage in this application is 800 Vdc. This is compatible with a 440/600-Vac source and the readily available 1200-V IGBT devices. The circuit diagram of this topology is shown in Fig. 6. When this converter is switched above the resonant frequency, a lagging load current is drawn from the inverter, which enables soft switching by the use of snubber capacitors across the IGBT's.

In analyzing this converter, four distinct linear circuit modes can be identified during a switching cycle. The circuit equations in each circuit mode along with the boundary conditions can be used to compute the different circuit variables and the

TABLE II
DESIGN DATA FOR THE ZVS SRC

	$\omega_n = 1.1$	$\omega_n = 1.2$
V_{no}	0.97 pu	0.91 pu
$I_{nl,pk}$	0.8 pu	0.74 pu
$V_{nc,pk}$	1.2 pu	1.2 pu
I_{noff}	0.16 pu	0.245 pu
IGBT Losses (@ 75 kHz)	1190 W	1350 W
R_{sa}	0.002 (°C/W)	< 0 (°C/W)

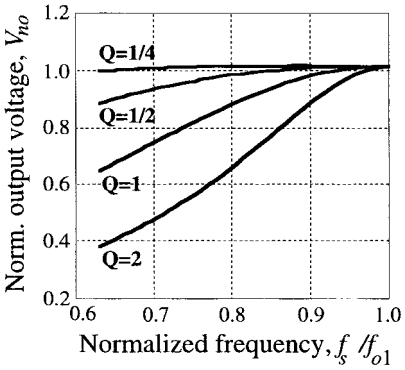


Fig. 8. Normalized voltage gain for the ZVS SRC.

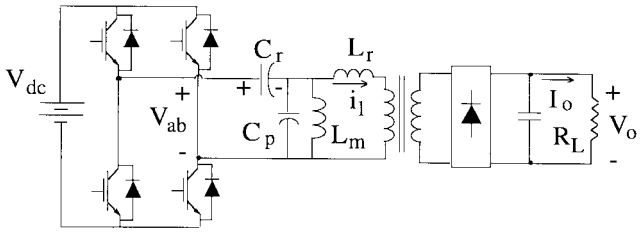


Fig. 9. The ZCS SRC.

voltage gain of the converter. A fundamental mode analysis, however, provides a simplified approach. The error due to this approximation is very small when the switching frequency is higher than the resonant frequency. The fundamental mode equivalent circuit is shown in Fig. 7. Note here that the reflected ac resistance R_{ac} can be computed as

$$R_{\text{ac}} = \frac{8}{\pi^2} R_L. \tag{14}$$

Using ordinary circuit analysis, the ac voltage gain $V_{\text{ac}}/V_{\text{in}}$, which is the same as the dc-voltage gain V_o/V_{dc}, can be computed as

$$V_{no} = \frac{V_{\text{ac}}}{V_{\text{in}}} \frac{1}{\sqrt{1 + \left[\frac{\pi^2}{8} Q\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)\right]^2}} \tag{15}$$

where $Q = \omega_0 L_r / R_L$ is the load quality factor and $\omega_0 = 1/\sqrt{L_r C_r}$ is the tank resonant frequency. The rest of the circuit variables can be computed in a similar way.

The resultant normalized design curves for the ZVS SRC are shown in Fig. 8. Note here that the circuit voltages and currents were normalized with respect to the dc-bus voltage and the dc-output current, respectively. By investigating Fig. 8, a high Q results in better control of the output voltage and lower peak resonant current. This is due to the fact that a high Q means that the link energy is higher. As a result, the peak resonant current may take several cycles to change appreciably. This simplifies the overcurrent protection and current-regulation schemes. The disadvantages of a high Q are the high resonant-capacitor voltage and higher resonant circuit losses. This would complicate the capacitor selection and construction.

Finally, the IGBT losses, which are the main losses, need to be computed for this converter topology. The resultant test data of the 1200-V/400-A IGBT characterization, presented in the previous section, will be used in this analysis. Using the measured device data, the IGBT losses can be computed as a function of the normalized switching frequency $(\omega_n = f_s/f_o)$ and the load quality factor Q. In addition, the thermal resistance of the heat sink (R_{sa}) needed to mount these devices is also computed. The projected converter design data and the resultant IGBT losses are shown in Table II, where V_{no} is the normalized output voltage gain, $I_{nl,pk}$ is the normalized peak resonant-inductor current, $V_{nc,pk}$ is the normalized peak resonant-capacitor voltage, and $I_{n\text{off}}$ is the normalized IGBT turn-off current. These variables were normalized with respect to the following base values:

$$V_{\text{base}} = V_{\text{dc}} \tag{16}$$

$$Z_{\text{base}} = Z_0 = \sqrt{L_r/C_r} \tag{17}$$

$$I_{\text{base}} = V_{\text{dc}}/Z_0. \tag{18}$$

The data in Table II were calculated for a 120-kW converter rating with 800-Vdc-bus voltage, 75-kHz switching frequency, 94 nF of snubber capacitance, and a load quality factor of 1.0.

As shown in Table II, the computed IGBT losses at an $\omega_n = 1.1$ are 1190 W, and the required heat-sink thermal resistance is 0.002 °C/W. This represents a high-loss figure, and an extremely good liquid-cooled heat sink is needed.

B. The ZCS SRC

Another variation of the SRC is the ZCS SRC shown in Fig. 9 [8]. This converter topology also meets all of the earlier defined design criteria. Again, the maximum dc-bus voltage in this application is 800 Vdc, which is compatible with a

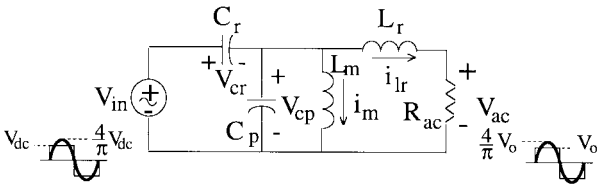


Fig. 10. Fundamental mode equivalent circuit of the ZCS SRC.

440/480-Vac source and the readily available 1200-V IGBT devices. The main difference between the ZVS SRC and the ZCS SRC is the presence of an additional parallel resonant circuit (C_p and L_m) as shown in Fig. 9. The inductance L_m could be the magnetizing inductance of the transformer.

If the circuit is switched below resonance, the IGBT's are turned on and off under nearly ZCS. In fact, the device is turned off with the magnetizing current flowing in it. However, the magnetizing current is rather small, due to the relatively large value of L_m, and the hard-switched turn-off losses at this current level are small as well. Hence, no snubber capacitance is needed.

By using the fundamental mode analysis and utilizing the same terminal relationships for input and output voltages as in the ZVS SRC, the fundamental equivalent circuit can be obtained and is shown in Fig. 10. Using ordinary circuit analysis, the ac voltage gain $V_{\rm ac}/V_{\rm in}$ can be computed as

$$V_{no} = \frac{V_{\rm ac}}{V_{\rm in}} = \left\{ \left[1 + \left(\frac{\omega_{o2}}{\omega_{o3}}\right)^2 - \left(\frac{\omega_{o2}}{\omega}\right)^2 \right]^2 + \left(\frac{\pi^2}{8} Q \left(\frac{\omega}{\omega_{01}} \right) \right)^2 \cdot \left[1 + \left(\frac{\omega_{o2}}{\omega_{o3}}\right)^2 - \left(\frac{\omega_{o2}}{\omega}\right)^2 - \left(\frac{\omega_{o1}}{\omega}\right)^2 \right]^2 \right\}^{-1/2} \tag{19}$$

where

$$Q = \omega_{o1} L_r / R_L$$

$$\omega_{o1} = 1/\sqrt{L_r C_r}$$

$$\omega_{o2} = 1/\sqrt{L_m C_r}$$

$$\omega_{o3} = 1/\sqrt{L_m C_p}$$

$$\omega_{o4} = 1/\sqrt{L_r C_p}.$$

In this topology, the ratio of the magnetizing inductance to the series inductance (L_m/L_r) is normally high. Hence, the coupling transformer magnetizing inductance can be used, and no additional inductance is needed. On the other hand, the ratio of the series resonant capacitance and the parallel capacitance (C_r/C_p) is also high, in the order of 100's. Hence, only a small capacitor is needed in this application.

The resultant normalized design curves as a function of the normalized switching frequency $(\omega_n = f_s/f_{o1})$ and the load quality factor Q are shown in Fig. 11. By inspecting Fig. 11, a high Q results in better control of the output voltage and lower peak resonant current. This is similar to the ZVS SRC case, and it is due to the fact that a high Q results in a higher link energy. The disadvantages of high Q are the high resonant-capacitor voltages and higher resonant circuit losses.

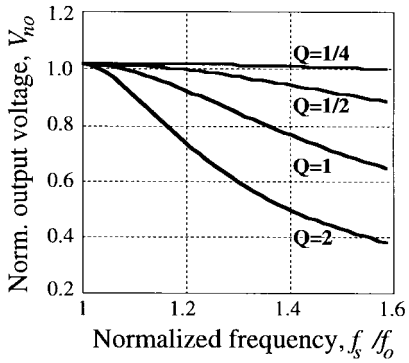


Fig. 11. Normalized voltage gain for the ZCS SRC.

The IGBT losses, which are the main losses, can be computed for this converter topology as well. The measured device data (1200-V/400-A IGBT) under turn-on and turn-off conditions will be used for this calculation. The projected converter design data, computed IGBT losses, and thermal resistance of the heat sink needed to mount these devices are shown in Table III, where $V_{ncr,pk}$ is the normalized peak-series resonant-capacitor voltage and $V_{ncp,pk}$ is the normalized peak-parallel resonant-capacitor voltage. The base values are the same as given by (16)–(18). These data were calculated for a 120-kW converter rating with 800-Vdc-bus voltage, 75-kHz switching frequency, and a load quality factor of 0.5. As shown in Table III, the computed IGBT losses at an $\omega_n = 0.83$ are 590 W, and the required heat-sink thermal resistance is 0.024 °C/W. This can be achieved by a good forced-cooled heat sink (like an AAVID 0.02 °C/W heat sink).

C. Final Topology Selection

In this section, a comparison will be made between the ZVS and the ZCS SRC based on the previous analysis to select a final topology.

Both the ZVS and the ZCS SRC's are voltage-fed topologies. In the ZVS SRC, two resonant components are needed while four are needed in the ZCS SRC. However, since the ratio of the parallel tank impedance to the series tank impedance is quite high, a small parallel capacitor is needed in the ZCS SRC, and the transformer magnetizing inductance can be used as a resonant component.

As discussed earlier, the impact of IGBT losses on the converter selection can be quite significant. In order to investigate their impact on the ZVS and ZCS SRC's, the IGBT loss breakdown for both converters is shown in Table IV. These data were calculated using the IGBT loss equations developed earlier in Section IV. As shown in Table IV, the main loss component in the ZVS SRC is the turn-off loss, which seems to be high and could be as high as 1.5 kW per device (@ 150-

TABLE III
DESIGN DATA FOR THE ZCS SRC

	$\omega_n = 0.83$	$\omega_n = 0.77$
V_{no}	0.995 pu	0.972 pu
$I_{nl,pk}$	0.973 pu	1.033 pu
$V_{ncr,pk}$	0.95 pu	1.0 pu
$V_{ncp,pk}$	1.95 pu	2.0 pu
IGBT Loss (@ 75kHz)	590 W	600 W
R_{sa}	0.026 (^{O}C/W)	0.024 (^{O}C/W)

TABLE IV
INSULATED GATE BIPOLAR TRANSISTOR LOSS BREAKDOWN FOR THE ZVS AND ZCS SRC'S

Loss component	ZVS SRC $\omega_n = 1.2$	ZCS SRC $\omega_n = 0.77$
Conduction loss	150 W	220 W
di/dt dependent loss	60 W	98 W
Turn-off loss	950 W	219.7 W
Package inductance turn-off loss	23 W	0.3 W
Turn-on loss	0.2 W	52 W
Total	1190 W	590 W

A 94-nF snubber capacitance). Hence, the ZCS SRC seems to be a more reasonable topology because of the much lower IGBT losses.

VI. EXPERIMENTAL IMPLEMENTATION

A high-power converter topology, suitable for fast charging of EV's, was selected. The proposed topology is a ZCS SRC. The impact of the IGBT losses under soft-switching conditions was incorporated in the design process to yield an optimized design.

For this implementation, power circulation was employed to test the experimental unit since the converter rating is somewhat higher than the existing lab supply. Since the converter will be used to test the existing 8:4 inductive coupler built at GM Hughes, a 1:2 transformer is needed to boost the voltage back to the dc-bus-voltage level (800 Vdc in this case). In addition, a second transformer which increases the converter output voltage sufficiently to overcome the converter regulation is needed. The adjusting transformer can be small as an auto transformer connection is allowable. A block diagram of the proposed experimental system is shown in Fig. 12. Note here that the dc-bus voltage is made variable for testing purposes only. Practically, the dc-bus voltage is either fixed, in which case output voltage control can be done using phase-shift control or PWM control or varied using another preregulator input stage such as a buck or boost converter.

With power circulation, the load current is determined by the resistive elements' voltage drop along the current path. Hence, a means to control the load current and operate at the specified power level is needed. Since fixed-frequency operation is required, a 1-kW adjustable resistive load can be serially connected just before recirculation back to the dc-bus

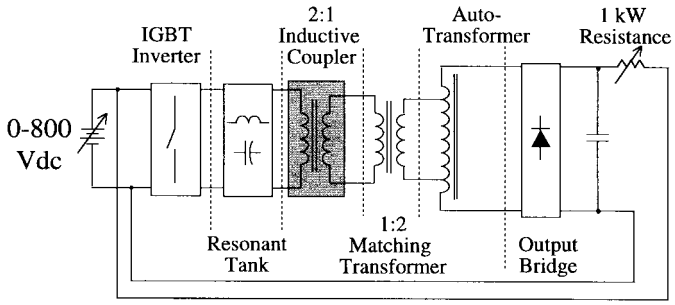


Fig. 12. Experimental system implementation.

voltage. This will control the resistance in the current path and, hence, control the load current.

The circuit was first simulated with SABER, and the resulting simulation results with power recirculation are shown in Fig. 13.

The full-bridge stage is designed to operate below the resonant frequency in order to insure ZCS. At 70-kHz switching frequency, the resultant resonant frequency is 105 kHz for a normalized frequency ratio (ω_n) of 0.67. Such a low ratio is necessary to insure that there is enough time to commutate the IGBT's of the same leg and prevent any shoot-through condition.

The maximum converter bus voltage for this implementation has been selected to be 800 Vdc. The selected switching devices were POWEREX 1200-V/400-A (CM400HA-24H) IGBT's. The secondary diode bridge was implemented using the antiparallel diodes of 1200-V/200-A FUJI (1MBI200L-120) IGBT modules. These are fast-recovery diodes with a transit time of 250 ns.

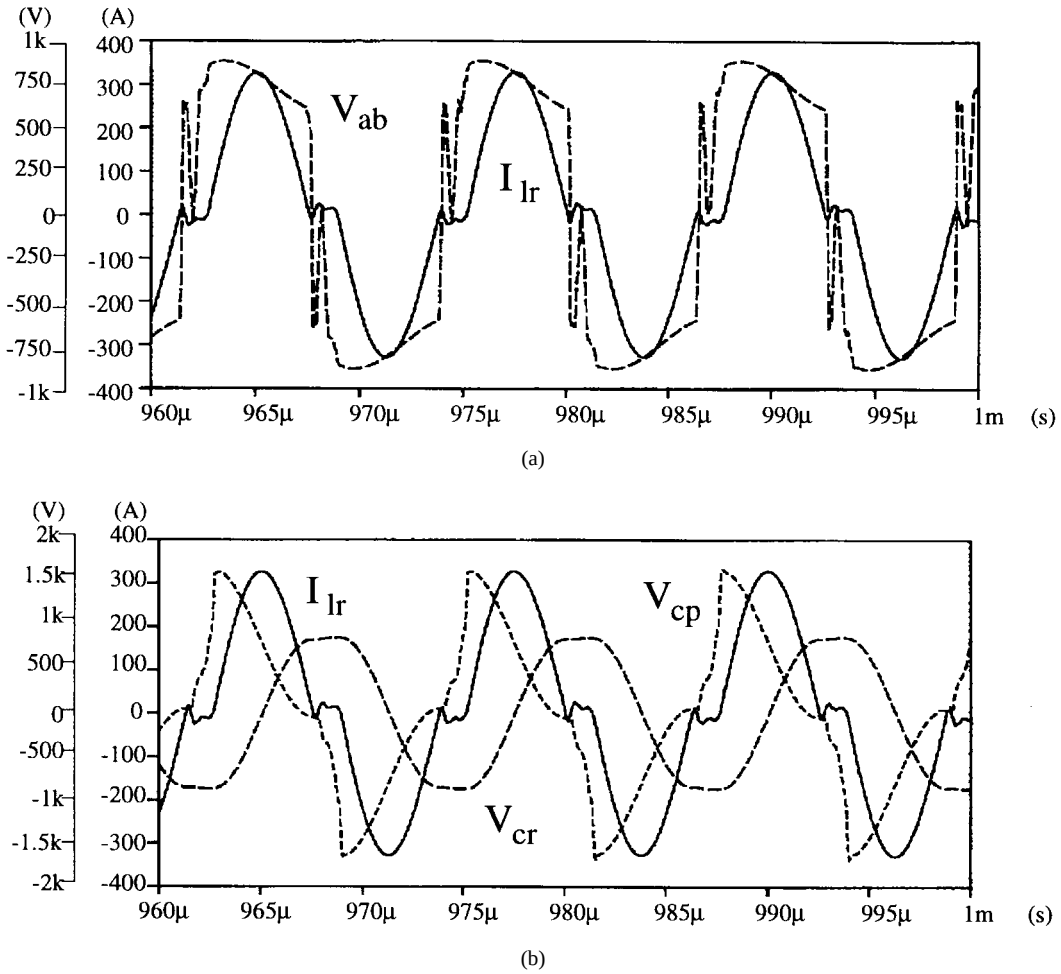


Fig. 13. SABER simulation results for the ZCS SRC with power circulation at $\omega_n = 0.77$.

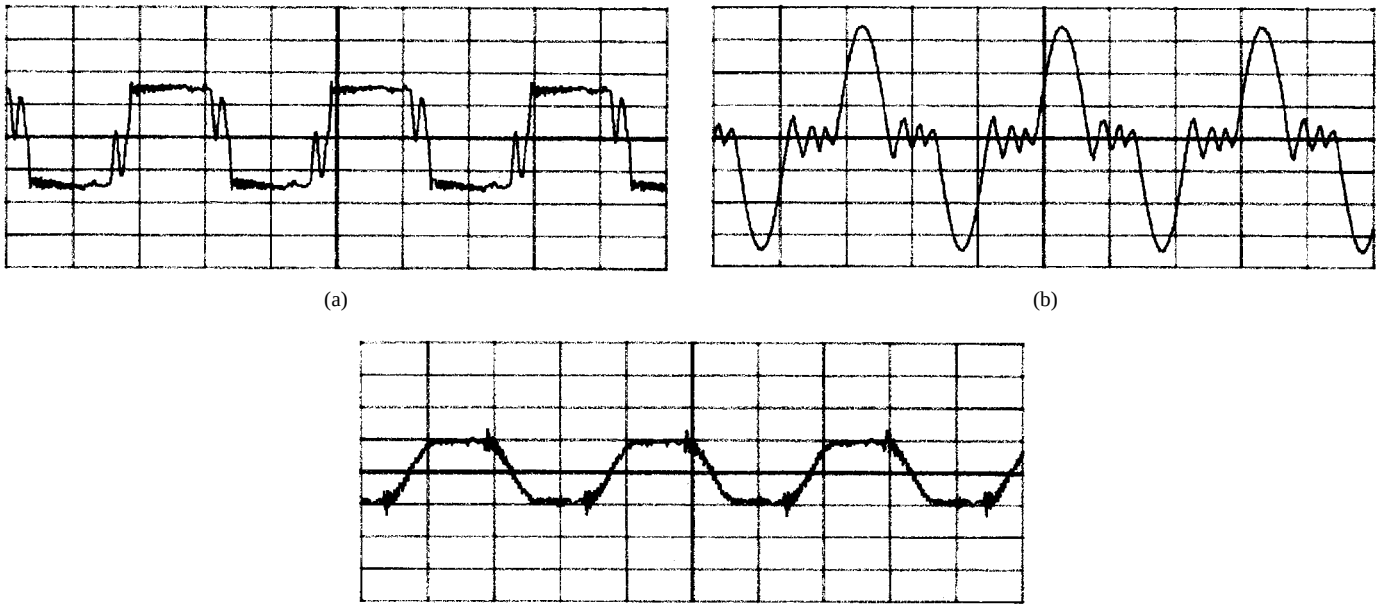
With a 120-kVA converter rating, the average dc-bus current is 150 A for an 800-V bus design. The resonant link carries a sinusoidal current with a half-cycle average of 150 A. This corresponds to a peak current of 384 A at an ω_n of 0.67. For a load quality factor of one half, a 4.0-μH resonant inductor is required. As a result, a 0.566-μF capacitor is needed to obtain a 105-kHz resonant frequency. In order to yield a more symmetrical structure, both of the resonant elements need to be split between the two inverter legs.

The resonant inductor for this implementation was realized using ferrite cores with a lumped air gap. The number of turns was two. The windings were constructed using 1.4-in 15-mil-thick copper strips. Heat sinks were used to provide cooling and optimize the losses within the windings. The total equivalent series resistance (ESR) calculated using finite-element analysis (FEA) was 1.75 mΩ, which gives a total loss of 100 W. Additional losses were incurred in the heat sink due to the induced currents within the sink. The heat-sink losses were calculated to be 103 W, which are quite significant compared to the winding losses. However, since these losses exist in the heat-exchange path, their impact on the thermal capacity of the windings is minimal. Twelve Phillips 3F10 C-core pairs were used to realize the resonant inductor. The selected core material was 3C81, and the total core losses estimated from manufacturer's data sheets were 210 W at 0.15 T and 70 kHz. As a result, the overall resonant-inductor losses are 413 W. In order to limit the maximum flux density to 0.15 T, a 0.14-in air gap is needed. The calculated resonant inductance value at under these conditions was 3.1 μH. The resonant capacitor was realized using two series modules of 1.0-μF/550 VAC high-frequency capacitors (CELEM CPRI 300). Hence, the series-effective capacitance is 0.5 μF, and the resultant resonant frequency is 123 kHz. The ESR of these capacitors at 100 kHz is 0.5 mΩ, which will result in 25 W of loss.

A simple fixed-frequency fixed-pulse controller was built to provide the driving signals for the gate drives. No feedback control is required here since output voltage control, and current limiting is done by controlling the input voltage.

Initial testing of the unit was carried out at 67 kHz with a bus voltage of 740 Vdc. The resonant frequency was found to be 120 kHz. A series load of 0.05 Ω was used before circulating back to the dc bus in order to limit the dc-output current. The power circulated through the unit was 96 kW with an average output current of 130 Adc. The input dc current was measured to be 6.35 A. As a result, the input power is 5447 W, and, hence, the converter efficiency is 94.7%. Fig. 14 shows the resultant experimental waveforms.

Based on the above measurements, the total converter losses are 5447 W. In order to verify these results, the calculated



(a) (b)

(c)

Fig. 14. Experimental results for the ZCS SRC with power circulation at $\omega_n = 0.67$.

TABLE V
CALCULATED COMPONENTS' LOSSES

Loss Component	Losses
DC Bus Caps	290 W
IGBTs	2600 W
Diode Bridge	920 W
Resonant Inductor (meas.)	515 W
Resonant Capacitor (meas.)	25 W
Parallel Inductor (meas.)	60 W
Auto transformer (meas.)	30 W
Series Load	845 W
Total Losses	5285 W

component losses are tabulated in Table V. Note here that the resonant-inductor measured losses (515 W) were higher than expected (413 W) due to the additional termination resistances which were not modeled by FEA. As shown in Table IV, the calculated losses (5285 W) pretty much match the measured ones (5447 W), which confirms the calculated figures.

VII. CONCLUSIONS

A high-power converter topology suitable for fast charging of EV's was selected. The proposed topology is a ZCS SRC. The impact of the IGBT losses under soft-switching conditions was incorporated in the analysis process to yield an optimized converter design. An experimental unit was built and tested in the laboratory. As shown earlier, the experimental results match the expected ones quite well.

Given the present IGBT die technology, it seems that under ZVS conditions, the additional losses caused by tail-current bump are quite significant, especially at high die temperatures. This limits the use of such IGBT's in high-power applications. On the other hand, ZCS eliminates the additional turn-off losses and, hence, allows high-power utilization of these devices. If IGBT's are to be effectively utilized in ZVS applications, the die design needs to be optimized for ZVS rather than hard-switching conditions.

REFERENCES

[1] N. H. Kutkut, D. M. Divan, and D. W. Novotny, "Inductive charging technologies for electric vehicles," in *PEC-Yokohama Conf. Rec.*, Apr. 1995, pp. 124–130.
[2] M. H. Kheraluwala, D. M. Divan, and E. Baumann, "Design considerations for high power density DC/DC converters," in *HFPC Conf. Rec.*, May 1990, pp. 324–335.
[3] F. C. Schwarz and J. B. Klassens, "Controllable 45 kW current source for DC machines," *IEEE Trans. Ind. Applicat.*, vol. IA-15, no. 4, pp. 437–444, 1979.
[4] R. L. Stiegerwald, "High frequency resonant transistor DC-DC converters," *IEEE Trans. Ind. Electron.*, vol. IE-31, pp. 181–191, May 1984.

[5] K. D. T. Ngo, "Analysis of a series resonant converter pulse width modulated or current controlled for low switching loss," *IEEE Trans. Power Electron.*, vol. 3, no. 1, pp. 55–63, 1988.
[6] A. Kurnia, O. H. Stielau, G. Vekataramanan, and D. M. Divan, "Loss mechanisms in IGBT's under zero voltage switching," in *IEEE-PESC Conf. Rec.*, 1992, pp. 1011–1018.
[7] A. Kurnia, H. Cherradi, and D. M. Divan, "Impact of IGBT behavior on design optimization of soft switching inverter topologies," in *IEEE-IAS Conf. Rec.*, 1993, pp. 807–813.
[8] J. Mucko, H. G. Langer, and J. Ch. Bendien, "A novel resonant DC-to-DC converter with high power density and high efficiency," in *EPE Conf. Rec.*, 1989, pp. 1467–1471.

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