High-Performance Active Gate Drive for High-Power IGBT's

Vinod John, *Student Member, IEEE*, Bum-Seok Suh, and Thomas A. Lipo, *Fellow, IEEE*

***Abstract*— This paper deals with an active gate drive (AGD) technology for high-power insulated gate bipolar transistors (IGBT's). It is based on an optimal combination of several requirements necessary for good switching performance under hard-switching conditions. The scheme specifically combines together the slow drive requirements for low noise and switching stress and the fast drive requirements for high-speed switching and low switching energy loss. The gate drive can also effectively dampen oscillations during low-current turn-on transient in the IGBT. This paper looks at the conflicting requirements of the conventional gate drive circuit design and demonstrates using experimental results that the proposed three-stage AGD technique can be an effective solution.**

***Index Terms*—Active gate drive, gate drive circuit, gate resistor, insulated gate bipolar transistor switching transient.**

I. Introduction

RECENTLY, the applications of insulated gate bipolar transistors (IGBT's) have expanded widely, particularly in the area of high-power converters. The gate drive circuit in the power converter is the interface between the IGBT power switches and the logic-level signals in the modulator. The gate drive circuit can be optimized to achieve the best performance that can be obtained from the power semiconductor device. A gate drive should switch the IGBT at a high speed, while limiting di/dt and dv/dt and associated noise generated during the switching transient. The simultaneous requirement to minimize switching losses, the peak reverse-recovery current stress during turn-on, and the peak overvoltage stress at turn-off makes gate drive design a challenging task. IGBT gate drive circuits have conventionally employed fixed gate resistors. The resistor is selected so as to suppress switching electromagnetic interference (EMI) to an acceptable level, and to limit the reverse-recovery current at turn-on and the overvoltage at turn-off with minimal energy loss. These conflicting requirements result in suboptimal performance of such a conventional gate drive (CGD) unit. To satisfy the switching stress constraint and the EMI generated, the required value of the gate resistor would be large. This compromise leads to long switching delays and higher switching losses, while merely being able to achieve acceptable noise levels and switching stresses.

The values of the turn-on and turn-off gate resistors have, in the past, been optimized and their effects studied in [1] and [2] with an aim to limiting the turn-on di/dt and the turn-off overvoltage and dv/dt. Also, [3] has investigated methods that utilize multiple gate resistors to control the overvoltage during turn-off switching transient at overcurrent levels. This study, however, was only for turn-off operation, and it was difficult to obtain optimized switching characteristics between the overvoltage and the turn-off energy loss at nominal current levels. The IGBT has been used in the active region at turn-off by using a closed-loop high-speed operational amplifier in the gate circuit [4]. In this case, the turn-off dv/dt can be precisely controlled according to the reference voltage command. The problem with this method is the large switching loss at turn-off, and the fact that the circuit cannot be easily extended to turn-on operation under an inductive load switching transient. A technique for reducing the power loss at turn-on by injecting additional current into the gate has been investigated in [5]. This method used a phase-locked loop to determine the instant of current injection into the gate of the device, which can result in poor operation under transient load current conditions. Also, the update of the control information occurs with one switching period delay and the total turn-on delay time is still quite large because a fixed gate resistor has been used to limit the di/dt during turn-on. Reference [6] has described a high-performance current-source gate drive used in a modular traction converter. Also, [7] has reported on the use of a high-performance gate drive for high-power IGBT converter applications. It is based on open-loop methods for reduced turn-on di/dt operation, with predetermined control points. Turn-off is controlled by using closed-loop measurement of the collector voltage. This information is used to limit the overvoltages for the series-connected IGBT's.

In this paper, a three-stage active gate drive (AGD) technique is presented for driving high-power IGBT's. The purpose of the proposed AGD is to obtain optimized switching performance for both turn-on and turn-off operation and for all operating conditions, with the following characteristics:

- reduced delay time at both turn-on and turn-off;
- reduced turn-on di/dt and the associated reverse-recovery effects;
- lower tail voltage and the resultant energy loss at turn-on;
- controlled overvoltage at turn-off;

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V. John and T. A. Lipo are with the Department Electrical and Computer Engineering, University of Wisconsin, Madison, WI 53706 USA (e-mail: vjohn@cae.wisc.edu; lipo@engr.wisc.edu).

B.-S. Suh was with the Department Electrical and Computer Engineering, University of Wisconsin, Madison, WI 53706 USA. He is now with Fairchild Korea Semiconductor, Samsung Electronics, Puchon 420-711, Korea (e-mail: bssuh@fairchildsemi.co.kr).

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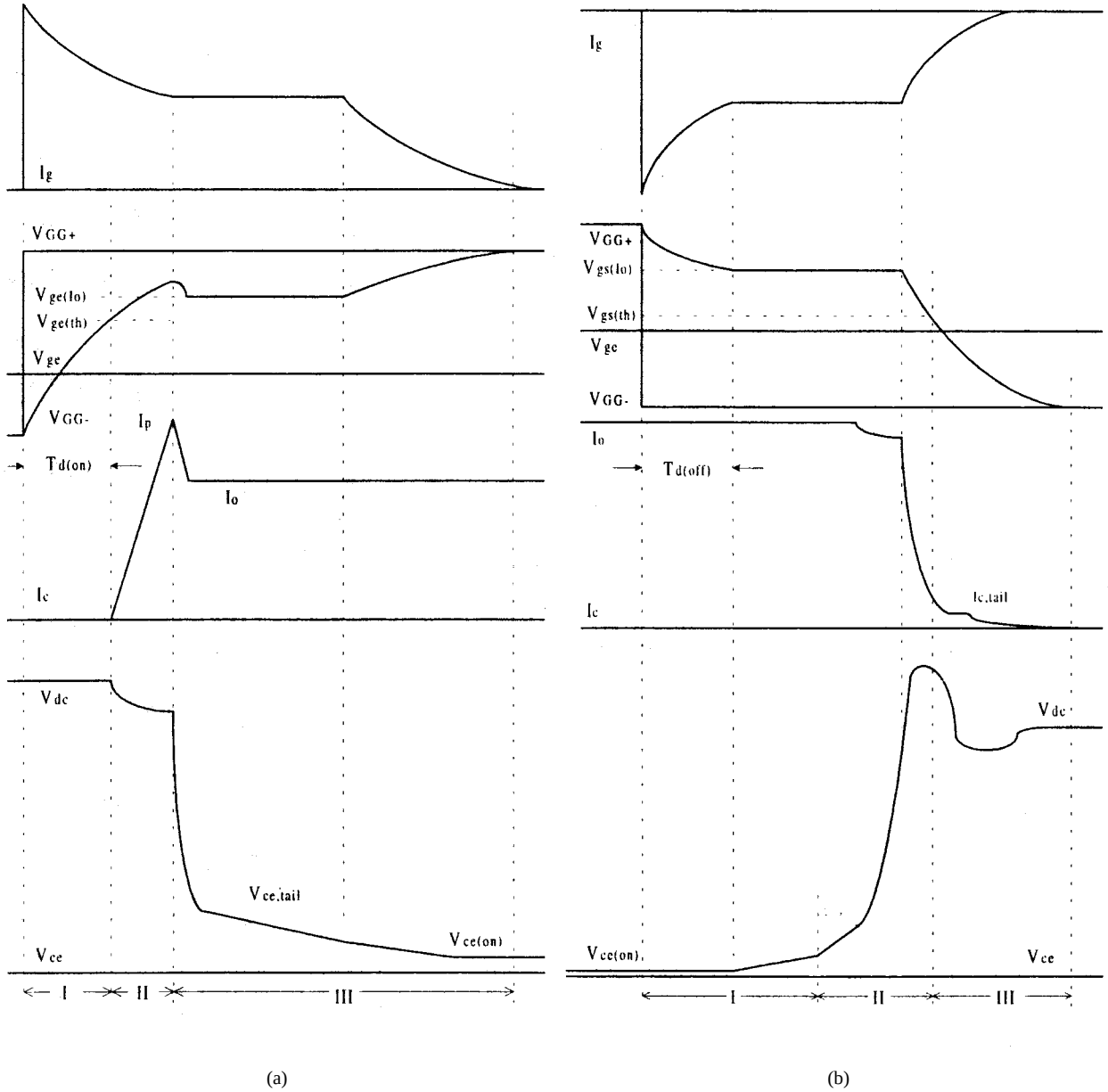


(a) (b)

Fig. 1. Sketches of (a) turn-on and (b) turn-off waveforms of an IGBT under inductive load switching with a CGD circuit.

- reduced energy loss due to improved dv/dt characteristics at turn-off;
- reduced total switching time at both turn-on and turn-off.

II. Proposed Three-Stage AGD

Typical collector and gate voltages and current waveforms at turn-on and turn-off with a CGD are sketched in Fig. 1. The turn-on characteristics show the delay time before the rising of the collector current, the reverse-recovery transient at the end of the current rise, and the tail voltage at the end of the voltage fall. During turn-off, Fig. 1(b) shows the delay time before the collector voltage rise, the overvoltage during the collector current fall, and the tail phenomena at the end of the collector current fall. Detailed explanation of the switching transient in the IGBT is available in [2] and [8]–[10]. This paper divides the typical switching waveform into three regions, in order to obtain different control purposes based on the successive stages of the switching transient, as shown in Fig. 1(a) and (b), respectively. Hence, it is called a three-stage AGD technique.

The timing requirement for the three-stage control is illustrated in Fig. 2. The power circuit topology considered is the hard-switched voltage-source inverter leg shown in Fig. 3. *Stage I* immediately follows the main command at turn-on. This stage is designed to minimize the delay time by rapidly charging the IGBT gate with a large gate current. Once the gate voltage has reached the threshold voltage level of the device, the second stage of operation is initiated. During this stage, control of the turn-on di/dt is achieved by a reduced rate of charging of the IGBT gate. This is because the turn-on behavior of the IGBT is similar to a MOSFET, which allows the collector current to be controlled based on the gate voltage. *Stage II* continues until the collector current reaches the load

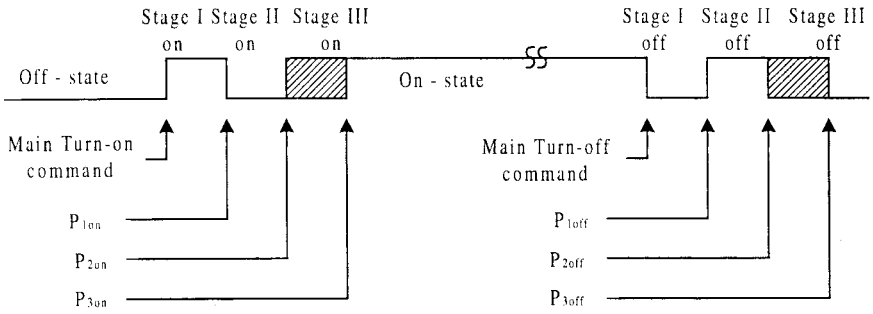


Fig. 2. Timing diagram corresponding to the three-stage active turn-on and turn-off switching.

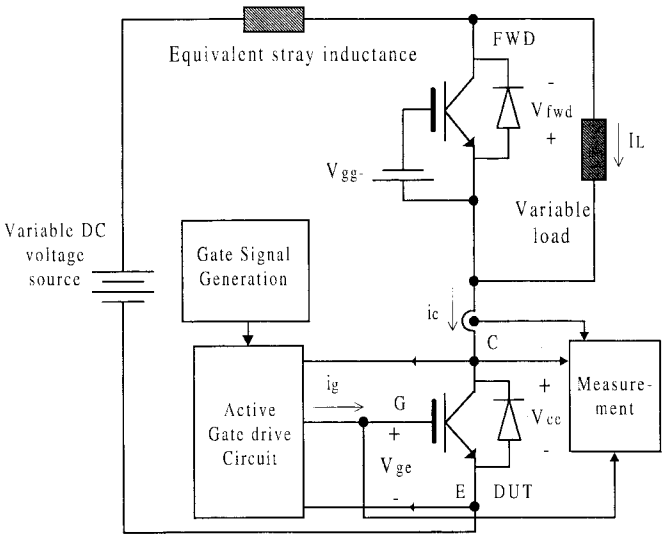


Fig. 3. The experimental setup used for investigating the gate drive circuits.

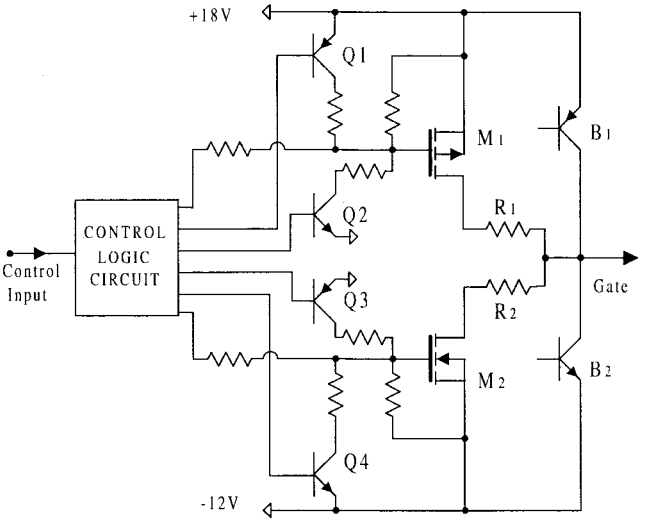


Fig. 4. Schematic of the proposed three-stage AGD circuit.

current plus the peak reverse-recovery current. The reverse-recovery current can be effectively controlled due to the lower turn-on di/dt. The current injected into the gate during *Stage II* is reduced so as to minimize the effects of the reverse-recovery current on the converter system. These effects include the overvoltage across the complementary switch caused by the freewheeling diode snap-off and the EMI generated by the ringing during the reverse-recovery transient. The circuit shifts to *Stage III* of turn-on at this point, and the gate is now rapidly charged to reduce the tail voltage, thus decreasing the power loss during turn-on. Also, the Miller plateau duration and the total switching time are reduced by *Stage III*.

The main objective of the active turn-off circuit is to control the overvoltage at turn-off with minimal switching delay and switching loss. *Stage I* of the three-stage active turn-off control starts at the main turn-off command. The first stage consists of rapid discharging of the gate-emitter capacitor until the rising instant of the collector voltage. This considerably reduces both the turn-off delay time and the power loss caused by the slow initial rise of the collector voltage. The large gate current during *Stage I* causes the gate voltage to go below the threshold voltage, resulting in a higher dv/dt and a lower power loss. At this point, *Stage II* is initiated and the gate current is reduced. The collector voltage rise during turn-off of the IGBT causes the gate voltage to charge up because of the displacement current through the gate-collector capacitor. The gate voltage goes above the threshold voltage, which results in excess carriers being injected into the IGBTs' buffer region through the gate channel. This results in a lower turn-off di/dt and a reduced overvoltage during turn-off. The gate is discharged slowly during *Stage II* of turn-off operation. This stage continues through the rising period of the collector voltage and the falling period of the collector current. *Stage III* is initiated at the end of the rapid falling of the collector current. This stage makes the gate voltage rapidly attain its final negative value. The low gate resistance during *Stage III* and turn-off steady state improves noise immunity during the off state of the IGBT [11]. The total switching time is also reduced. Any re-turn-on of the IGBT is prevented in the three-stage method because the gate current remains negative in all three active turn-off stages, thus ensuring stable operation.

III. Implementation of the Three-Stage AGD

The schematic diagram of the gate drive circuit is shown in Fig. 4. A MOSFET and a bipolar junction transistor (BJT) are used in parallel in the circuit for both turn-on and turn-off operation. The use of MOSFET's M_1 and M_2 in the gate drive allows one to effectively obtain higher gate current required during *Stage-I* and *Stage-III* operation for high-power IGBT's.

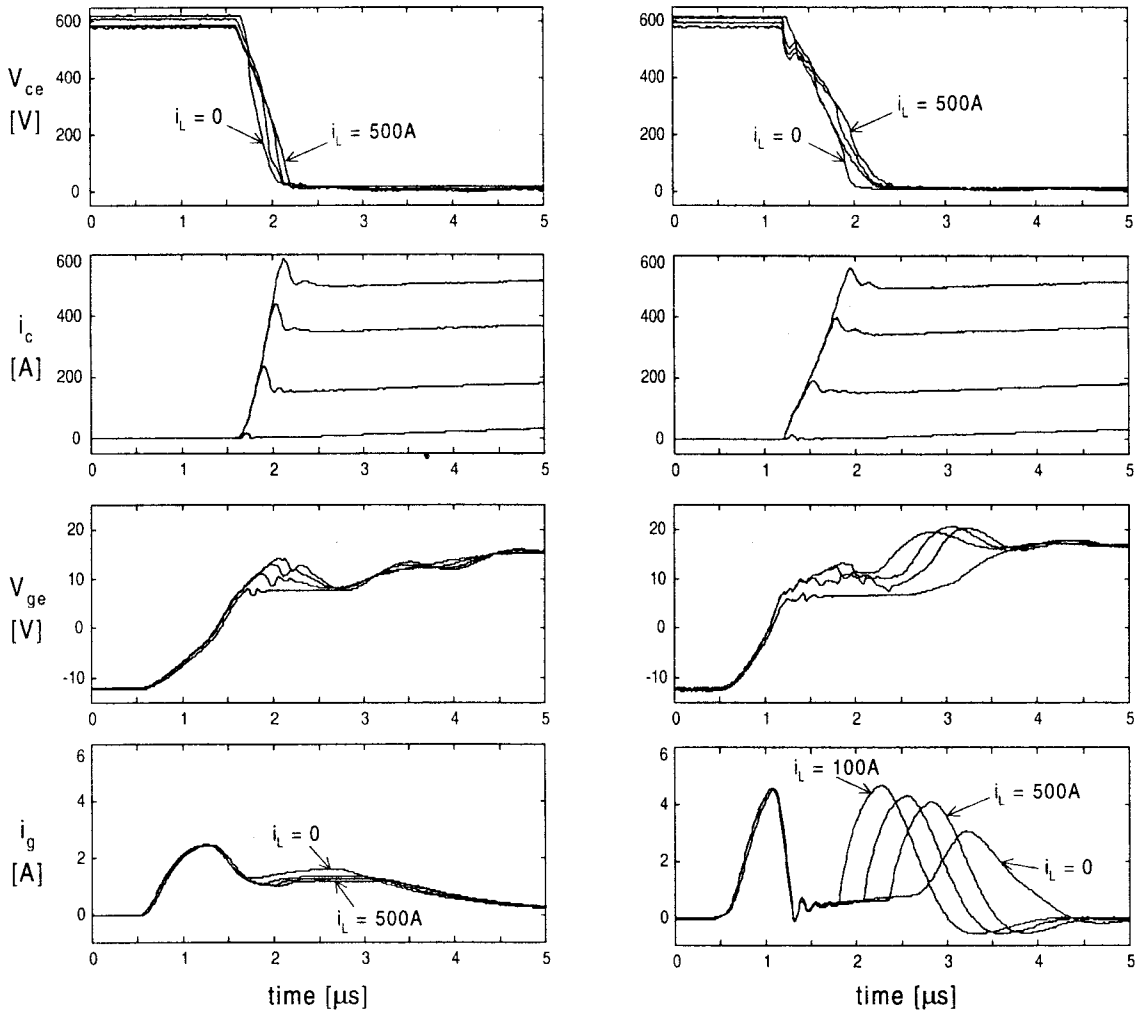


Fig. 5. Measured turn-on switching waveforms $(v_{ce}, i_c, v_{ge}, i_g)$ with (a) the CGD and (b) the AGD at current levels of 0, 150, 350, and 500 A. Turn-on resistor of 5.6 Ω is used in the CGD. Other conditions are as follows: $V_{dc} = 600$ V; $V_{gg+} = 18$ V; $V_{gg-} = -12$ V.

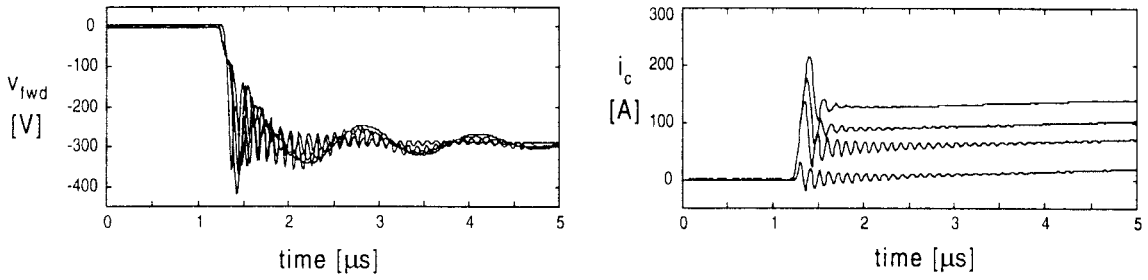
One can fully utilize the supply voltage in the gate drive and operate rail to rail by using the MOSFET's. The BJT's B_1 and B_2 in parallel with the MOSFET's allow precise gate current control during *Stage II* of the active switching transient. Additional BJT's, Q_1–Q_4, which are shown in Fig. 4, are used to control M_1 and M_2 during *Stage II* and *Stage III*. Resistors R_1 and R_2 are used to limit the peak gate current and to obtain damped switching transients in the AGD circuit.

A. Active Turn-On

At the main command to turn the IGBT on, *Stage I* is initiated by turning MOSFET M_2 off and turning M_1 on in Fig. 4. The use of an extremely low value of the gate resistor R_1 results in rapid charging of the IGBT gate. The turn-off of M_1 occurs at time $P_{1\text{on}}$, which is shown in Fig. 2, corresponds to the rising instant of the collector current in the IGBT. However, due to propagation time in the turn-off of M_1, one has to initiate the turn-off of M_1 at a prior instant. This can be selected as a fixed parameter for an IGBT of given ratings. $P_{1\text{on}}$ can also be triggered using measured gate voltage. The gate now charges at a controlled current level determined by transistor B_1, which is used in the active region as a controlled current source during *Stage II*. $P_{2\text{on}}$ is detected in the AGD by utilizing the di/dt information obtained by measuring the voltage from the Kelvin emitter to the power emitter in the IGBT [12]. This allows the gate of the IGBT to be controlled based on the instantaneous load current level. Once the collector current reaches the peak reverse recovery current, *Stage III* is initiated by turning M_1 on again. $P_{3\text{on}}$ is a fixed parameter based on the ratings of the IGBT, and it can be considered the minimum on time for the device under consideration.

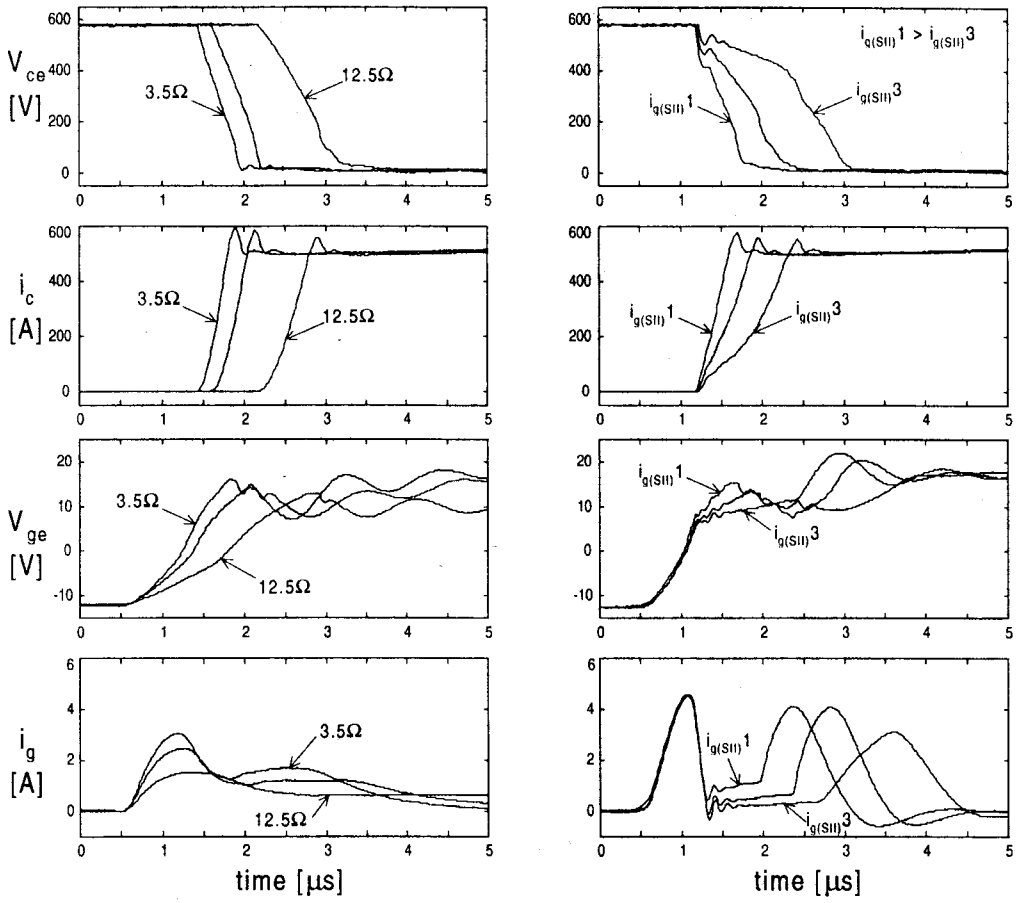
B. Active Turn-Off

This operation is also realized by the three-stage AGD turn-off technique. At the main command to turn off the IGBT, MOSFET M_1 is turned off and M_2 is turned on. The resistor R_2 is selected to be a very low value in comparison with the recommended value from the data sheets. *Stage I* continues until the rising instant of the collector voltage. $P_{1\text{off}}$



(a) (b)

Fig. 6. Measured turn-on waveforms with the CGD at current levels of 0, 50, 80, and 120 A when the gate resistor of 0.5 Ω is used. (a) The freewheeling diode voltage. (b) The collector current. Other conditions are as follows: $V_{dc} = 300$ V; $V_{gg+} = 18$ V; $V_{gg-} = -12$ V.



(a) (b)

Fig. 7. Measured turn-on switching waveforms $(v_{ce}, i_c, v_{ge}, i_g)$ with (a) the CGD and (b) the AGD when the turn-on di/dt is varied. Turn-on gate resistors used for varying di/dt in the CGD are 3.5, 5.6, and 12.5 Ω. Other conditions are as follows: $V_{dc} = 600$ V; $I_L = 500$ A; $V_{gg+} = 18$ V; $V_{gg-} = -12$ V.

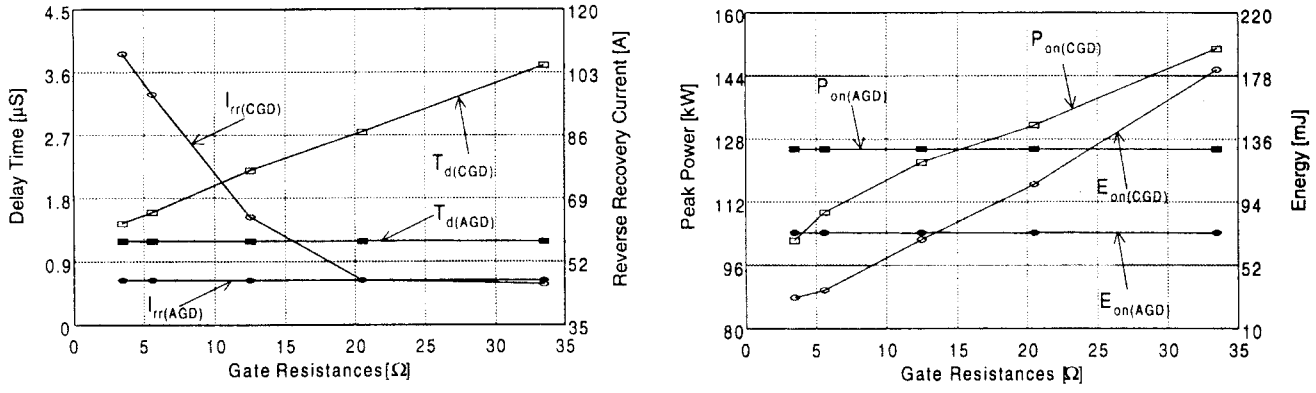
is detected using a collector voltage desaturation circuit. *Stage II* is initiated at this instant by turning M_2 off. Transistor B_2 drains a controlled current level out of the gate during this stage. *Stage III* is initiated at $P_{2\text{off}}$, which corresponds to the falling edge of the collector current. The gate voltage reaches its final negative value by $P_{3\text{off}}$, which can be considered to be the total turn-off time for the given IGBT.

IV. Performance of the Three-Stage AGD

Comparative results with the CGD are presented in order to investigate the operational performance of the three-stage AGD. The device used for the experimental test is a 1200-V 600-A Powerex IGBT (CM600HA-24H). The switching waveforms for the CGD circuit were acquired using a gate resistance of 5.6 Ω, which is a typical value for obtaining acceptable low-noise switching for this IGBT. The value of the resistors R_1 and R_2 in the AGD shown in Fig. 3 is 0.5 Ω. The trigger point for all measurements is the main command to the gate drive, which corresponds to zero in the time axis.

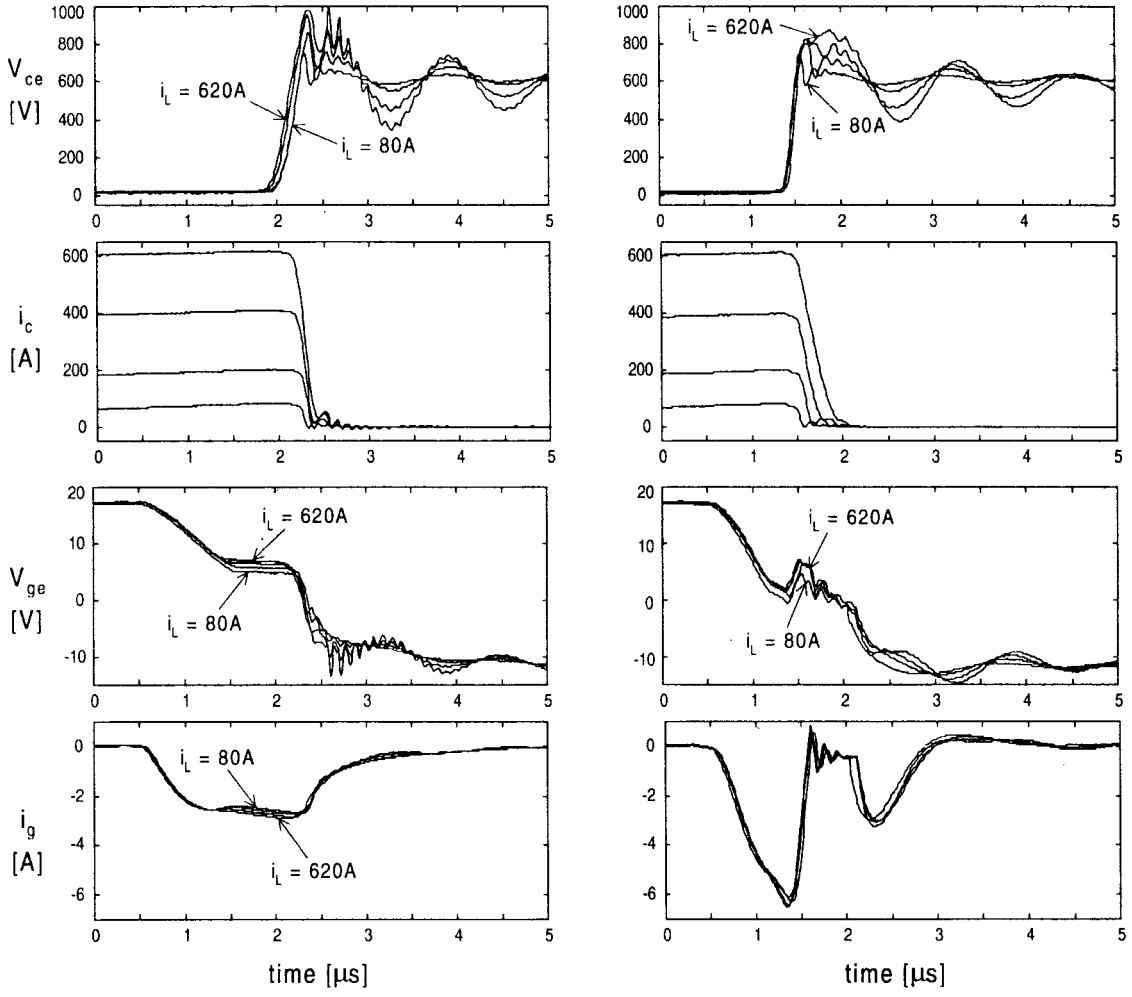
A. Investigation of Turn-On Characteristics

The turn-on switching waveforms of the CGD and the AGD at different load current levels are shown in Fig. 5(a) and (b), respectively. The waveforms plotted are the collector



(a) (b)

Fig. 8. Comparison of turn-on characteristics between the AGD and the CGD as gate resistance is varied. (a) Investigation of the turn-on delay time and the peak reverse-recovery current. (b) Investigation of the peak power and the turn-on energy loss. Operating conditions are as follows: $V_{dc} = 600$ V; $I_L = 350$ A; $V_{gg+} = 18$ V; $V_{gg-} = -12$ V.



(a) (b)

Fig. 9. Measured turn-off switching waveforms $(v_{ce}, i_c, v_{ge}, i_g)$ with (a) the CGD and (b) the AGD at current levels of 80, 205, 405, and 620 A. Turn-off gate resistor used in the CGD is 5.6 Ω. Other conditions are as follows: $V_{dc} = 600$ V; $V_{gg+} = 18$ V; $V_{gg-} = -12$ V.

voltage v_{ce}, the collector current i_c, the gate voltage v_{ge}, and the gate current i_g. It can be seen that the AGD circuit reduces the turn-on delay time, as well as the total switching time, while limiting the reverse-recovery current below that obtained using the CGD. The di/dt in the AGD is controlled by *Stage II* to a lower value, and the collector voltage is held higher for a longer duration during the rising time of the collector current. The time required for the gate voltage to

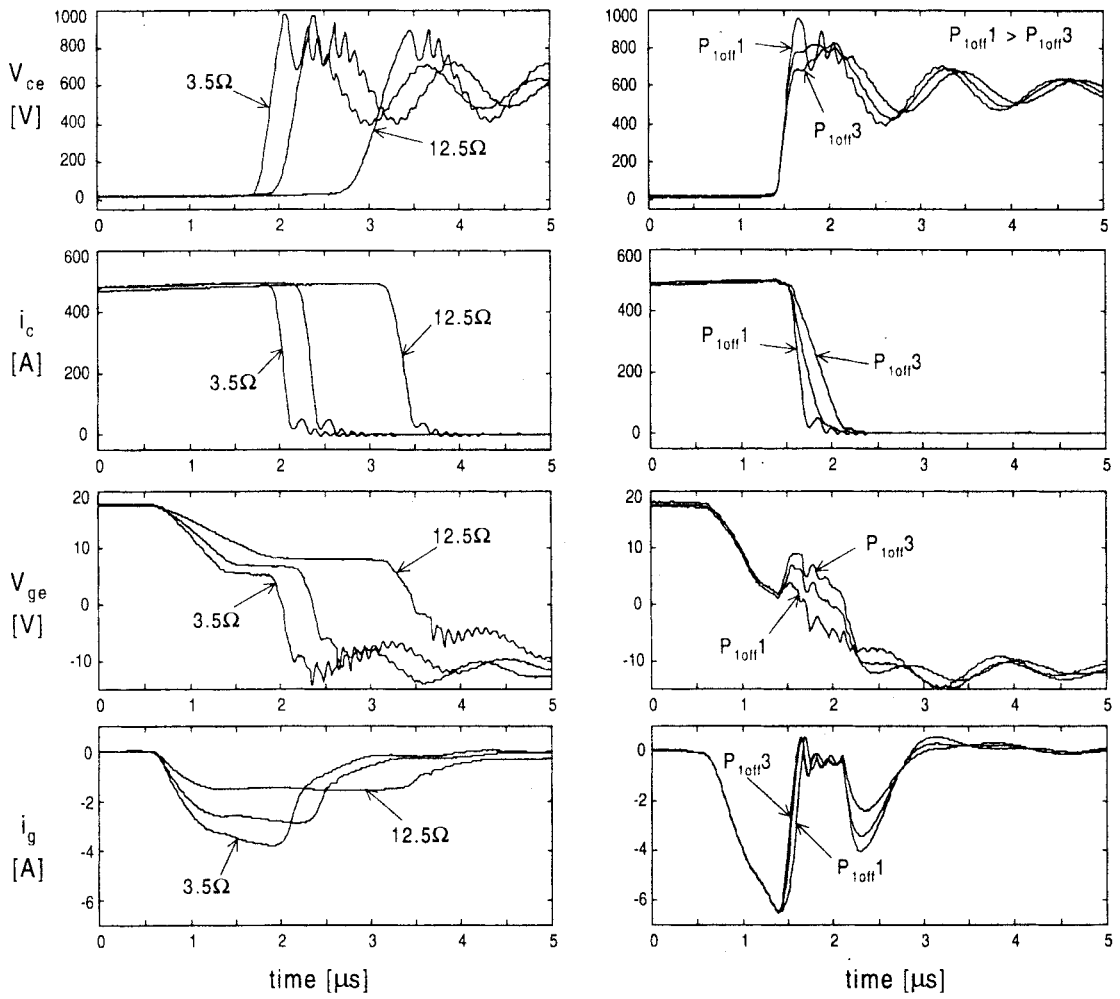


Fig. 10. Measured turn-off switching waveforms $(v_{ce}, i_c, v_{ge}, i_g)$ with (a) the CGD and (b) the AGD when the turn-off di/dt is varied. Turn-off gate resistors used in the CGD for varying di/dt are 3.5, 5.6, and 12.5 Ω. Other conditions are as follows: $V_{dc} = 600$ V; $I_L = 500$ A; $V_{gg+} = 18$ V; $V_{gg-} = -12$ V.

reach the given positive bias voltage, +18 V, is reduced in the AGD. Therefore, the turn-on switching energy due to the tail voltage can be considerably reduced. The effect of variation of collector current level on the AGD can be seen from the gate current waveforms, which show the adaptation of the duration of *Stage II* based on the instantaneous load current level.

If one uses a small fixed gate resistor (0.5 Ω) in the CGD circuit, the peak reverse-recovery current and the peak voltage across the freewheeling diode will be large. Lower current level and dc-bus voltage are used in this test because of IGBT failure with very small gate resistance, due to the high di/dt and dv/dt during switching. In particular, there are large oscillations at low current turn-on, as can be seen in the freewheeling diode voltage and the collector current waveforms in Fig. 6(a) and (b), respectively. This effect occurs because the rapid turn-on of the device can set up highly underdamped oscillations between the parasitic capacitance of the device and the inductance of the bus structure and interconnects. The snap-off process during the reverse recovery excites the oscillation. These oscillations are most severe at low current levels. The conductivity modulation lag effect increases the effective resistance in the circuit at turn-on [13], and helps to dampen out the turn-on oscillations. The AGD extends the duration of *Stage-II* turn-on operation and damps out oscillations at low current turn-on, as shown in Fig. 5(b). Increase in the turn-on power loss due to longer *Stage II* does not occur due to the very low load current level.

Fig. 7(a) and (b) show the effect of control of the turn-on di/dt in the CGD and the AGD, respectively. This can be achieved in the CGD by varying the gate resistor. The whole gate current waveform is lowered when the gate resistor is increased, as shown in Fig. 7(a). This leads to the longer turn-on delay and the larger collector voltage tail. From the gate current waveform in Fig. 7(b), it can be seen that the turn-on di/dt in the AGD is effectively controlled by the variation of gate current during *Stage II*, $i_{g(\mathrm{sII})}$, without affecting the delay time. Higher levels of gate current during *Stage II* at turn-on leads to higher di/dt. Variation of the dc-bus voltage does not lead to any significant difference in the performance of the CGD or the AGD. The turn-on di/dt is higher at the larger dc-bus voltage.

Fig. 8(a) and (b) show the tradeoff in turn-on characteristics of the delay time, the peak reverse-recovery current, the peak power dissipation, and the energy loss in the case of the CGD.

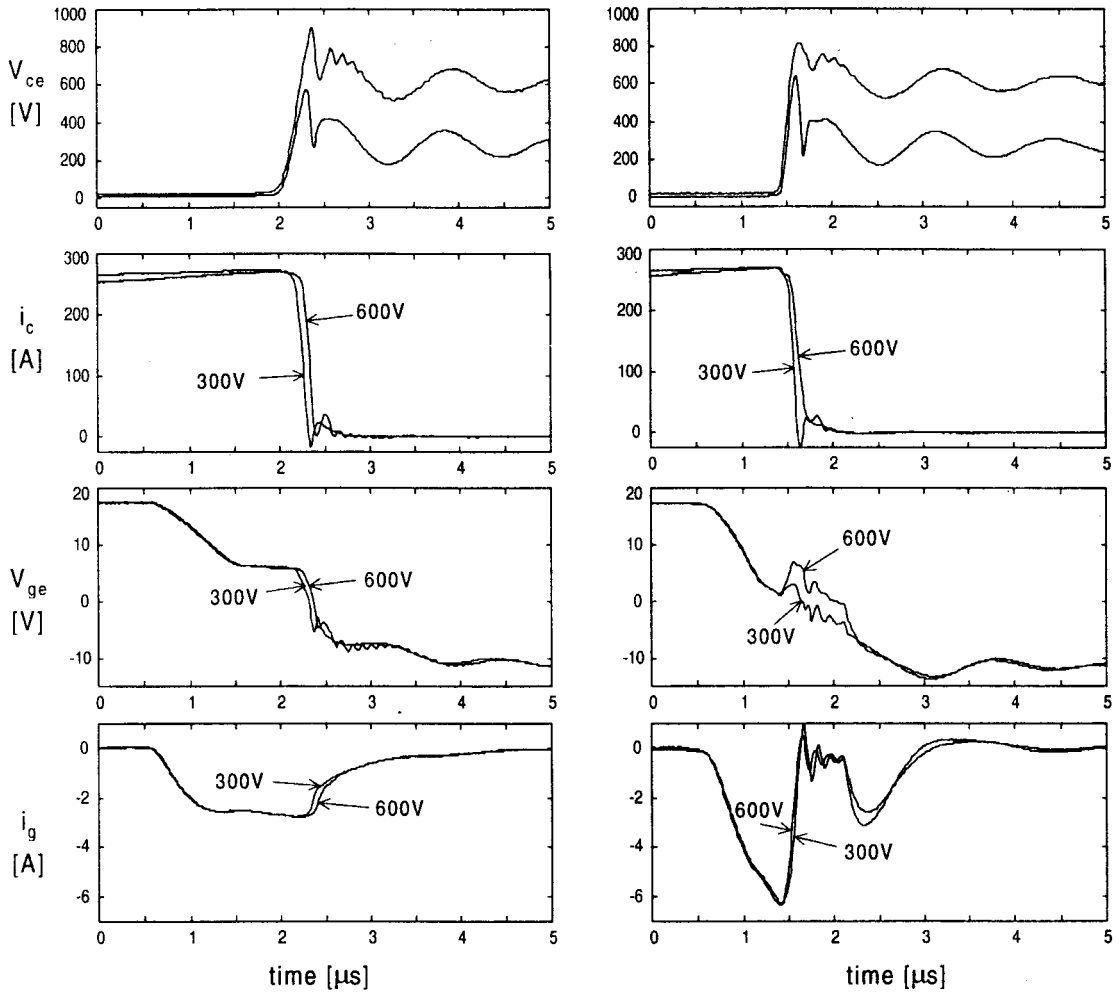


Fig. 11. Measured turn-off switching waveforms $(v_{ce}, i_c, v_{ge}, i_g)$ with (a) the CGD and (b) the AGD when the dc-bus voltage is varied. The dc-bus voltages are 300 and 600 V. Turn-off gate resistor used in the CGD is 5.6 Ω. Other conditions are as follows: $I_L = 270$ A; $V_{gg+} = 18$ V; $V_{gg-} = -12$ V.

Different turn-on gate resistors are used under a constant load current of 350 A. The results are compared with that obtained with the AGD circuit at the same power conditions. As the turn-on gate resistor $R_{g\text{on}}$ is increased, the delay time and the dissipated turn-on energy increase, while the peak reverse-recovery current decreases. The delay time of the AGD is shorter than that of a CGD with $R_{g\text{on}}$ of 3.6 Ω and reverse-recovery current lower than that of a CGD with 15 Ω, and the switching energy less than a CGD with 12.5 Ω. The improved performance of the AGD over the CGD holds good for a wide range of current levels and operating conditions.

B. Investigation of Turn-Off Characteristics

The switching waveforms of the CGD and the AGD at turn-off for different load current levels are shown in Fig. 9(a) and (b), respectively. The turn-off dv/dt is higher in the AGD, while the di/dt is lower. The AGD results in a lower overshoot and ringing in the collector voltage waveform, as shown in Fig. 9(b). This can lead to lower EMI generated during turn-off transient. The peak overshoot in the collector voltage is limited to a lower level for a wide range of collector currents in the AGD. As turn-off delay time is varied with load current, the transition from *Stage I* to *Stage II* is adapted by the AGD to further reduce the turn-off di/dt at higher current levels. The active turn-off reduces the switching losses by reducing the slow initial rising duration of the collector voltage, while at the same time achieving better control of the overvoltage compared to the case of utilizing a large gate resistor in the CGD circuit.

Fig. 10(a) and (b) show the control of the turn-off di/dt during turn-off switching transient. This control is achieved in the CGD by controlling the gate resistor value. Increasing the gate resistor results in increased switching delay and a softer switching transient. The lower dv/dt that occurs with larger gate resistors increases the turn-off energy. The di/dt control in the AGD is achieved by introducing a delay in the $P_{1\text{off}}$ control point. This determines the gate voltage level during *Stage II* of active turn-off. A larger delay in the $P_{1\text{off}}$ control point results in a higher turn-off di/dt. From the collector current waveforms in Fig. 10(b), it can be seen

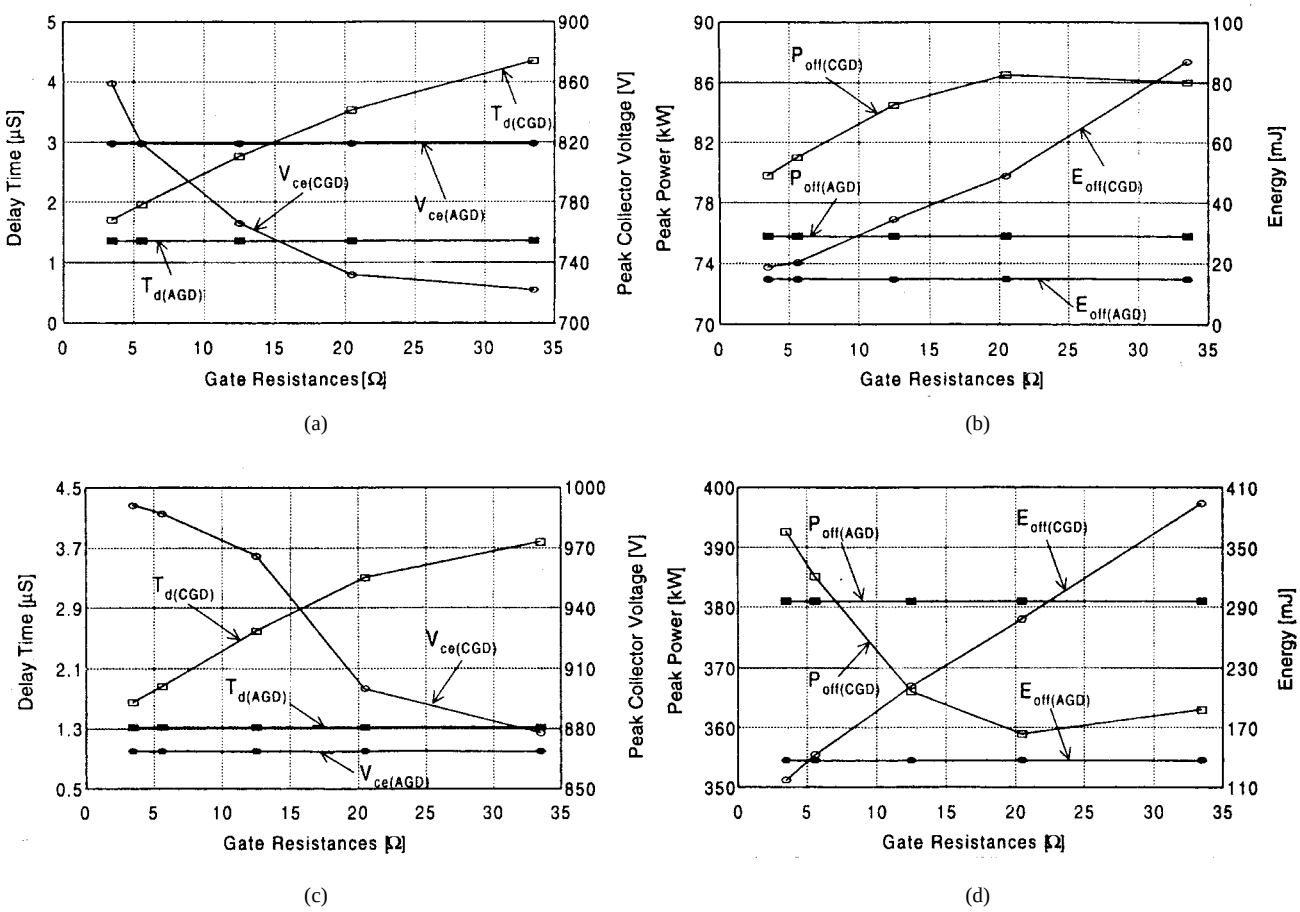


Fig. 12. Comparison of turn-off characteristics between the AGD and the CGD as the gate resistance is varied. (a) and (b) $I_L = 150$ A. (c) and (d) $I_L = 620$ A. (a) and (c) Investigate the delay time and the peak collector voltage. (b) and (d) Investigate the peak power and the energy loss. Operating conditions are as follows: $V_{dc} = 600$ V; $V_{gg+} = 18$ V; $V_{gg-} = -12$ V.

that the switching delay time and the di/dt variation are decoupled. The higher turn-off di/dt results in the higher collector overvoltage, but reduces the energy loss.

Fig. 11(a) and (b) show the effect of increasing the dc-bus voltage on the performance of the CGD and the AGD, respectively. The overvoltage level in the case of the CGD is similar at higher dc-bus voltages. In the case of the AGD, the overvoltage is reduced because the reverse transfer capacitance, the collector-gate capacitance of the IGBT, is more effective in increasing the gate voltage during turn-off *Stage II* as the dc-bus voltage is increased. This can be seen from the gate voltage waveform of the AGD in Fig. 11(b). This leads to lower turn-off di/dt at higher dc-bus voltages in the AGD.

The tradeoff in the CGD performance according to variation of the turn-off gate resistance and the comparison with that of the AGD are illustrated in Fig. 12. Fig. 12(a) and (b) are at a load current of 150 A, and Fig. 12(c) and (d) are at 620 A. The turn-off performance is compared in terms of parameters such as the delay time, the peak collector voltage, the peak power dissipation, and the energy loss at turn-off. As the turn-off gate resistor R_{goff} is increased, the delay time and the turn-off energy loss increase, while the peak collector voltage reduces. The AGD has the turn-off delay lower than that of a CGD with R_{goff} of 3.6 Ω, and the overvoltage of the AGD is less than that of a CGD with 5.6 Ω at a collector current level of 150 A. The turn-off energy is lower than that of a CGD with 5.6 Ω. At higher current level, the AGD is more effective in suppressing the overvoltage. Fig. 12(c) shows that the AGD has a lower overvoltage than that of a CGD with 33 Ω at a turn-off current level of 620 A.

V. Conclusions

This paper has demonstrated that an AGD is able to achieve shorter switching delay and total switching time. Thus, it can be operated with lower blanking times, leading to lower distortion in the output spectrum of IGBT power converters. The lower peak reverse-recovery current level at turn-on and the lower peak overvoltage at turn-off can reduce the switching stress and EMI problem. The switching energy in the AGD is lower than that of a CGD operating at the same peak device stress level. The positive bias voltage of +18 V is a little higher than the conventional one, which can lead to large fault currents under short-circuit conditions. Hence, it is important to combine the operation of the AGD with a fault-current-limiting circuit [12] when higher gate voltages are used. One drawback of the AGD is control complexity. Also, the AGD has to be tuned to operate with the individual device. However, most of the tuning can be implemented as software initialization of the gate drive unit. This would make the AGD compatible with a wide range of IGBT applications. Also, the

same gate drive circuit can be used in both hard-switched and soft-switched applications. In a soft-switched power converter, *Stage II* of the AGD switching operation can be eliminated to obtain a high-speed gate drive. Such a gate drive circuit would be appropriate for building standardized power converters like the "Power Electronic Building Blocks."

REFERENCES

[1] F. Blaabjerg and J. K. Pederson, "An optimum drive and clamp circuit design with controlled switching for a snubberless PWM-VSI-IGBT inverter leg," in *Proc. IEEE PESC'92*, 1992, pp. 289–297.

[2] R. Chokhawala, J. Catt, and B. Pelly, "Gate drive considerations for IGBT Modules," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 1992, pp. 1186–1195.

[3] H. G. Eckel and L. Sack, "Optimization of the turn-off performance of IGBT at overcurrent and short-circuit current," in *Proc. EPE'93*, 1993, pp. 317–322.

[4] A. N. Githiari, R. J. Leedham, and P. R. Palmer, "High performance gate drives utilizing the IGBT in the active region," in *Proc. IEEE PESC'96*, 1996, pp. 1754–1759.

[5] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo, and M. Melito, "A new adaptive driving technique for high current gate controlled devices," in *Proc. IEEE APEC'94*, 1994, pp. 480–486.

[6] A. Lindberg, W. Belwon, and P. Oom, "MACS ICON-IGBT based propulsion system," in *Proc. EPE'97*, 1997, pp. 3.492–3.497.

[7] S. Gediga, R. Marquardt, and R. Sommer, "High power IGBT converters with new gate drive and protection circuit," in *Proc. EPE'95*, 1995, pp. 66–70.

[8] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics Converters, Applications and Design*. New York: Wiley, 1995.

[9] F. Calmon, J. P. Chante, E. Reymond, and A. Senes, "Analysis of the IGBT dv/dt in hard switching mode," in *Proc. EPE'95*, 1995, pp. 1.234–1.239.

[10] V. Venketashan, M. Eshaghi, R. Borras, and S. Deuty, "IGBT turn-off characteristics explained through measurements and device simulation," in *Proc. IEEE APEC'97*, 1997, pp. 175–178.

[11] N. McNeill, S. J. Finney, and B. W. Williams, "Assessment of negative off-state gate voltage requirements for IGBT's," in *Proc. IEEE PESC'96*, 1996, pp. 627–630.

[12] V. John, B. S. Suh, and T. A. Lipo, "Fast clamped short circuit protection of IGBT's," *IEEE Trans. Ind. Applicat.*, vol. 35, pp. 477–486, Mar./Apr. 1999.

[13] M. Redding and R. Kraus, "The influence of the base resistance modulation on switching losses in IGBT's," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 1996, pp. 1500–1506.

Vinod John (S'92), for a photograph and biography, see p. 486 of the March/April 1999 issue of this TRANSACTIONS.

Bum-Seok Suh, for a photograph and biography, see p. 486 of the March/April 1999 issue of this TRANSACTIONS.

Thomas A. Lipo (M'64–SM'71–F'87), for a photograph and biography, see p. 486 of the March/April 1999 issue of this TRANSACTIONS.