A Unity-Power-Factor Three-Phase PWM SCR Rectifier for High-Power Applications in the Metal Industry

Ian Wallace, Ashish Bendre, Jonathan P. Nord, and Giri Venkataramanan

***Abstract*—A new thyristor current-source rectifier that achieves unity power factor, low-current total harmonic distortion (THD), and dc-bus current and voltage control is presented. The rectifier is suitable for high-power applications such as induction heating and dc arc furnaces. It combines a traditional six-pulse thyristor bridge and a dc chopper that together solve power quality problems such as poor power factor and flicker generation. This topology achieves low input current THD and dc power control without additional power-factor-correction equipment, harmonic trap filters, use of multiple pulse rectifiers, or high-K-factor transformers.**

***Index Terms*—Commutated circuits, pulsewidth-modulated power converters, rectifiers, thyristor converters.**

I. Introduction

HIGH-POWER ac–dc rectifiers constitute an important enabling technology in the metals industries. Their applications include electrowinning, dc arc furnaces, resistive heating and plasma cutting, to name a few [1], [2]. Historically, they have been realized using regulating transformers followed by uncontrolled diode bridge rectifiers and phase-controlled SCR bridge rectifiers.

Fig. 1 shows the schematic of the power circuit of an SCR phase-controlled rectifier. The dc voltage and current can be controlled by adjusting the firing angle of the thyristor. However, the phase control action inherently results in poor displacement power factor. Furthermore, the line current is typically rich in low-frequency harmonics. In order to meet harmonic control standards such as IEEE 519, passive and/or active harmonic compensation techniques have to be employed. In most instances, the transformers used to feed the system will have to be K-factor rated in order to account for the additional heating resulting from harmonic currents. These, and a host of other benefits have prompted the introduction of dc choppers to be applied for these applications [2].

The power circuit schematic of such a diode bridge rectifier–dc chopper system configuration is shown in Fig. 2. The diode bridge rectifier feeds a capacitor bank on the dc bus. The rectified voltage at the dc bus is conditioned using a buck-type dc–dc converter, which is capable of controlling the output current or voltage as required by the load. This configuration is becoming preferred especially with the dramatic advances in the technology of insulated gate bipolar transistors (IGBTs).

While the diode bridge has near-unity displacement power factor, the input current total harmonic distortion (THD) is still poor. Multipulse techniques will have to be used for harmonic elimination. Furthermore, the transformer K-factor rating remains high. The electrolytic capacitor bank typically applied across the dc bus is typically a weak link in the entire system, especially at high voltage levels, wherein series-connected capacitor banks would be necessary.

Alternatively, a current-source rectifier (CSR) with pulsewidth-modulation (PWM) capability can be used to achieve low input current THD, unity power factor, and dc power control simultaneously in a single power stage. A CSR using transistors is well known [3]–[5] and a schematic of the same is shown in Fig. 3. SCRs are replaced with IGBTs with series diodes to enable them to block reverse voltage when they are not conducting. The ac filter capacitors are present to circulate the switching current ripple. This is a buck-derived topology, which allows the dc-bus voltage to be controlled. However, the additional diode that is applied in series with the transistor essentially doubles the conduction losses in the converter, making this solution unattractive.

Hence, it is proposed to develop PWM control technology for thyristor-based rectifiers. Approaches to enable PWM capability in thyristor rectifiers have been presented in the past [6]–[11]. However, they have generally been complex in realization.

A PWM CSR topology using thyristors and capable of unity power factor, low-current THD, and dc-bus voltage control is presented in this paper. The topology is derived by a cascade connection of the classical thyristor rectifier and a buck dc–dc converter without any intermediate energy storage element. The topology utilizes a new active commutation technique, which allows the switching of the SCRs to be pulsewidth modulated.

The commutation technique being used in the topology was proposed in [12] which utilizes a series-connected gate-turn-off device with an SCR. This principle is extended here to provide

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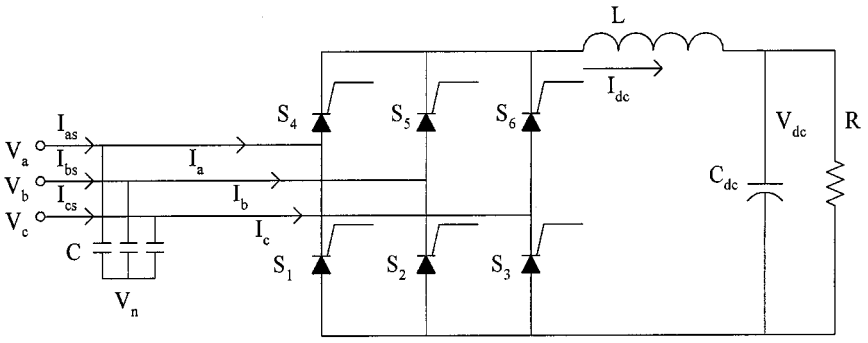

Fig. 1. Power circuit schematic of a phase-controlled SCR rectifier.

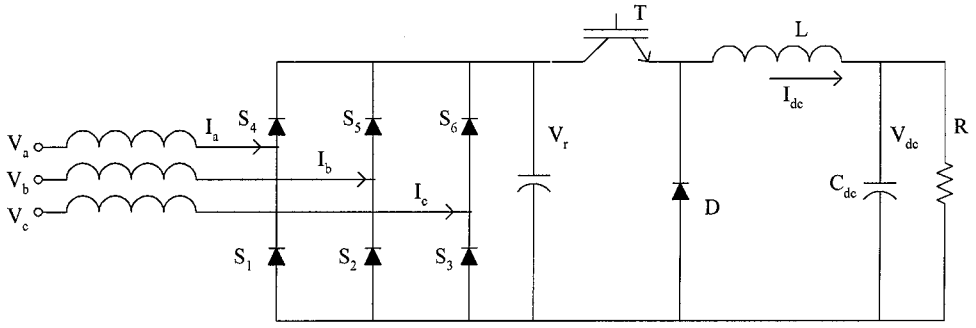

Fig. 2. Power circuit schematic of a diode rectifier with dc-side chopper.

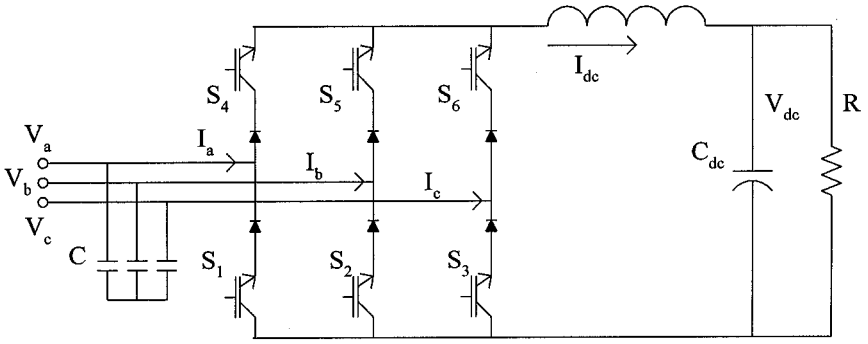

Fig. 3. Power circuit schematic of CSR with IGBTs.

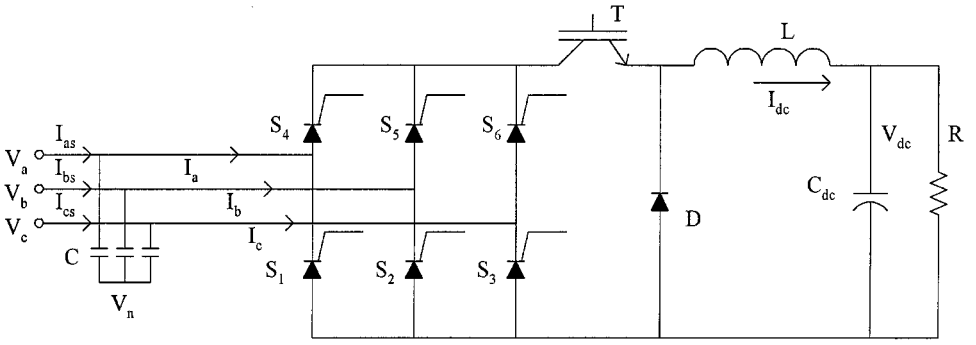

Fig. 4. Power circuit schematic of CSR with PWM capability using SCRs.

PWM capability for the classical six-pulse SCR rectifier. The schematic of the power circuit is illustrated in Fig. 4. The inductor that feeds the dc bus acts as a stiff current source. The converter consists of six thyristors as in a classical line-commutated rectifier, with the addition of a series IGBT (T) and freewheeling diode (D). These devices are employed to actively commutate the SCRs, thus enabling PWM operation.

The principles and limitations of active commutation of the SCR bridge using a dc-side switch are described and illustrated using experimental waveforms in Section II. In Section III, the

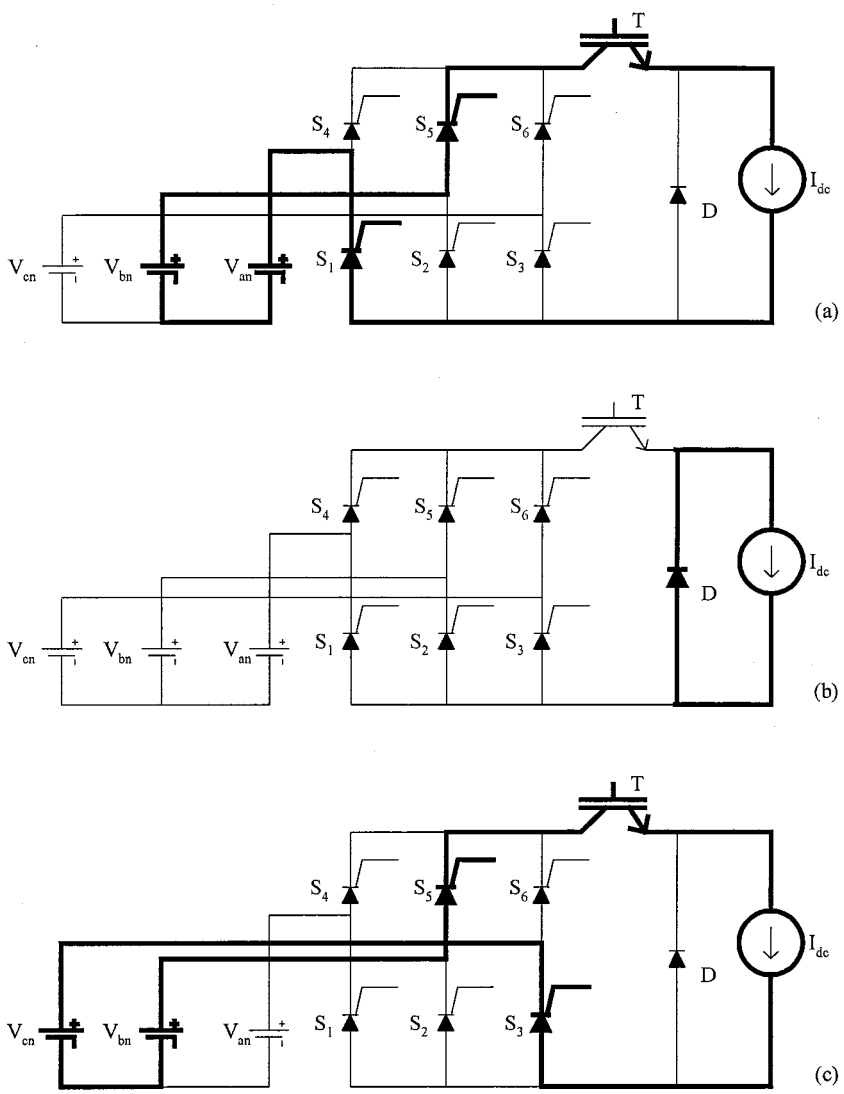

Fig. 5. Schematic of current flow during typical switching states and commutation modes.

analysis of converter operation using averaged switching functions is presented. Transfer properties relating the input and output variables with the duty ratio functions are developed. Section IV presents the modulation schemes for the proposed converter. Computer simulation results verifying the operation of the converter are presented in Section V, followed by a concluding discussion in Section VI.

II. Active Commutation

The operating modes of the converter are key to understanding the active commutation process. In addition, they highlight SCR switching characteristics that are important to ensure successful realization of the proposed technique. These topics and experimental results demonstrating the active commutation technique are discussed in this section.

A. Converter Operating Sequence

Fig. 5 may be used to follow the operating sequence of the converter including the active commutation technique. During the short interval of time of an operating sequence, the inductor may be replaced by a stiff current source and the ac inputs may be considered to be three dc voltage sources of different amplitudes. During the interval under consideration, the phase voltages V_{an} and V_{bn} are assumed to be positive and V_{cn} is assumed to be negative. The operating modes can be appropriately modified to fit other operating conditions.

When the IGBT T is closed, the converter operates as a classical CSR. In Fig. 5(a), the inductor current $I_{\rm dc}$ is drawn from one of the phases (V_{bn}) through one of the upper SCRs, S_5 and returns to a different phase (V_{an}) through one of the lower SCRs, S_1. During this time, the remaining four SCRs are off. If at some instant, T is turned off, the current flow from the source is interrupted and the inductor current will freewheel through diode D. This condition is illustrated in Fig. 5(b). As the conducting SCR current has been reduced to zero, it will turn off after the lapse of a delay period. This time is required for the stored charge to decay through recombination. Beyond this instant, the SCR will be off and able to block forward or reverse voltage. After this commutation interval, a new set of SCRs can be gated on. When T is turned back on, the freewheeling diode is commutated off and the dc current is sourced from a new phase and a

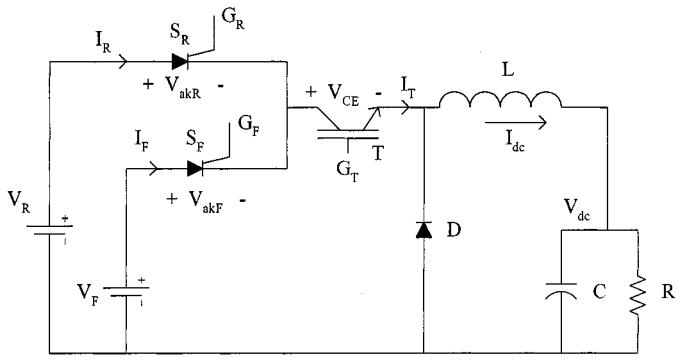

Fig. 6. Schematic of the test circuit used to characterize the commutation of SCRs.

new set of SCRs. This mode is shown in Fig. 5(c) with S_3 and S_5 conducting.

It is clear that the proposed commutation scheme can be successful as long as both the voltages V_{ba} and V_{bc} are positive. More importantly, there is no restriction of V_{ba} being greater than V_{bc} or otherwise, as long as they are both positive. It is also true that at any given instant of time, there are at least two line–line voltages that are positive. It is, hence, clear that the proposed active commutation technique can be used to control the input currents in a six-pulse converter to be sinusoidal. However, during normal operation, an SCR may be either forward biased or reverse biased during an OFF state, depending on the magnitude of the line-voltages.

For instance, in the commutation sequence that was just described, S_1 may be forward biased if $V_{ba} > V_{bc}$ or reversed biased if $V_{ba} < V_{bc}$.

The interval when T is off must be sufficient to allow the SCRs to regain blocking state through minority carrier recombination. This type of commutation of SCR is not common and deserves definitive investigation. A test circuit was designed and built to characterize switching behavior under this commutation technique.

B. Active Commutation Test Circuit

The test circuit, illustrated in Fig. 6, consists of a buck-type dc–dc converter operating from two input voltage sources. The input voltages are set at different levels to verify commutation under transitions between a reverse-biased and a forward-biased SCR, both back and forth. It may be observed that if $V_F > V_R$, S_R denotes the reversed-biased SCR while S_F denotes the forward-biased device. The buck switch T is modulated at 2.5 kHz with a fixed duty cycle of 75%. This results in a 100-μs period available for freewheeling, while the transistor T remains open. The SCR control was configured so S_R and S_F were triggered during alternating ON periods of T. The SCRs were gated on immediately prior to turning on T. Additionally S_R and S_F were modulated at the same duty cycle. The test conditions were $V_R = 112$ V; $V_F = 155$ V; $I_{\rm dc} = 12.5$; and $V_{\rm dc} = 100$ V.

The ideal waveforms for test circuit, over a complete switching cycle are illustrated in Fig. 7. Initially, both T and S_R are gated on, as reflected in the corresponding gate and device voltage waveforms (G_T, V_{ce}, G_R, and V_{akR}). The inductor current flows through T and S_R to the load as indicated by current waveforms I_T and I_R, respectively.

C. S_R to S_F Transition

Three events make up the transition between the reverse-biased SCR to the forward-biased SCR.

1) S_R OFF: While S_R and T are conducting the inductor current and the gate for S_R (G_R) has been removed, T is turned off. The current in T and S_R is reduced to zero, and the inductor current freewheels in D. The voltage across T, V_{ce}, immediately rises to V_R, while the voltage across V_{akR} remains zero. Thus, the switching loss in this commutation is borne by T.
2) S_R to S_F: After a delay period to ensure S_R is off, S_F is gated on. The voltage across T reflects that S_R is on, as V_{ce} rises to V_F. As V_F is larger than V_R, S_R is reversed biased at this time. This interval marks a potential commutation, as S_F has been gated but is yet to carry the inductor current. G_F remains high through the rest of the commutation interval.
3) S_F ON: T is gated on, resulting in S_F carrying the inductor current, turning off D. As I_F is exceeds the holding current, S_F may be considered to be on. The gate signal may be removed from S_F shortly thereafter, so as to prepare for the next transition.

The experimental waveforms for this transition are displayed in Fig. 8(a) and (b). The dynamic saturation of S_F is visible on V_{akF} waveform in Fig. 8(b).

D. S_F to S_R Transition

In similar manner, three events make up the transition between the forward-biased SCR to the reverse-biased SCR.

1) S_F OFF: T is turned off while S_F and T are conducting. The current in T and S_F is reduced to zero. V_{ce} rises to V_F, while the voltage across V_{akF} remains zero. The switching loss in this commutation is borne by T.
2) S_F to S_R: After a delay period to ensure S_F is off, S_R is gated on. The voltage across T reflects that S_R is on, as V_{ce} falls to V_R. As V_F is larger than V_R, S_F is forward biased at this time. This interval marks a potential commutation, as S_R has been gated but is yet to carry the inductor current. G_R remains high through the rest of the commutation interval.
3) S_R ON: T is gated on, resulting in S_R conducting the inductor current. As soon as I_R exceeds the holding current, S_R is considered on.

The experimental waveforms for this transition are displayed in Fig. 8(c) and (d).

The experimental results of both S_F to S_R transition and S_R to S_F transition indicate the viability of the proposed active commutation scheme for application in CSRs.

III. Converter Modeling

In this section, an averaged fundamental component model of the PWM CSR and the various duty ratio modulation functions are developed. The six SCRs and the buck switch modulate the

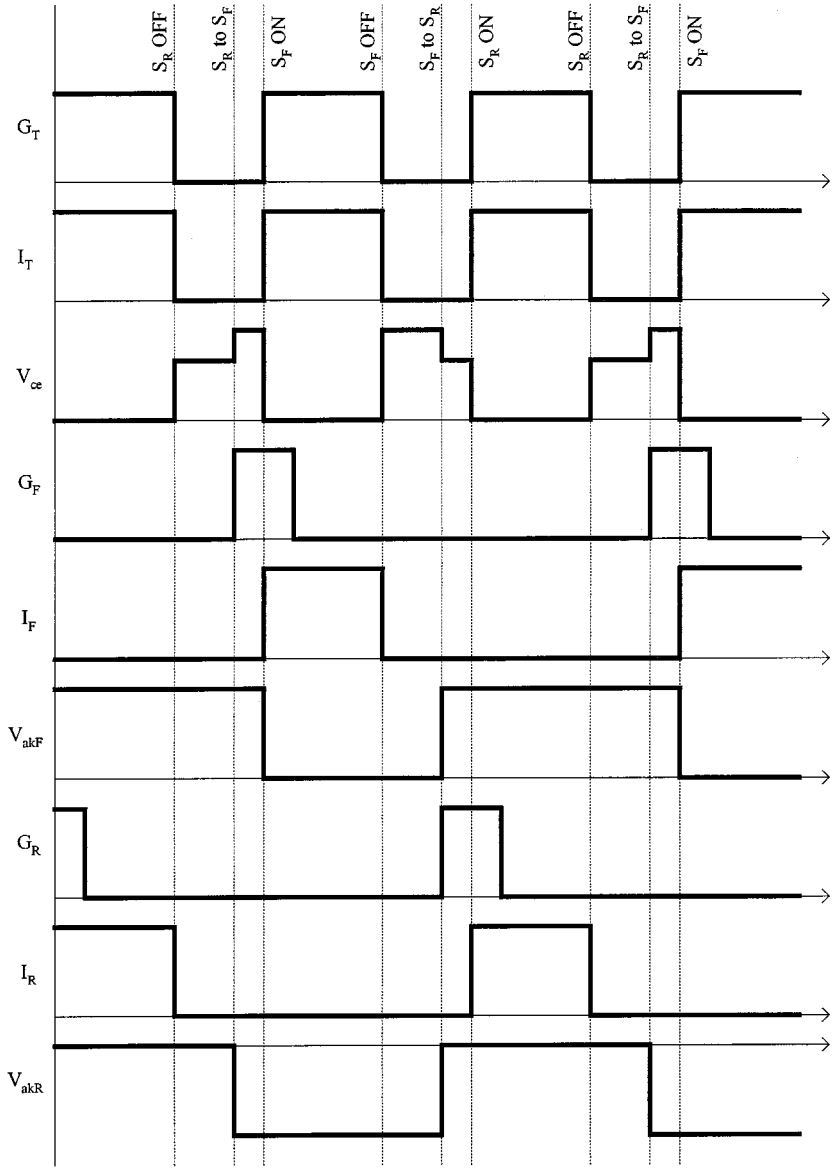

Fig. 7. Ideal test circuit waveforms for a complete switching cycle.

dc-link current into the source phases. The switching functions for these devices are designed so that the fundamental components of the phase currents approximate balanced three-phase sinusoids [13].

A. Fundamental Component Model

A simplified equivalent circuit of the buck-derived CSR with complete control capability can be represented by two single-pole quadruple-throw switches as illustrated in Fig. 9. Throws 1–6 represents the corresponding SC's S_1–S_6 and throw D represents the freewheeling diode D.

Let H_1–H_6 be the switching functions of the six SCR throws, and H_D be the switching function of D. Continuity of the inductor current can be explicitly constrained using the following relationships:

$$H_1 + H_2 + H_3 + H_D = 1 \tag{1}$$

$$H_4 + H_5 + H_6 + H_D = 1. \tag{2}$$

With the switching functions defined as above, the three phase source currents ($I_a - I_c$) can be represented in terms of the inductor current ($I_{\rm dc}$) as

$$\begin{aligned} I_a &= (H_1 - H_4) I_{\rm dc} \\ I_b &= (H_2 - H_5) I_{\rm dc} \\ I_c &= (H_3 - H_6) I_{\rm dc}. \end{aligned} \tag{3}$$

If the average values of the switching functions H_1–H_6 and H_D are given by their duty ratios D_1–D_6 and D_D, respectively, (3) can be represented as

$$\begin{aligned} I_a &= (D_1 - D_4) I_{\rm dc} \\ I_b &= (D_2 - D_5) I_{\rm dc} \\ I_c &= (D_3 - D_6) I_{\rm dc}. \end{aligned} \tag{4}$$

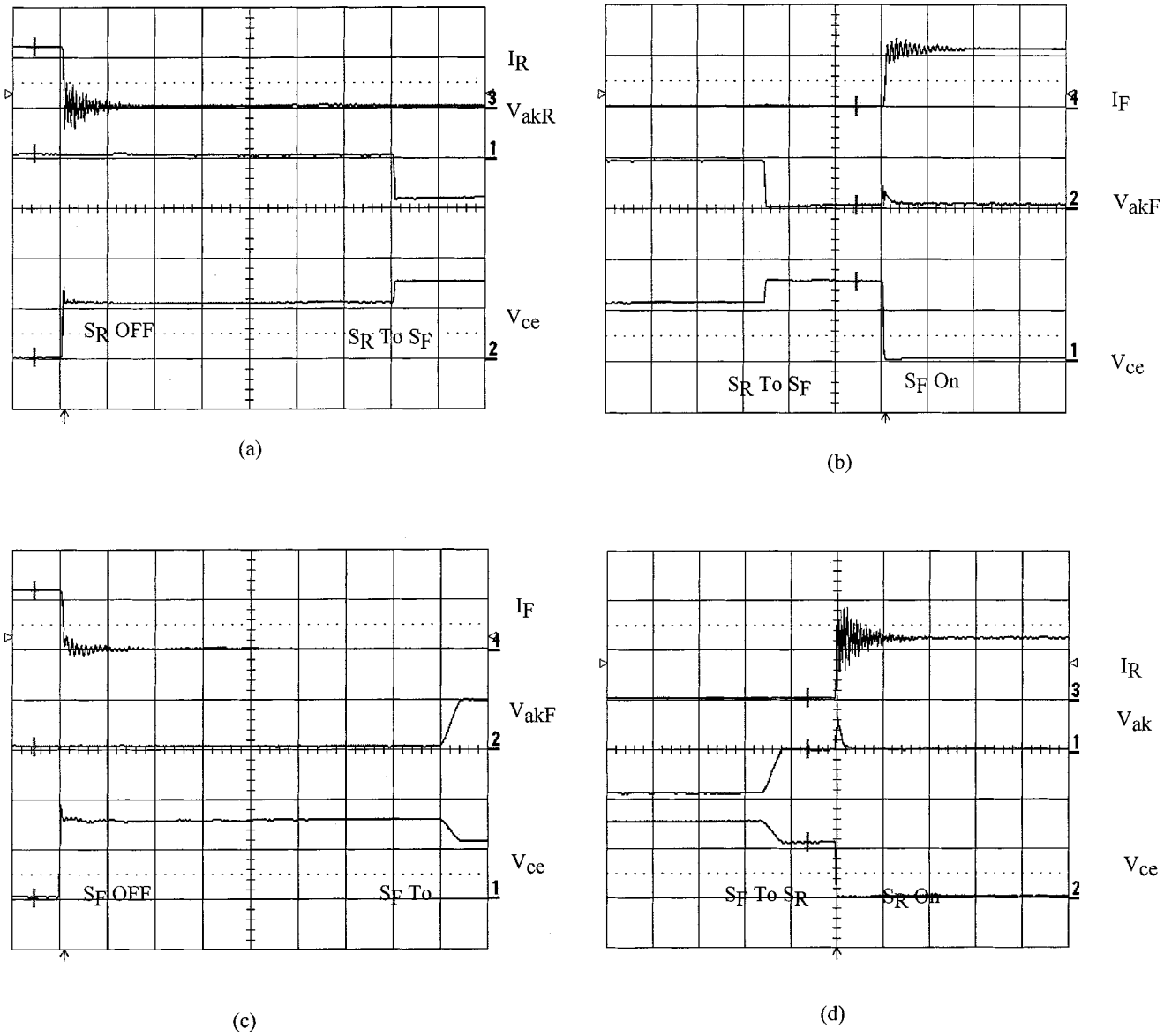

Fig. 8. (a) Traces of the S_R voltage and current, and IGBT voltage waveforms during a S_R to S_F transition: S_R OFF and S_R to S_F events I_R (10 A/div), V_{akR} (50 V/div), V_{ce} (100 V/div), 10 μs/div. (b) Traces of the S_F voltage and current, and IGBT voltage waveforms during a S_R to S_F transition: S_R to S_F and S_F ON events I_F (10 A/div), V_{akF} (50 V/div), V_{ce} (100 V/div), 10 μs/div. (c) Traces of the S_F voltage and current, and IGBT voltage waveforms during a S_F to S_R transition: S_F OFF and S_F to S_R events I_F (10 A/div), V_{akF} (50 V/div), V_{ce} (100 V/div), 10 μs/div. (d) Traces of the S_R voltage and current, and IGBT voltage waveforms during a S_F to S_R transition: S_F to S_R and S_R ON events I_R (10 A/div), V_{akR} (50 V/div), V_{ce} (100 V/div), 10 μs/div.

If effective duty ratios D_a, D_b, and D_c are defined as D_1–D_4, D_2–D_5, and D_3–D_6, respectively, the three phase currents may be derived to be

$$\begin{aligned} I_a &= D_a I_{\rm dc} \\ I_b &= D_b I_{\rm dc} \\ I_c &= D_c I_{\rm dc}. \end{aligned} \tag{5}$$

In order to synthesize sinusoidal source currents, the effective duty ratios D_a, D_b and D_c may be chosen to be a set of balanced sinusoidal functions at line frequency f, with an amplitude D_m. In that case, the phase currents become

$$\begin{aligned} I_a &= I_{\rm dc} D_m \cos(2\pi f t - \phi) \\ I_b &= I_{\rm dc} D_m \cos(2\pi f t - 120^\circ - \phi) \\ I_c &= I_{\rm dc} D_m \cos(2\pi f t + 120^\circ - \phi) \end{aligned} \tag{6}$$

which may be represented as three phasors, $Is\angle -\phi$, $I_s\angle -\phi - 120^\circ$, and $I_s\angle -\phi + 120^\circ$, where $\phi = 0$ for a unity-power-factor load.

For a balanced three-phase source, the line-to-neutral voltage phasors V_a, V_b, and V_c can be represented as $V_s\angle 0$, $V_s\angle(-120^\circ)$, and $V_s\angle(120^\circ)$, respectively. The instantaneous input power $P_{\rm in}$ is given by

$$P_{\rm in} = 3 V_s I_s \cos(\phi). \tag{7}$$

This is equal to the instantaneous output power $P_{\rm dc}$ drawn from the dc bus $V_{\rm dc}$, which can be expressed as

$$P_{\rm dc} = V_{\rm dc} I_{\rm dc}. \tag{8}$$

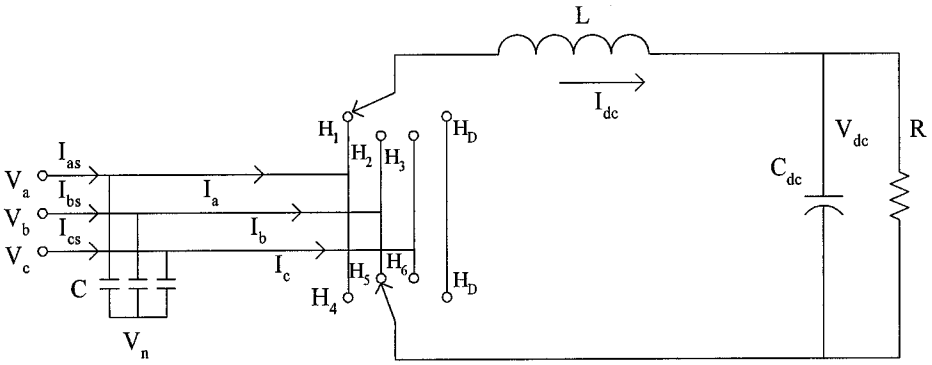

Fig. 9. Ideal switch equivalent circuit of the PWM CSR converter.

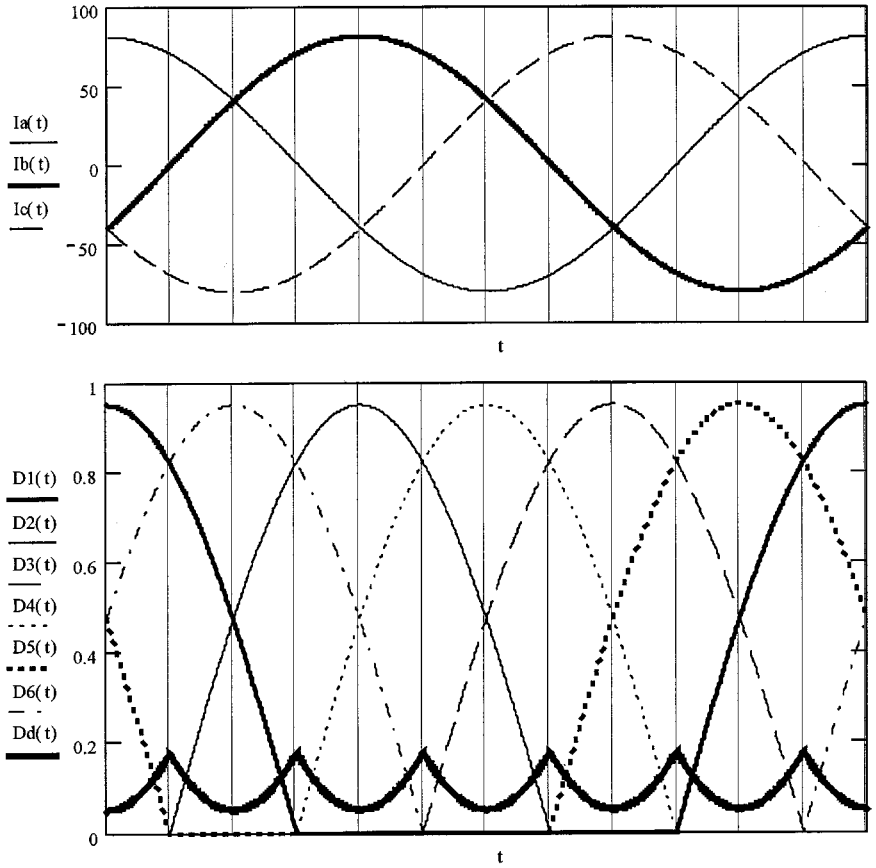

Fig. 10. Waveforms of three-phase current references and switch states for the buck rectifier.

Equating (7) and (8), a relationship between effective value of dc-bus voltage ($V_{\rm dc}$), line-to-neutral source voltage (V_s), power factor ($\cos\phi$), and the maximum value of the effective duty ratio (D_m) can be determined to be

$$V_{\rm dc} = \frac{3}{\sqrt{2}} V_s D_m \cos(\phi). \tag{9}$$

Thus, for a given input power factor, increasing the maximum effective duty ratio (D_m) leads to an increase in the output dc-bus voltage.

The maximum achievable dc-bus voltage, in terms of the peak value of the line-to-line voltage, is

$$V_{\rm dc} = \frac{\sqrt{3}}{2} V_{\rm peak(L\text{–}L)}. \tag{10}$$

For a comparison, a maximum voltage obtainable from a three-phase six-pulse thyristor rectifier (at $\alpha = 0$) is $3/\pi V_{\rm peak(L\text{–}L)}$. Of course, a diode bridge rectifier with a capacitive dc bus features a dc-bus voltage that is almost equal to $V_{\rm peak(L\text{–}L)}$. One may conclude that while a classical SCR is capable of developing about 95% of the peak value of the line–line voltage at the output terminals, the ideal CSR can

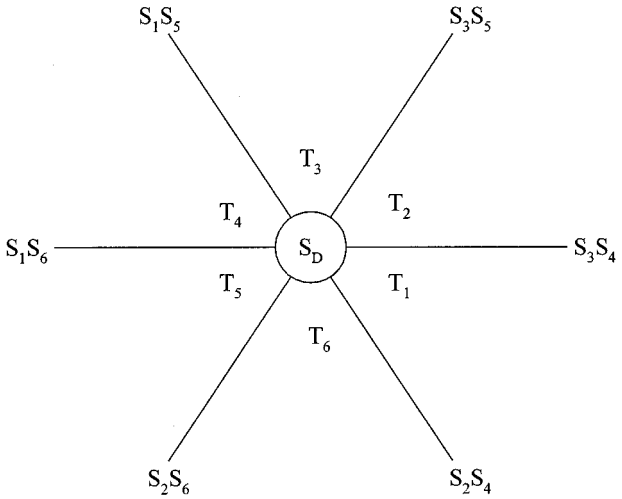

Fig. 11. Phase-plane illustration of the switching states of the PWM CSR.

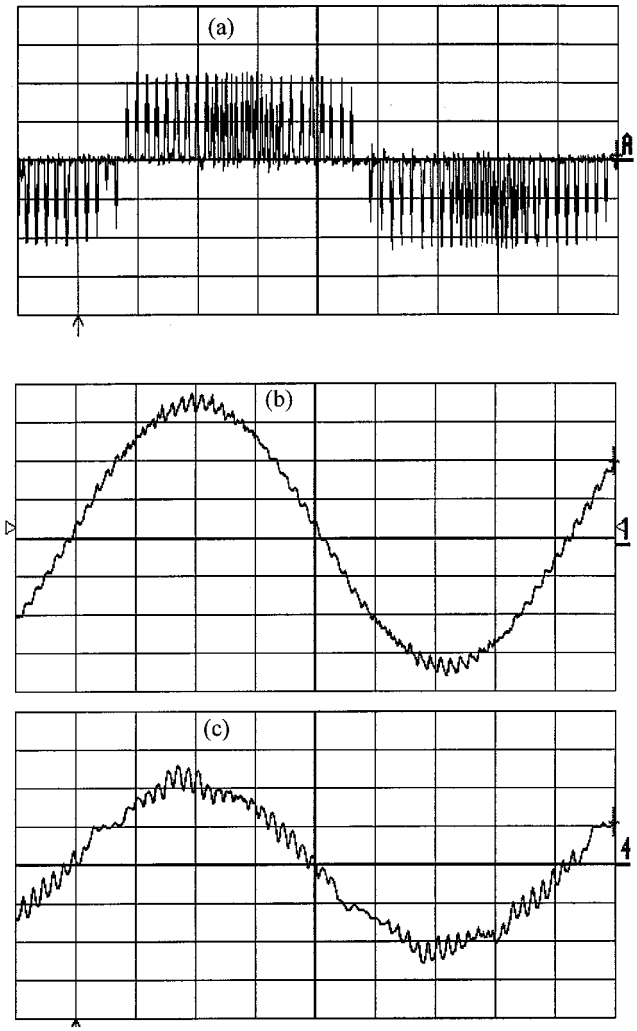

Fig. 12. Traces (2 ms/div) of (a) source voltage (V_{ab} at 50 V/div), (b) source current (I_a at 2 A/div), and (c) converter input current (I_a at 5 A/div).

develop only above 87% of the same. Furthermore, in a practical converter, minimum pulsewidth and SCR commutation period create an effective lost duty cycle, further reducing the maximum dc-bus voltage.

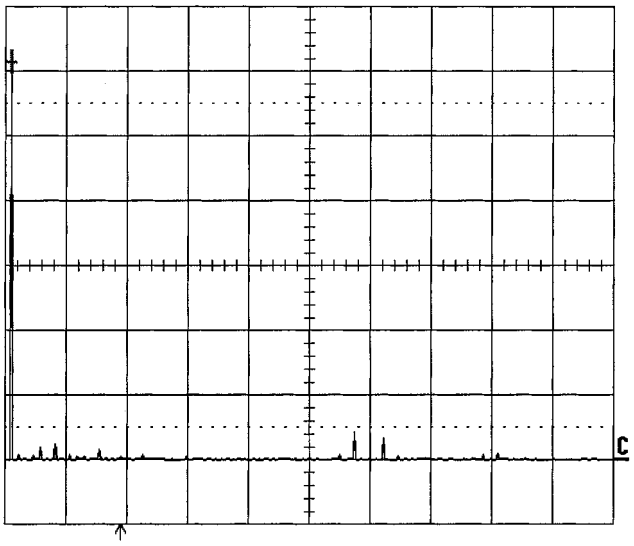

Fig. 13. Fourier spectrum (500 Hz/div) of converter input current I_{as} (0.7 A/div).

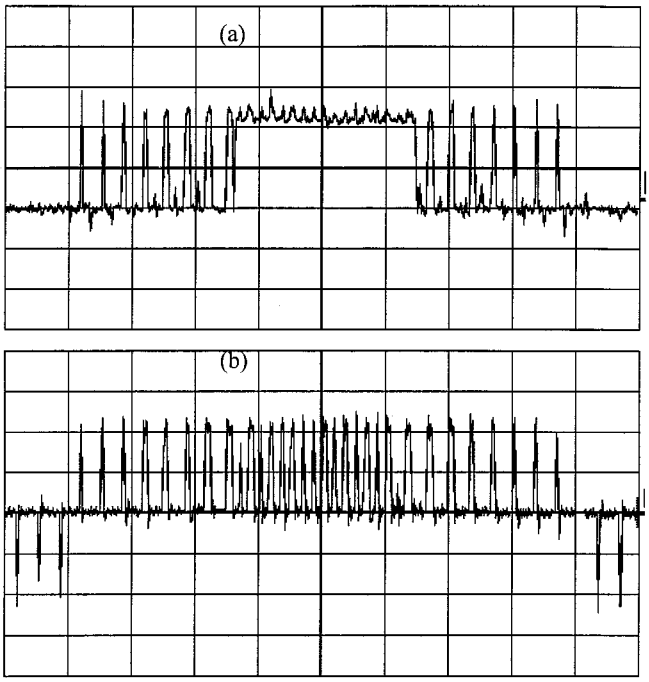

Fig. 14. Experimental waveforms of (a) S_4 gate voltage and (b) converter input current I_a during one-half of a fundamental period.

B. Modulation Functions

The effective duty cycle D_a, D_b, D_c can be decomposed into average SCR duty cycles D_1–D_6 as follows:

$$\begin{aligned} D_1 &= D_a u(D_a) \\ D_2 &= D_b u(D_b) \\ D_3 &= D_c u(D_c) \\ D_4 &= -D_a u(-D_a) \\ D_5 &= -D_b u(-D_b) \\ D_6 &= -D_c u(-D_c) \end{aligned} \tag{11}$$

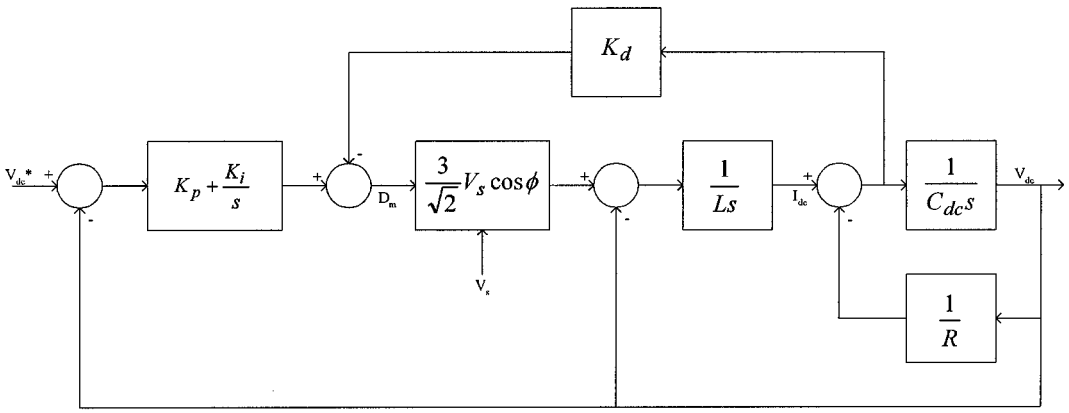

Fig. 15. Block diagram of a control for a regulated dc bus, power-factor-controlled rectifier.

where $u(.)$ is the unit step function. Furthermore, the average duty ratio D_D of the freewheeling diode is given by

$$D_D = 1 - (D_1 + D_2 + D_3). \tag{12}$$

Fig. 10 illustrates the three phase currents and the corresponding duty ratios as functions of time, for a D_m of 0.95.

IV. Realization of Modulator

The pulsewidth modulator forms the innermost loop of the PWM CSR. The modulator generates switch states for the six SCRs and the buck IGBT from balanced three-phase sinusoidal output current commands. The modulator employed for this converter is similar to the one developed for the actively commutated current-source inverter (CSI) [3], [4], [13]. Symmetry of the three phase waveforms permits the modulation technique to be developed for any 60° sector, and transposed accordingly.

When the reference waveform for a particular phase is within a 60° band centered at its peak, the corresponding SCR is maintained on throughout the interval. During the 60° interval that a given SCR is held on, the complementary SCR of the same phase has to be gated off to allow the inductor current to flow out to the source. Furthermore, at any given instant, only one of the high-side SCRs S_1, S_2, or S_3 and one of the low-side SCRs S_4, S_5, or S_6 can be turned on to avoid output line-to-line shorts. Hence, it is clear that once the SCR that is to be maintained on during a given 60° has been identified, it completely dictates the three other SCRs in the bridge that have to be off. The two remaining SCRs are now modulated to achieve the desired switching function.

The switching states of the CSR are summarized in Fig. 11. During any operating sector, the system chooses the three switching states that form the vertices thereof. For instance, during the segment T_3, the switching states chosen are S_2S_4, S_2S_6 and the S_T state. Every transition from S_2S_4 to S_2S_6 and vice-versa is forced to go through the S_D state. This strategy ensures successful active commutation of S_4 and S_6. The controlled switch T is turned off during the zero state.

V. Experimental and Simulation Results

A. Experimental Results

A prototype SCR was built and tested to verify the operation of the active commutation and modulation strategy. In addition, computer simulations were performed to demonstrate the input current and dc-bus voltage control capability of the converter.

A 208-V 1- kW version of the proposed converter, as shown in Fig. 3, was built and evaluated during steady-state operation with a resistive load. The parameters of circuit components were as follows:

$$L_s = 500\ \mu\text{H} \qquad C = 60\ \mu\text{F}$$
$$L_{\text{dc}} = 30\ \text{mH} \qquad C_{\text{dc}} = 12\ \text{mF} \qquad R = 4.3\ \Omega.$$

The modulation scheme presented in Section IV was implemented using sine-triangle comparison techniques and a field-programmable gate array (FPGA). Waveforms were captured while operating the converter with a carrier frequency of 3 kHz and an input ac line–line voltage of 120 V.

The steady-state waveforms at $V_{\text{dc}} = 44$ V are displayed in Fig. 12. The pulsewidth-modulated nature of the rectifier input current (I_a) is evident in Fig. 12(a), as is the ripple voltage across the input filter capacitor line–line voltage (V_{ab}) shown in Fig. 12(b). The resulting fundamental component of the line current (I_{as}) is sinusoidal. A Fourier spectrum of the converter input current (I_{as}) is shown in Fig. 13. As may be expected, the spectrum of the current has components at the fundamental frequency and at sidebands centered at the multiples of the carrier frequency.

Furthermore, the gate-drive voltage for device S_4 and the rectifier input current I_a are illustrated in Fig. 14. It may observed from the figure that, although S_4 is gated on continuously during the time when the voltage V_a is the most positive among the input phase voltages, the current I_a is pulsewidth modulated due to the switching of return current through S_2 or S_3, as the case may be.

B. Simulation Results

In order to demonstrate the dynamic performance of the converter, computer simulation of the converter incorporating a closed-loop regulator was performed. Although many loads in the metal industry are typically passive nonlinear loads, an equivalent resistive load was used in simulating the response of the system to a step change in the load. A 480-V 850-kW rectifier was simulated to operate at 5-kHz switching frequency.

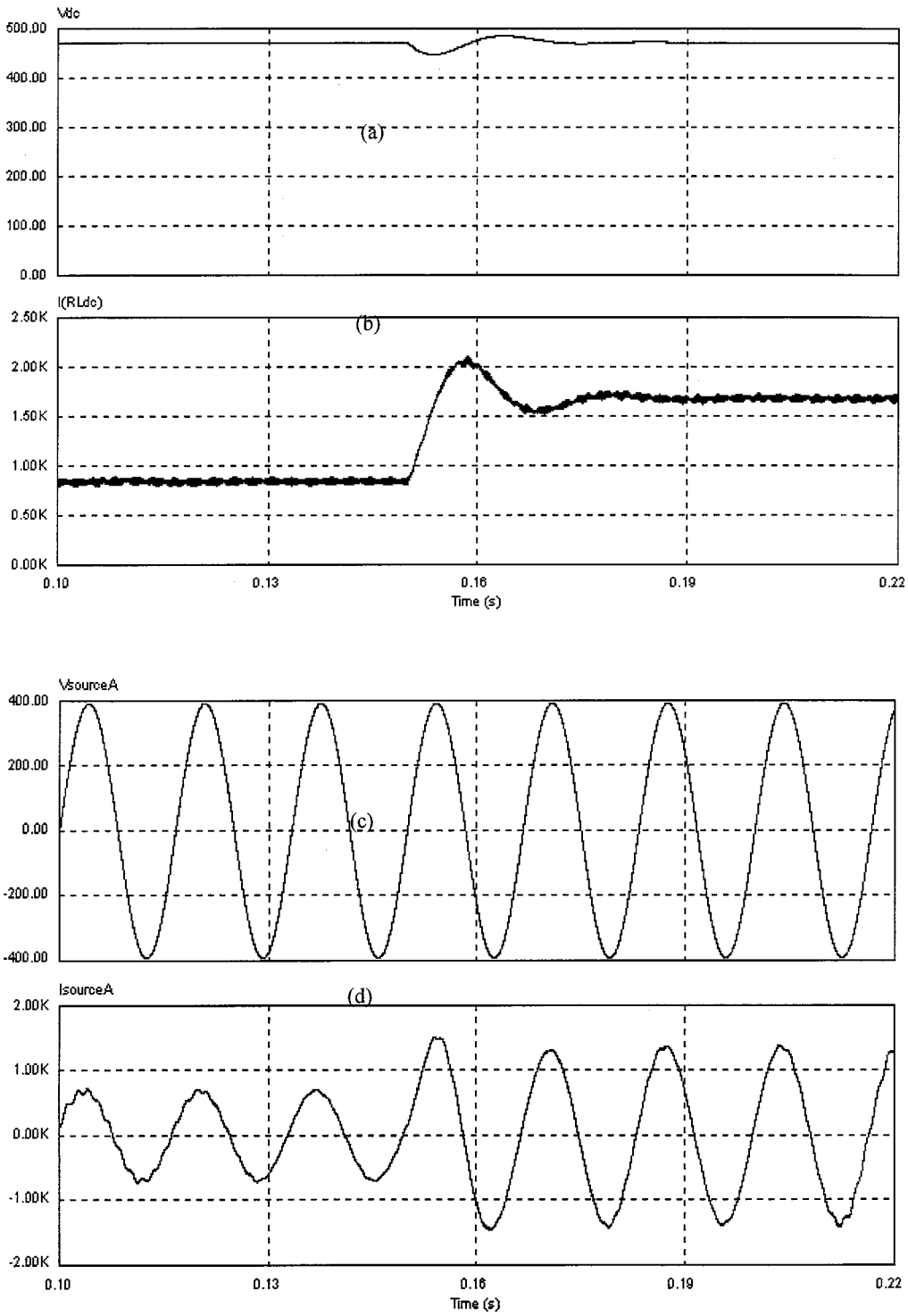

Fig. 16. Traces of dc-bus voltage ($V_{\rm dc}$), dc-bus current ($I_{\rm dc}$), source voltage (V_a), and source current (I_{as}) during a step change in load power from 0.5 to 1.0 p.u.

The per-unit parameters of the components used in the simulation of the circuit illustrated in Fig. 4 were as follow:

$X_{Ls} = 0.08$ p.u. $X_C = 22.2$ p.u.

$X_L = 0.5$ p.u. $X_{Cdc} = 0.1$ p.u. $R = 1.0$ p.u.

A closed-loop feedback controller was developed to regulate the dc-bus voltage. The control block diagram of the system is shown in Fig. 15. A proportional plus integral (PI) regulator with derivative feedback is used to regulate the dc-bus voltage. The dc-bus capacitor current feedback is used to provide the derivative feedback and, hence, dampen the dc filter resonance.

The dynamic performance of the converter to a step change in load demand of 0.5 p.u. is illustrated in Fig. 16. It may be seen that soon after the step change in load occurs, the dc-bus voltage drops and the increased demand in load current is sourced from the output capacitor. However, through feedback action the dc voltage is restored, and the voltage returns back to its nominal value.

The regulator may also be suitably adapted to perform load current regulation instead of voltage regulation. A detailed discussion of the design of the closed-loop regulator is beyond the scope of this paper, and will be discussed in an upcoming publication in the future.

VI. Conclusions

An SCR-based CSR with PWM capability has been presented in this paper. Its operation is based on an active commutation strategy. The feasibility of active commutation was demonstrated through an experimental test circuit, establishing the viability of the approach. One of the limitations of the active commutation strategy is the need for limiting the turn-on di/dt of the SCRs. Appropriate snubber circuits or soft-switching networks will have to be added to the power circuit to enable successful application of the converter at a high power level.

A modulation strategy for the converter that realizes sinusoidal input current waveforms has been presented. The modulation strategy has been verified using computer simulations. The operation of the converter with the proposed modulation strategy has been verified using a laboratory prototype. Furthermore, the operation of a closed-loop feedback controller was also demonstrated using simulations.

The closed-loop regulation can be extended to regulate the dc-bus current to fit the needs of the plant control. The dynamic performance of the system is fast enough to regulate flicker that may occur due to rapid load variations.

Some of the advantages of the proposed approach include the following:

- sinusoidal input current waveforms;
- utilizes low-cost and rugged SCRs;
- dc-bus regulation with power-factor control;
- suitable for high-power applications;
- line current regulation will produce balanced input currents;
- built-in inrush current limiting;
- only one additional gate-turn-off device used to achieve PWM of SCRs.

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