Inverter Nonlinearity Effects in High-Frequency Signal-Injection-Based Sensorless Control Methods

Juan Manuel Guerrero, *Member, IEEE*, Michael Leetmaa, *Student Member, IEEE*, Fernando Briz, *Member, IEEE*, Antonio Zamarrón, and Robert D. Lorenz, *Fellow, IEEE*

***Abstract*—An analysis of pulsewidth-modulation inverter nonlinearities influencing high-frequency carrier-signal voltage injection for saliency-tracking-based rotor/flux position estimation is presented in this paper. Distortion of the injected carrier voltage caused by the nonlinear behavior of the inverter has been reported to cause errors in the estimated rotor/flux position. Though a number of techniques have been developed to compensate for inverter nonlinearities, they have not been proven to be effective when a high-frequency low-magnitude voltage needs to be generated. Both the origins of the distortion as well as the requirements for compensation methods to be effective when producing such high-frequency voltages will be established in this paper.**

***Index Terms*—Deadtime, pulsewidth modulation (PWM), saliency, sensorless.**

I. Introduction

A NUMBER of sensorless control techniques have been developed in the past two decades [1]–[8]. The aim of these techniques is to accurately control the electrical machine without any mechanical position or speed sensor. There are two main groups of estimation methods: those which rely on the back-electromotive-force (EMF) voltage associated with fundamental component excitation of the machine [1], [2], [8] and those which use a second excitation signal, in addition to the fundamental excitation [1]–[7]. Estimators based on the back EMF have been shown to be successful at medium and high rotor speeds; however, they fail at very low speed due to the small magnitude and low frequency of the back-EMF signals. To overcome this limitation, methods which inject an additional signal have been proposed. In this paper, the injection of a high-frequency rotating voltage vector for saliency position estimation will be analyzed. Errors in voltage production, due to inverter nonideal behavior (mainly deadtime), can cause a significant distortion of the injected high-frequency voltage, eventually giving rise to significant estimation errors in the saliency position. There are a number of solutions for compensating for the inverter deadtime effect and other inverter nonlinearities when injecting fundamental voltage to the machine [9]–[26]. Recently, some compensation methods for high-frequency carrier-signal generation have been reported [5], [6]; but the origins of the distortions seen in the high-frequency signal current have not been rigorously documented. In this paper, the effect of inverter nonlinearities on the injected high-frequency carrier voltage will be documented and its causes explained in detail. Results obtained through simulation and experiments will be presented.

Paper IPCSD-04-066, presented at the 2003 Industry Applications Society Annual Meeting, Salt Lake City, UT, October 12–16, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Drives Committee of the IEEE Industry Applications Society. Manuscript submitted for review August 1, 2003 and released for publication November 22, 2004. This work was supported in part by the Research, Technological Development and Innovation Programs of the Principado of Asturias under Grant PB-EXP01-24 and Grant PB02-055, in part by the Spanish Ministry of Science and Technology-ERDF under Grant DPI2001-3815, and in part by the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC) of the University of Wisconsin, Madison.

J. M. Guerrero and F. Briz are with the Department of Electrical, Computer and Systems Engineering, University of Oviedo, Gijón 33204, Spain (e-mail: guerrero@isa.uniovi.es).

M. Leetmaa is with the Department of Mechanical Engineering, University of Wisconsin, Madison, WI 53706 USA (e-mail: leetmaa@cae.wisc.edu).

A. Zamarrón is with the Department of Mechanical and Electrical Engineering, Technological Institute of León, León, México.

R. D. Lorenz is with the Department of of Mechanical Engineering and the Department of Electrical and Computer Engineering, University of Wisconsin, Madison, WI 53706 USA (e-mail: lorenz@engr.wisc.edu).

Digital Object Identifier 10.1109/TIA.2005.844411

II. Carrier-Signal Injection Methods

The use of a high-frequency rotating voltage or current vector superimposed on the fundamental excitation, and the analysis of the resulting high-frequency current (or voltage) to track spatial saliencies has been widely studied as a viable option to estimate the rotor or flux position [3]–[7]. When a high-frequency rotating voltage vector is injected (1), if the machine contains rotor-position-dependent saliencies (asymmetries), their angle will be embedded in the negative-sequence component of the high-frequency current (2)

$$v^s_{qds\_c} = V_c e^{j\omega} c^t \tag{1}$$

$$i^s_{qds\_c} = i^s_{qds\_cp} + i^s_{qds\_cn} = -jI_{cp}e^{j\omega}c^t + jI_{cn}e^{(h\theta_r - j\omega_c t)}. \tag{2}$$

A tracking observer, such as that presented in [3], extracts the position estimate with zero-lag filtering of unwanted noise. Fig. 1 shows the process of injecting a high-frequency signal and the extraction of the current components. One of the major limitations of carrier-signal-injection-based techniques is unwanted distortion of the negative-sequence carrier-signal current caused by unmodeled or incorrectly modeled secondary saliencies, mostly saturation induced, which can result in noticeable rotor position estimation errors, and even in instability problems. When multiple saliencies are to be tracked, precise

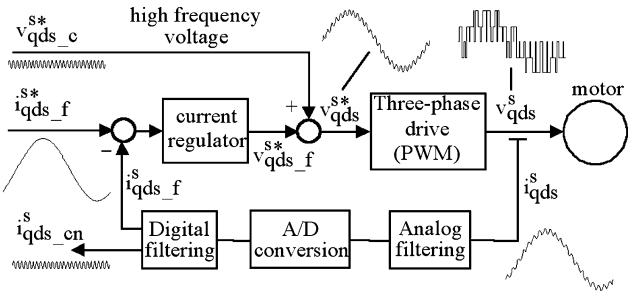

Fig. 1. Injection of a high-frequency voltage and extraction of current components.

knowledge of their origin and behavior is needed to extract the position of each one [4], [5], [7]. A second source of distortion of the negative-sequence carrier-signal current is the distortion of the injected carrier voltage caused by the pulsewidth-modulation (PWM) inverter nonlinearities, which will also produce additional components of the negative-sequence carrier-signal current corrupting the signal containing information related to the position of the rotor and/or flux.

III. Inverter Nonideal Behavior Effects in High-Frequency Signal Injection

Distortion of the negative-sequence carrier-signal current containing the rotor position information can be caused by unmodeled saliencies or by distortion in the injected high-frequency voltage. Such distortion can cause errors in the estimated position.

In [4]–[6], distortion in the negative-sequence carrier-signal current was shown in the time domain when the phase currents crossed zero. As this distortion was not observed when a linear inverter was used to supply the motor, and it increased with deadtime, it was attributed to inverter deadtime in [4]. Some of the results of [4] are reproduced in Fig. 2. Fig. 2(a) shows the phase current after the carrier signal has been removed. No distortion is observed in these currents even though no deadtime compensation was used in the current regulators. The negative-sequence carrier signals, shown in the negative-sequence carrier-signal current reference frame, for 2 and 4 μs deadtime, are shown in Fig. 2(b) and (c), respectively. Significant distortion is evident in the negative-sequence carrier-signal reference frame when any of the phase currents cross zero. In addition, the detrimental effect of increasing deadtime is also clear.

The same effect was observed in [5]. In that case, the high-frequency voltage was measured, and distortion was observed in the high-frequency injected voltage with respect to its commanded value whenever the phase current crossed zero. Inverter clamping is the name used for that type of inverter nonlinearity, which was attributed in [15] to variations in switch turn-on and turn-off times at low current levels. A method for compensating this distortion, named space modulation profiling, was proposed in [5], based on a torque- and flux-dependent two-dimensional lookup table. Moreover, no deadtime effect was observed when fundamental current was not injected.

Improvements in rotor position estimation were investigated in [6] for the case of surface-mounted permanent-magnet machines (SMPMs), using different deadtime compensation

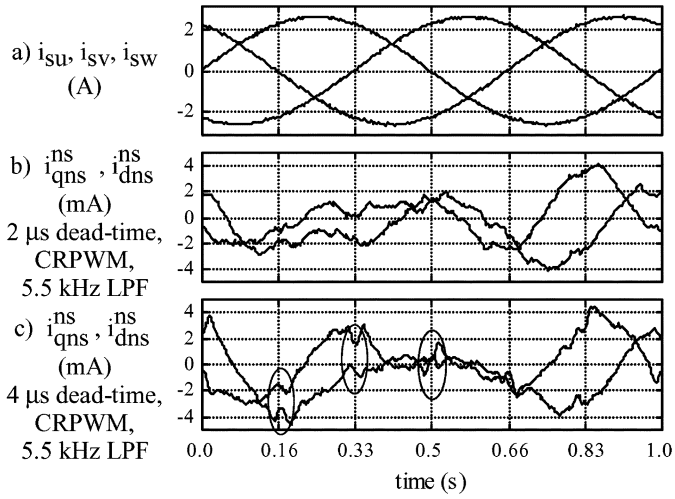

Fig. 2. (a) Phase currents (after filtering off the carrier-signal current) and (b), (c) negative-sequence carrier-signal current components for two different values of the deadtime in the inverter, shown in the negative-sequence carrier-signal reference frame. A 0.75-kW induction motor was operated with constant excitation and rotor speed frequencies of $\omega_e = 1$ Hz and $\omega_r = 1.5$ Hz, a fundamental current of $|i_{qds}| = 2.64$ A, and a carrier voltage of $V_c = 7$ V. A current-regulated pulsewidth-modulated inverter with a switching frequency of 15 kHz, and carrier frequency of 535 Hz was used. (a) i_{su}, i_{sv}, i_{sw} (A). (b) $i^{ns}_{qns}, i^{ns}_{dns}$, (mA) 2 μs deadtime, CRPWM, 5.5-kHz LPF. (c) $i^{ns}_{qns}, i^{ns}_{dns}$ (mA) 4 μs deadtime, CRPWM, 5.5–kHz LPF.

methods. The same distortion as in [4], [5] was observed in the high-frequency output voltages and currents when the phase currents crossed zero. Using the fundamental component compensation method of [18], reduction in the high-frequency distortion was not achieved. In contrast, a significant improvement in position estimation was reported when using the deadtime compensation method proposed in [16].

IV. Inverter Voltage Error Mechanisms

Several inverter nonlinearities caused by the nonideal behavior of the switching devices have been studied, and different compensation methods reported [8]–[27]. The most relevant nonlinearities are the following.

- Deadtime, also known as shoot-through delay [15], [23], dwell time, or interlock time [10], is described in [9]–[26]. Deadtime is needed to prevent the dc link from being short circuited when the two devices of a leg of the inverter are switched. Its effects can be seen in Fig. 3. When the switch state of a leg changes, a delay time must be given for the switch initially *on* to turn *off* before the other switch is turned *on*. During that time, both switches are off, the states reflected in Fig. 4(c) and (d). This delay time generates short voltage error pulses of a constant amplitude and width in the output voltage of one inverter leg, with respect to the commanded voltage value. The sign of the error pulse is the opposite of the current polarity in that leg.
- Turn-on and turn-off times of the IGBT's are the time that the switch takes to turn *on* or *off* (fully conduct or fully block the current, respectively) from when it is commanded to do so. Some of the proposed compensation methods for deadtime include solutions for this problem

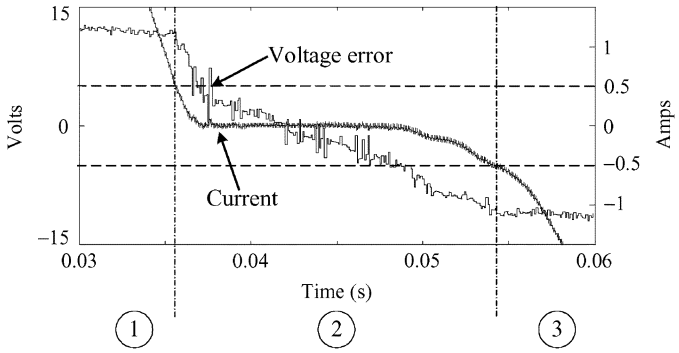

Fig. 3. Simulation. Phase current and voltage error (3). $|v^*| = 27$ V ω_e Hz. No carrier signal. An *RL* load is used. $R = 0.82\ \Omega$ $L = 5.5$ mH. Deadtime: $T_d = 2\ \mu$s. Switching time: $T_{PWM} = 100\ \mu$s. Simulation step: $T_s = 90$ ns.

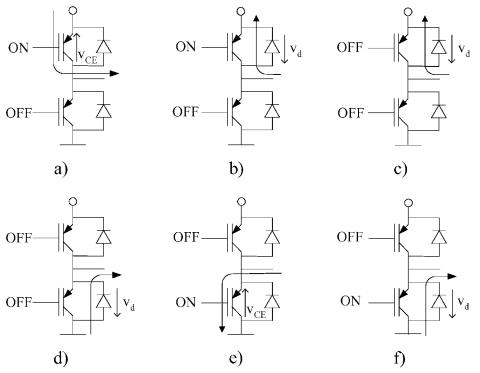

Fig. 4. Possible instantaneous output voltages depending on the current direction and switching state, (a) $V_{\rm out} = V_{\rm DC} - v_{CE}$. (b) $V_{\rm out} = V_{\rm DC} + v_d$. (c) $V_{\rm out} = V_{\rm DC} + v_d$. (d) $V_{\rm out} = -v_d$. (e) $V_{\rm out} = v_{CE}$, (f) $V_{\rm out} = -v_d$.

[18], [23], [25], though in other cases its effects are neglected [10].

- Parasitic capacitance of semiconductors causes changes in the slope of the rising and falling edges of the output voltage when the current is very small due to the fact that the current charges up the parasitic capacitance of the diodes [14] or switches [15] prior to flowing through the diode. Turn-on and turn-off times are also affected by these capacitances in such a way that switching times and parasitic capacitances combine to produce a unique distortion effect in the output voltage in the low-current region.
- Zero-current clamping occurs when a phase current nears zero during the deadtime [13], [14], [21], [25], [26], and is caused first by the extinction of the current in the freewheeling diode, resulting in the phase leg being disconnected from the bus during a portion of the deadtime period, and second, by the larger commutation times at low current levels due to the nonideal nature (parasitic capacitance) of the diodes [14]. This is especially important for low-frequency signals, which remain in the zero-current-clamping region much longer [13].
- Voltage drops in the semiconductors (i.e., insulated gate bipolar transistors (IGBTs) and diodes) are another source of error in the injected voltage. They can be modeled as a constant voltage plus an equivalent resistor and compensated by using models [8], [18], [25] or lookup tables [23].
- Short pulse suppression appears when the commanded pulse is shorter than the deadtime [17]. This is not generally an issue in self-sensing methods, as they are typically only employed at low speeds where modulation indexes are far from the inverter voltage limit.
- Reference [27] adds contributions to voltage distortion from power board components, long cables, and ac motors.

All these issues related to PWM generation have been studied from the point of view of power transmission; however, a better understanding is still needed of their relative importance when high-frequency signal injection is used for saliency tracking purposes.

The influence of the previous inverter modulation error sources on the carrier-signal distortion were studied with the aid of detailed SABER simulations. A three-phase inverter feeding an *R–L* load ($R = 0.82\ \Omega, L = 5.5$ mH) was used for simulation purposes; experimental results with an induction motor are presented in a later section.

Fig. 3 shows the voltage error (3) (voltage reference, V^*, minus average output voltage per switching period, $V_{\rm avg}$) and the current when a fundamental voltage reference of 27 V and 4 Hz is commanded to the inverter. A deadtime of 2 μs, and models for irg4ph40u IGBT and hfa15tb60 diode were used. Three different zones are apparent in the plot. The error in zones 1 and 3 corresponds to the well-known deadtime effect, being nearly constant and a function of the current polarity. This error can be calculated using (4)

$$V_{\rm error} = V^* - V_{\rm avg} \tag{3}$$

$$\begin{aligned} V_{\rm error} &= V_{\rm dc}\frac{T_d}{T_s} + v_{ce}\frac{T_{\rm on} - T_d}{T_s} \\ &\quad - v_d\frac{T_{\rm off} + T_d}{T_s}, \qquad i > 0 \\ V_{\rm error} &= -V_{\rm dc}\frac{T_d}{T_s} - v_d\frac{T_{\rm on} + T_d}{T_s} \\ &\quad - v_{ce}\frac{T_{\rm off} - T_d}{T_s}, \qquad i < 0 \end{aligned} \tag{4}$$

where T_s is the switching time period; $T_{\rm on}$ is the on-state time of one single inverter leg; $T_{\rm off}$ is the corresponding off-state time; T_d is the deadtime given to avoid shoot-through; $V_{\rm dc}$ is the dc-link voltage; v_d is the diode forward voltage drop; and v_{ce} is the collector-to-emitter voltage drop in the IGBT. Voltage drop in the semiconductors are often modeled as a constant voltage plus a resistor [8], [18]. Though the voltage drop is often negligible when compared with $V_{\rm dc}$, it can become significant for high-power devices; in those cases the resistance can be assumed to be part of the stator resistance [8]. In most cases, using the first term of the summations in (4) gives a good prediction of the deadtime effect error (offset error). This statement becomes more significant with increased dc-link voltages. The number of terms in (4) is augmented if the rise and fall times of the IGBTs are considered [18], [23], [25]. Rise and fall times increase with current magnitude. Rise time is often small compared to fall time, the difference being almost constant [18]. The different flow paths for current are shown depending on the switching

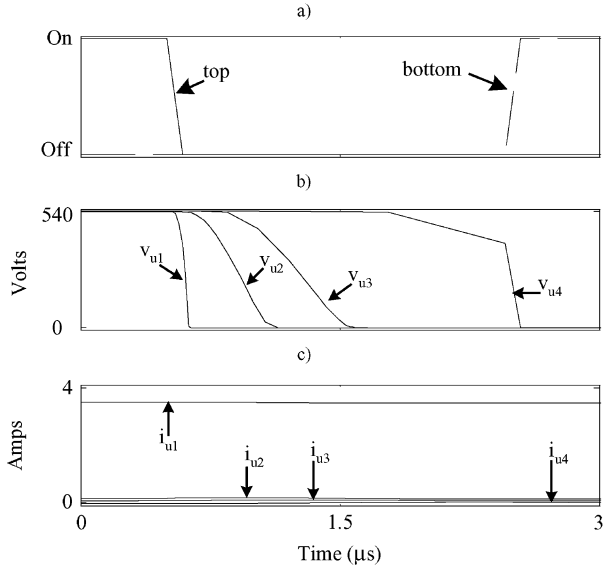

Fig. 5. Simulation. Inverter leg output voltage during deadtime for different current levels. Simulation conditions as stated in Fig. 3. (a) IGBT gate signals: solid line = top IGBT; dashed line = bottom IGBT. (b) Output voltage for different current levels. (c) Phase current.

state of the IGBTs in Fig. 4. Using this graph, the errors given by (4) are easily obtained. If the current is positive (i.e., flowing from the inverter to the motor), during the *on* state the instantaneous output voltage in the inverter leg will be that in Fig. 4(a). During the deadtime, Fig. 4(d) shows the path for the current. Finally, during the *off* state, the output voltage will be that in Fig. 4(f). When current is large enough in any direction, the transition between the three different states is very fast and only minor differences are observed due to rise and fall times.

In zone 2 of Fig. 3 the voltage error does not follow the expression given in (1). Beyond a certain magnitude of the current, approximately 0.5 A in Fig. 3, the parasitic capacitance of the diodes [14] and/or IGBTs [15] and the turn-off time of the IGBTs play a fundamental role in the modulation. This effect is seen in Fig. 5. In Fig. 5, output voltage v_{u1} corresponds to region 1 of Fig. 3 where the current is higher than approximately 0.5 A. For that case, the top IGBT turns off with some delay; the bottom diode is quickly reversed and the voltage rapidly decreases to zero. For v_{u2}, the current magnitude is smaller, and the voltage decay is slower. In v_{u3} and v_{u4}, a lower current stresses this behavior. In the limit, when current is zero, voltage stays high until the bottom IGBT turns on.

Two regions are easily seen in the output voltages of Fig. 5 once the top IGBT gate signal is turned *off*. The first region has a delay in which the voltage stays high. A lower current increases this delay. The second region starts when voltage slope rapidly changes. A lower current decreases this slope. A similar behavior, but with raising voltage slopes, is seen when the bottom IGBT is turned *off*.

This makes the voltage error decrease. In [15], it was stated that the rate of change of voltage and, thus, the voltage error, is inversely proportional to the capacitance and directly proportional to the current. In [16], a linear model describing the voltage error as a function of the current was introduced for low values of current. This will be explained next in detail.

In [28], the turn-off process was modeled in three time intervals: a *delay time* period, a *fall time*, and a so-called *tail time* interval. During the delay time, the current remains flowing through the IGBT; during the fall time, current is transferred to parasitic capacitor; this period increases the total turn-off time for larger current levels. Beyond a threshold current limit (tail current level), the current decreases more slowly due to device internal construction.

The IGBT turn-off process is always referred to as *current* extinction, while collector-to-emitter voltage and, consequently, output voltage, will depend on the application. In three-phase inverters, the process in the low-current region is the following:

- During the delay time, the output voltage keeps constant. This time will be similar for the relevant small current levels.
- During the fall time, current is transferred from the switch to the parasitic capacitances, both from the top and bottom devices. The voltage rate of change in the output will depend on the current level and the capacitance, and it will be the same (except for the sign) for the collector-to-emitter voltage of the top and the bottom IGBTs (5)

$$\frac{dV}{dt} = \frac{i_{\mathrm{TOP}}}{C_{\mathrm{TOP}}} \qquad \frac{dV}{dt} = \frac{i_{\mathrm{BOT}}}{C_{\mathrm{BOT}}} \tag{5}$$

where $i_{\mathrm{TOP}}, i_{\mathrm{BOT}}$ is the current flowing through the top or bottom capacitances, and C_{TOP} and C_{BOT} are the top and bottom capacitances. The total current will be that flowing through the switch and the parasitic capacitances (6)

$$i = i_{sw} + i_{\mathrm{BOT}} + i_{\mathrm{TOP}}. \tag{6}$$

The IGBTs parasitic capacitances decrease with increased collector-to-emitter voltage [29].

At the beginning of current transfer to the capacitances, the collector-to-emitter voltage in the top IGBT is low. This makes this capacitance dominant and most of the current will be transferred to it and, thus, the voltage derivative will be low. The output voltage will remain constant at the dc-bus voltage.

When the collector-to-emitter voltage increases in the top IGBT, its capacitance decreases abruptly in a nonlinear fashion. At this point, both top and bottom capacitances take a similar magnitude and the voltage derivative increases. This corresponds to the end of the delay and the beginning of the nearly linear voltage fall. Low currents, therefore, will increase the delay in the voltage fall and, in addition, diminish its slope.

The current level at which the error decreases will depend on the stray capacitances of the devices. Different current limits have been found using different IGBT models.

The current-clamping effect is also apparent in zone 2 of Fig. 3 at low current levels. In [13] and [16], this effect is attributed to the extinction of the diode current. In this case, the voltage in the inverter leg output becomes uncontrolled and it is governed by the back-EMF voltage. A second explanation, given in [16], is the parasitic capacitances explained in the previous paragraph, which apparently agree with the simulations

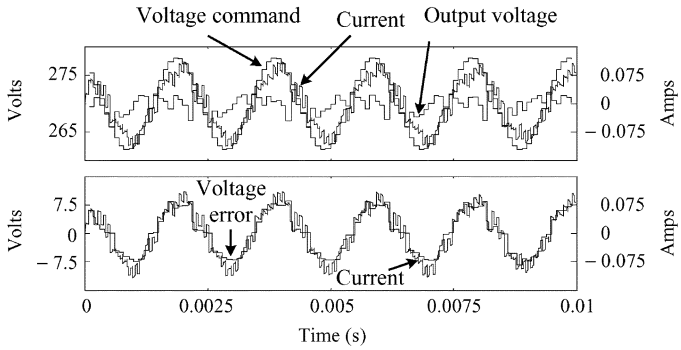

Fig. 6. Simulation. Injection of a high-frequency voltage. Top: voltage command, current, and output voltage. Bottom: voltage error and current. $|v_c| = 8.1$ V. , $\omega_c = 500$ Hz. No fundamental. An *RL* load is used. $R = 0.82\ \Omega$ $L = 5.5$ mH. Deadtime: $T_d = 2\ \mu$s. Switching time: $T_{\rm PWM} = 100\ \mu$s. Simulation step: $T_s = 90$ ns.

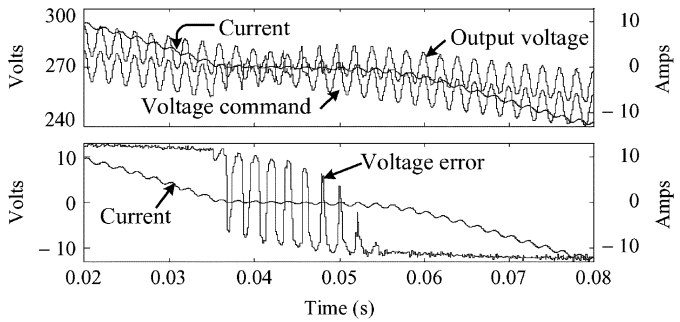

Fig. 7. Simulation. Injection of fundamental and high-frequency voltage. Top: voltage command, current, and output voltage. Bottom: voltage error and current. $|v^*| = 27$ V. $\omega_e = 4$ Hz. $|v_c| = 8.1$ V. $\omega_c = 500$ Hz. A RL load is used. $R = 0.82\ \Omega$ $L = 5.5$ mH. Deadtime: $T_d = 2\ \mu$s. Switching time: $T_{\rm PWM} = 100\ \mu$s. Simulation step: $T_s = 90$ ns.

carried out. In the first case, there is always a path for small currents through the parasitic capacitances, so that blocking of the current is prevented. In Fig. 5, phase current i_{u4} crosses zero during deadtime. This clamping effect will not be seen in high-frequency voltages.

V. High-Frequency Carrier Voltage Distortion Caused by the Nonideal Behavior of the Inverter

In this section, the origin of the distortions seen in the negative-sequence carrier-signal current reported in [4]–[6] is explained. Fig. 6 shows a simulated waveform of the currents and voltages when a carrier voltage is injected, with no fundamental voltage. Because of the low amplitude and relative high frequency of the injected carrier voltage, the resulting high-frequency current is within the range of zone 2 of Fig. 3. The voltage error waveform is of the same frequency and in phase with the high-frequency current. Hence, the output voltage is a waveform at the same frequency as the commanded voltage but with a different amplitude and phase. The frequency of the current remains unaltered, and because the high-frequency injection is open loop, there is no apparent distortion of the type reported in [5]. It should also be noted in Fig. 6 that no clamping is produced when the high-frequency current crosses zero.

Fig. 7 shows a simulation in which both fundamental (open loop) and carrier voltages are commanded. When the current magnitude is large enough (at the beginning and the end of the plot) the voltage error remains approximately constant, only a small variation due to the resistive component of the semiconductors being observed. When the phase current crosses the band where the parasitic capacitance of the semiconductors influence the output voltage, the voltage error is modulated at the carrier-signal frequency. The distortion seen in the carrier signal in [4]–[6] is then explained as follows. When the current is large enough (above approximately 0.5 A in Fig. 7), there is no relative distortion in the high-frequency voltage. When the fundamental current approaches zero, the carrier-signal current is modulated by a voltage error at the carrier frequency, causing a decrease in the carrier current magnitude and a phase lag. Current regulators, if they exist, will cancel the zero-current clamping making current cross zero faster and, therefore, the distortion will be shorter in time. It is noticeable that current clamping appears in Fig. 7 for fundamental current, although instantaneous current is continuously crossing zero. This is not in agreement with the explanation of current blocking when current goes to zero during the deadtime.

From this analysis, it can be concluded that most of the conventional compensation methods will fail to prevent the nonideal behavior of the inverter from causing a distortion of the injected high-frequency voltage when phase currents are nearly zero, with the exception of the method in [16] which takes into account the parasitic capacitances in compensating for clamping in phase currents. This would explain the improvement seen in [6] when using that method. Two software-based solutions are proposed in [16] for the zero-current-clamping region. The first one estimates the point at which current crosses zero and the back-EMF voltage and calculates a compensation voltage based on the motor model. The second solution uses a linear model of the voltage error once the current goes beyond a threshold level to compensate for it. Nevertheless, the proposed model for current regions close to zero is too simple according to the explanation given in Section IV, and it will be discussed in detail in Section VII.

VI. Experimental Results

Simulation results presented so far were experimentally confirmed in a test rig consisting of a three-phase inverter, using Semikron SKM 50GB123D IGBT modules driving a 0.75-kW induction motor. Semikron SKHI 22 A drivers were used to generate gate signals. Control of the inverter was implemented in a dSpace DS1102 DSP board. Custom printed circuit boards (PCBs) were designed for interfacing and current sensing. A second inverter with different IGBTs is used for comparison.

Fig. 8 shows the change in the falling slope of one inverter leg output voltage during the deadtime for different current levels. This behavior is in agreement with the simulation in Fig. 5.

A similar process is followed by the rising output voltage, in Fig. 9, for negative current levels. From Figs. 8 and 9, it can be concluded that the voltage error in the low-current region will be almost symmetric for negative and positive currents.

According to this behavior, the voltage error is only dependent on the current level for a given device. To demonstrate this statement, Fig. 10 shows a comparison for two different cur-

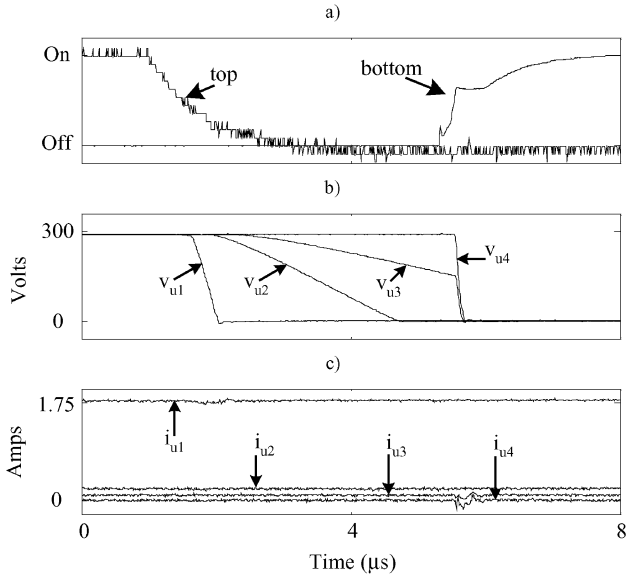

Fig. 8. Experimentally measured. Output voltage falling edges, during deadtime, with different current levels. Deadtime: $T_d = 4.8\ \mu$s. Switching time: $T_{\rm PWM} = 200\ \mu$s. Sampling time: $T_s = 10$ ns. (a) IGBT gate signals: smooth line = bottom IGBT; quantized line = top IGBT. (b) Output voltage for different current levels. (c) Phase current.

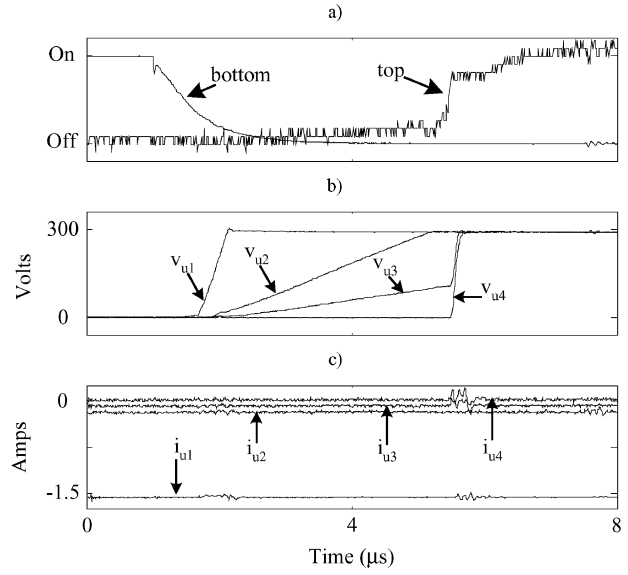

Fig. 9. Experimentally measured. Output voltage rising edges, during deadtime, for different current levels. Deadtime: $T_d = 4.8\ \mu$s. Switching time: $T_{\rm PWM} = 200\ \mu$s. Sampling time: $T_s = 10$ ns. (a) IGBT gate signals: smooth line = bottom IGBT; quantized line = top IGBT. , (b) output voltage for different current levels. (c) Phase current.

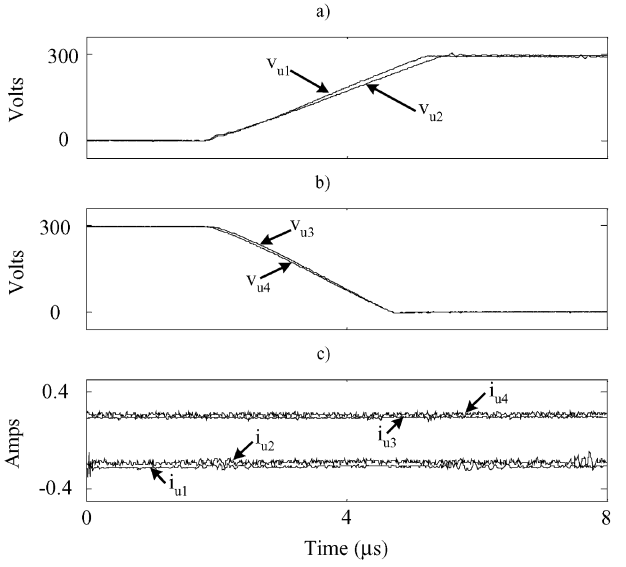

Fig. 10. Experimentally measured. Output voltage, during deadtime, for different injection conditions and similar current levels. Deadtime: $T_d = 4.8\ \mu$s. Switching time: $T_{\rm PWM} = 200\ \mu$s. Sampling time: $T_s = 10$ ns. (a) Output voltage for similar negative current levels. Rising edges. $V_{u1} : V_f = 50$ V. $\omega_f = 5$ Hz//$V_{u2} : V_f = 45$ V. $\omega_f = 5$ Hz + $V_c = 20$ V. $\omega_c = 500$ Hz. (b) Output voltage for similar positive current levels. Falling edges. $V_{u3} : V_f = 50$ V. $\omega_f = 5$ Hz//$V_{u4} : V_f = 45$ V. $\omega_f = 5$ Hz + $V_c = 20$ V. $\omega_c = 500$ Hz. (c) Phase current.

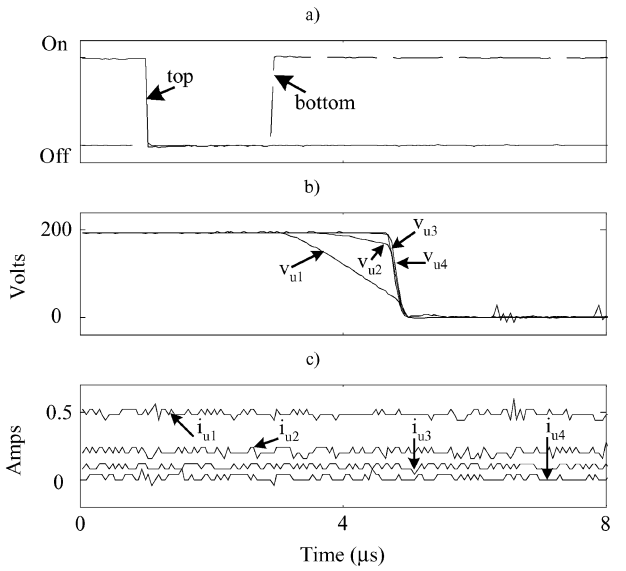

Fig. 11. Experimentally measured. Output voltage falling edges, during deadtime, with different current levels. Deadtime: $T_d = 2\ \mu$s. Switching time: $T_{\rm PWM} = 66.6\ \mu$s. Sampling time: $T_s = 50$ ns. (a) IGBT command signals: solid line = top IGBT; dashed line = bottom IGBT. (b) Output voltage for different current levels. (c) Phase current.

rent levels with two different voltage commands. In Fig. 10(a), output voltage rising edges are shown with similar negative current magnitude. In Fig. 10(b), the same experiment is carried out for falling edges and a positive current magnitude. In both cases, similar voltage slopes are, respectively, observed.

Similar tests were conducted using a second inverter, dc-bus voltage of 200 V, and a deadtime of 2 μs. Fig. 11 shows the results. Though similar to those obtained with the first inverter, some differences are observed. For the second inverter, the gate signals were not available, so command signals to the IGBT drivers are sampled instead. This explains the extended delay seen in the output voltage, which can be considered another source of error [27]. For that inverter, the bottom IGBT will switch *on* before the slope of voltage had changed for very low currents. Thus, there will be an extended zone around 0 A in which the error will be nearly zero. In Fig. 12(b), v_{u3} and v_{u4} are equal in practice, whereas their current magnitudes are different.

Fig. 12 shows the injection of a fundamental and carrier voltage. The voltage error changes depending on the current

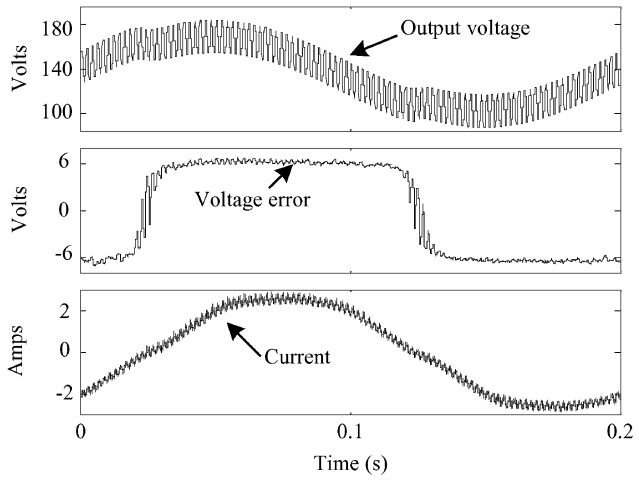

Fig. 12. Experimentally measured. Injection of fundamental and carrier voltage. $V_f = 45$ V. $\omega_f = 5$ Hz + $V_c = 20$ V. $\omega_c = 500$ Hz. Deadtime: $T_d = 4.8\,\mu$s. Switching time: $T_{\rm PWM} = 200\,\mu$s. Sampling time: $T_s = 200$ ns.

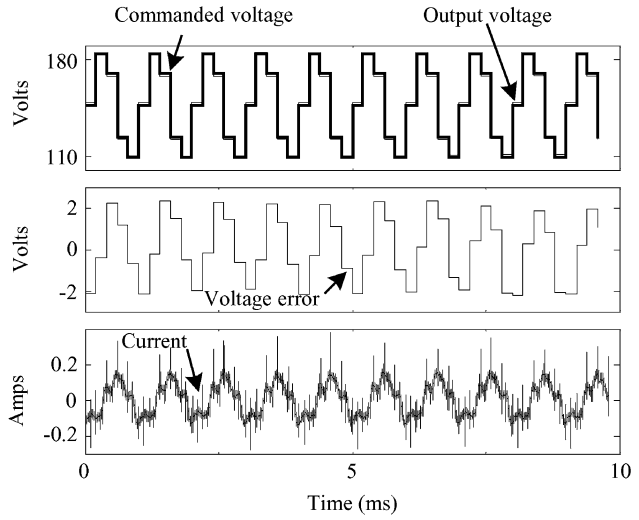

Fig. 13. Experimentally measured. Injection of a high-frequency carrier signal. $|v_c| = 20$ V. $\omega_c = 1000$ Hz. No fundamental. Deadtime: $T_d = 4.8\,\mu$s. Switching time: $T_{\rm PWM} = 200\,\mu$s. Sampling time: $T_s = 10$ ns.

level. For high positive or negative current this error is an offset. In this period no voltage error is introduced in the carrier signal, and conventional compensation methods could compensate for that error. When current approaches zero, a modulation of the error is produced and a more precise compensation is required. This agrees with the simulation in Fig. 7.

Figs. 13 and 14 show the injection of a carrier-signal voltage at 1000 and 500 Hz, respectively. To obtain carrier currents of about 100-mA peak, carrier voltages of 20- and 40-V peak were used. In this case, the error produced does not distort the voltage to the same degree as in the simulation of Fig. 6, due to the voltage command being much larger in order to obtain a similar current level. The voltage distortion is relatively larger for slower frequencies (Fig. 14) as smaller voltage command amplitudes are used in order to keep an adequate volts/hertz magnitude.

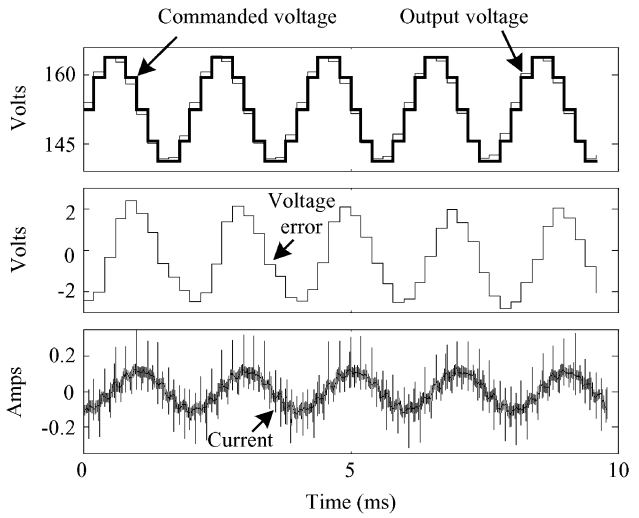

Fig. 14. Experimentally measured. Injection of a high-frequency carrier signal. $|v_c| = 20$ V. $\omega_c = 500$ Hz. No fundamental. Deadtime: $T_d = 4.8\,\mu$s. Switching time: $T_{\rm PWM} = 200\,\mu$s. Sampling time: $T_s = 10$ ns.

VII. Development of Deadtime Compensation Methods

From the previous analysis, the expected performance of already existing methods to compensate for the inverter nonideal behavior, as well as the required properties for new methods that could be developed, can be derived.

Most of the described methods [9]–[15], [17]–[26] do not take into account changes in the output voltage slope during deadtime in the low-current region. Thus, these methods are not expected to improve the carrier-signal generation.

In [16], two approaches are investigated for deadtime compensation in the zero-current-clamping or low-current region. The first one is based on the assumption that current is clamped to zero when it crosses zero during the deadtime. Improvements in rotor position estimation using this compensation method are reported in [6].

The second approach is based on the fact that the actual voltage switching depends on the current magnitude due to device parasitic capacitances. This method realizes that, from a certain current threshold level, the voltage error is a function of the current. The compensation strategy is based on a current-dependent voltage error linear function, used from the threshold level. In [6], it is not clarified if the first method is complemented with this approximation, though only the first method is explained.

Zero-current clamping has not been seen as the origin of the distortions, either for the case when only the carrier voltage is injected or for when both carrier and fundamental voltages are injected. Accordingly, efforts in its compensation are not expected to noticeably reduce the distortion of the carrier-signal voltage reported.

It has been shown that the output voltage slope during the deadtime and, thus, the voltage error, depend on the current. For a given switching period, the error will depend on the current level in *both edges* of the voltage pulse. During most of the switching periods, the current will not cross zero and only the current magnitude in the falling edge will be required for positive values of the current, or, in the rising edge for negative

values of the current. When the current crosses zero, both levels will be very close to zero if the switching frequency is large enough, which will be the case in modern drives. In this case, the voltage slope in both edges will be, in practice, the same as with zero current; this is especially true with small deadtimes, as for the case shown in Fig. 11.

From these observations, it can be concluded that the second method proposed in [16] is a good candidate for compensating distortion in the carrier signal, although some additional improvements are also proposed as follows.

The voltage error linear model should be changed to a nonlinear analytical function depending on the current level, the dc-bus voltage magnitude, the deadtime, and the power device characteristics. Alternatively, a lookup table could be used only for the current region affected by parasitic capacitances.

Current prediction should be focused on the beginning or end of the pulse depending on the sign of the current. If a change of polarity is detected in a switching period, no compensation would be required. According to the simulations and experiments, the current remains almost constant during the deadtime. Thus, its prediction during that period of time is required.

The improved method has not yet been implemented. The most significant difficulties are expected in current sensing and in its prediction, which is a common issue in all deadtime compensation methods, although most of them only require polarity determination.

VIII. Conclusion

High-frequency carrier-signal injection commonly used for zero-frequency sensorless control is an open-loop process that will require precise voltage generation. The fundamental component current regulator will minimize the distortion seen in the fundamental voltage, but not in the carrier voltage.

Errors in the injected high-frequency voltage will exist when inverter nonlinearities are not taken into account. Furthermore, such errors can produce fictitious saliencies, i.e., components of the negative-sequence carrier-signal current whose physical origin is not a saliency in the machine and which could eventually cause incorrect modeling of saturation-induced saliencies.

A detailed analysis of the inverter nonideal characteristics, which have an impact on the carrier signal, has been presented. The effect of parasitic capacitances of the power devices during the deadtime has been found to be the main contributor to carrier-signal distortion. This effect is seen as a nonlinear voltage error modulation in phase with the phase current for low-magnitude currents. It is caused by the different charging times of the parasitic capacitances depending on the current magnitude.

From this study, requirements for deadtime compensation methods suitable for high-frequency carrier-signal voltage injection have been derived. Most conventional compensation methods are believed to fail to compensate for carrier-signal distortion as they do not take into account, or neglect, the effect of parasitic capacitances. The method in [16] approximates the required solution although possible improvements are proposed based on a nonlinear model of the voltage error or by using an appropriate lookup table.

References

[1] J. Holtz, "Sensorless control of induction motor drives," *Proc. IEEE*, vol. 90, no. 8, pp. 1359–1394, Aug. 2002.

[2] P. Vas, *Sensorless Vector and Direct Torque Control*. Oxford, U.K.: Oxford Univ. Press, 1998.

[3] P. L. Jansen and R. D. Lorenz, "Transducerless position and velocity estimation in induction and salient AC machines," *IEEE Trans. Ind. Appl.*, vol. 31, no. 2, pp. 240–247, Mar./Apr. 1995.

[4] F. Briz, M. W. Degner, J. M. Guerrero, A. Zamarrón, and R. D. Lorenz, "Implementation issues affecting the performance of carrier signal injection based sensorless controlled AC drives," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Chicago, IL, 2001, pp. 2645–2652.

[5] N. Teske, G. M. Asher, K. J. Bradley, and M. Sumner, "Analysis and suppression of inverter clamping saliency in sensorless position controlled induction machine drives," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Chicago, IL, 2001, pp. 2129–2137.

[6] C. Silva, G. M. Asher, and M. Sumner, "Influence of dead-time compensation on rotor position estimation in surface mounted PM machines using HF voltage injection," in *Proc. IEEE Power Conversion Conf.*, Osaka, Japan, 2002, pp. 1279–1284.

[7] M. W. Degner and R. D. Lorenz, "Using multiple saliencies for the estimation of flux, position, and velocity in AC machines," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1097–1104, Sep./Oct. 1998.

[8] J. Holtz and J. Quan, "Sensorless vector control of induction motors at very low speed using a inverter model and parameter identification," *IEEE Trans. Ind. Appl.*, vol. 38, no. 4, pp. 1087–1095, Jul./Aug. 2002.

[9] Y. Murai, T. Watanabe, and H. Iwasaki, "Waveform distortion and correction circuit for PWM inverters with switching lag-times," *IEEE Trans. Ind. Appl.*, vol. 23, no. 5, pp. 881–886, Sep./Oct. 1987.

[10] R. C. Dodson, P. D. Evans, H. T. Yazdi, and S. C. Harley, "Compensating for dead time degradation of PWM inverter waveforms," *Proc. Inst. Elect. Eng.*, pt. B, vol. 137, no. 2, pp. 73–81, Mar. 1990.

[11] T. Sukegawa, K. Kamiyama, K. Mizuno, T. Matsui, and T. Okuyama, "Fully digital, vector controlled PWM VSI-fed AC drives with an inverter dead-time compensation strategy," *IEEE Trans. Ind. Appl.*, vol. 27, no. 3, pp. 552–559, May/Jun. 1991.

[12] Y. Wang and H. Grotstollen, "Control strategies for the discontinuous current mode of AC drives with PWM inverters," in *Proc. European Power Electronics Conf.*, Florence, Italy, 1991, pp. 217–222.

[13] Y. Murai, A. Riyanto, H. Nakamura, and K. Matsui, "PWM strategy for high frequency carrier inverters eliminating current-clamps during switching dead-time," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Houston, TX, 1992, pp. 317–322.

[14] J. W. Choi and S. K. Sul, "New dead time compensation eliminating zero current clamping in voltage-fed PWM inverter," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Denver, CO, 1994, pp. 977–984.

[15] R. B. Sepe and J. H. Lang, "Inverter nonlinearities and discrete-time vector current control," *IEEE Trans. Ind. Appl.*, vol. 30, no. 1, pp. 62–70, Jan./Feb. 1994.

[16] J.-W. Choi, "A new compensation strategy reducing voltage/current distortion in PWM VSI systems operating with low output voltages," *IEEE Trans. Ind. Appl.*, vol. 31, no. 5, pp. 1001–1008, Sep./Oct. 1995.

[17] W. S. Oh, Y. T. Kim, and H. J. Kim, "Dead time compensation of current controlled inverter using space vector modulation method," in *Proc. Int. Conf. Power Electronics and Drive Systems*, Singapore, 1995, pp. 374–378.

[18] J. W. Choi, S. I. Yong, and S. K. Sul, "Inverter output voltage synthesis using novel dead time compensation," *IEEE Trans. Power Electron.*, vol. 11, no. 2, pp. 221–227, Mar. 1996.

[19] C. B. Jacobina, A. M. N. Lima, and A. C. Oliveira, "Enhanced PWM voltage waveform and dead-time compensation for AC drive systems," in *Proc. IEEE IECON'97*, New Orleans, LA, 1997, pp. 694–697.

[20] D. Leggate and R. J. Kerkman, "Pulse-based dead-time compensator for PWM voltage inverters," *IEEE Trans. Ind. Electron.*, vol. 44, no. 2, pp. 191–197, Apr. 1997.

[21] L. Ben-Brahim, "The analysis and compensation of dead-time effects in three phase PWM inverters," in *Proc. IEEE IECON'98*, Aachen, Germany, 1998, pp. 792–797.

[22] Y.-H. Liu and C.-L. Chen, "Novel dead time compensation method for induction motor drives using space vector modulation," in *Proc. IEE—Elect. Power Appl.*, vol. 145, Jul. 1998, pp. 387–392.

[23] A. R. Muñoz and T. Lipo, "On-line dead-time compensation technique for open-loop PWM-VSI drives," *IEEE Trans. Power Electron.*, vol. 14, no. 4, pp. 683–689, Jul. 1999.

[24] C. Attaianese and G. Tomasso, "Predictive compensation of dead-time effects in VSI feeding induction motors," *IEEE Trans. Ind. Appl.*, vol. 37, no. 3, pp. 856–863, May/Jun. 2001.

[25] H.-S. Kim, H.-W. Kim, and M.-J. Youn, "A new on-line dead-time compensation method based on time delay control," in *Proc. IEEE-IECON'01*, Denver, CO, 2001, pp. 1184–1189.
[26] T. Summers and R. E. Betz, "Dead-time issues in predictive current control," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Pittsburgh, PA, 2002, pp. 2086–2093.
[27] R. J. Kerkman, D. Leggate, D. W. Schlegel, and C. Winterhalter, "Effects of parasitics on the control of voltage source inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 140–150, Jan. 2003.
[28] J. Qian, A. Khan, and I. Batarseh, "Turn-off switching loss model and analysis of IGBT under different switching operation modes," in *Proc. IEEE IECON'95*, Orlando, FL, 1995, pp. 240–245.
[29] "Application characterization of IGBTs," International Rectifier, El Segundo, CA, App. Note INT-990, 2004.

Juan Manuel Guerrero (S'00–A'04–M'04) was born in Gijón, Spain, in 1973. He received the M.E. degree in industrial engineering and the Ph.D. degree in electrical and electronic engineering from the University of Oviedo, Gijón, Spain, in 1998 and 2003, respectively.

Since 1999, he has been a Teaching Assistant in the Department of Electrical, Computer and Systems Engineering, University of Oviedo. From February to October 2002, he was a Visitor Scholar at the University of Wisconsin, Madison. His research interests include parallel-connected motors fed by one inverter, sensorless control of induction motors, control systems, and digital signal processing.

Dr. Guerrero received an award from the College of Industrial Engineers of Asturias and León, Spain, for his M.E. thesis in 1999.

Michael Leetmaa (S'99) received the B.S. degree in mechanical engineering in 1991 from Stanford University, Stanford, CA, and M.S. degree in mechanical engineering in 1996 from the University of Wisconsin, Madison, where he is currently working toward the Ph.D. degree in mechanical engineering in the area of sensorless control of induction machines.

He was a Composites and Manufacturing Engineer with Hughes Aircraft Corporation. He was also with Kodak Corporation's Research and Development Laboratory, developing camera shutter actuators. His main interests are in controls and advanced drive technologies.

Mr. Leetmaa is a Member of the IEEE Industry Applications Society.

Fernando Briz (A'96–M'99) received the M.S. and Ph.D. degrees from the University of Oviedo, Gijón, Spain, in 1990 and 1996, respectively.

From June 1996 to March 1997, he was a Visiting Researcher at the University of Wisconsin, Madison. He is currently an Associate Professor in the Department of Electrical, Computer and Systems Engineering, University of Oviedo. His topics of interest include control systems, high-performance ac drives control, sensorless control, and digital signal processing.

Antonio Zamarrón received the B.S. degree in electromechanical engineering from the Instituto Tecnológico de León, León, México, in 1990, the M.S. degree in electrical engineering from the Instituto Tecnológico de la Laguna, Torreón, México, in 1992, and the Ph.D. degree in electrical engineering from the University of Oviedo, Gijón, Spain, in 1993.

Since 1993, he has been an Associate Professor at the Instituto Tecnológico de León, where from 1994 to 1999, he was the Head of the Electromechanical Department. From 1997 to 1999, he was an Automation Engineer at a water pump plant. His research interest is induction motors sensorless control.

Robert D. Lorenz (S'83–M'84–SM'91–F'98) received the B.S., M.S., and Ph.D. degrees from the University of Wisconsin, Madison, and the M.B.A. degree from the University of Rochester, Rochester, NY.

Since 1984, he has been a member of the faculty of the University of Wisconsin, Madison, where he is the Mead Witter Foundation Consolidated Papers Professor of Controls Engineering in both the Department of Mechanical Engineering and the Department of Electrical and Computer Engineering. He is Co-Director of the Wisconsin Electric Machines and Power Electronics Consortium, which celebrated its 20th anniversary in 2001. It is the largest industrial research consortium on motor drives in the world. He is also the thrust leader for control and sensor integration in the Center for Power Electronic Systems, an NSF Engineering Research Center (ERC) which is a joint ERC with Virgina Polytechnic Institute and State University, Rensselaer Polytechnic Institute, University of Puerto Rico-Mayaguez, and North Carolina A&T. From 1972 to 1982, he was a member of the research staff at the Gleason Works, Rochester, NY, working principally on high-performance drives and synchronized motion control. He was a Visiting Research Professor in the Electrical Drives Group, Catholic University of Leuven, Leuven, Belgium, in the summer of 1989 and in the Power Electronics and Electrical Drives Institute, Technical University of Aachen, Aachen, Germany, in the summers of 1987, 1991, 1995, 1997, and 1999, where he also was the SEW Eurodrive Guest Professor from September 1, 2000 until July 7, 2001. In 1969–1970, he conducted Master thesis research in adaptive control of machine tools at the Technical University of Aachen. His current research interests include sensorless electromagnetic motor/actuator technologies, real-time signal processing and estimation techniques, precision multiaxis motion control, and ac/dc drive and high-precision machine control technologies. He has authored more than 170 published technical papers and is the holder of 20 patents, with two more pending.

Dr. Lorenz is the IEEE Division II Director for 2005/2006, was the IEEE Industry Applications Society (IAS) President for 2001, a Distinguished Lecturer of the IAS for 2000/2001, immediate past Chair of the IAS Awards Department, and past Chairman of the IAS Industrial Drives Committee, and is a member of the IAS Industrial Drives, Electric Machines, Industrial Power Converter, and Industrial Automation and Control Committees. He is also the current Chair of the Periodicals Committee for the IEEE Technical Activities Board. He is a member of the IEEE Sensor Council AdCom. He was awarded the 2003 IEEE IAS Outstanding Achievement award, which honors his outstanding contributions and technological developments in the application of electricity to industry. He has won 17 prize paper awards. He is a Member of the American Society of Mechanical Enginees, Instrument Society of America, and The International Society for Optical Engineers. He is a Registered Professional Engineer in the States of New York and Wisconsin.